SECURE CONNECTIONS
FOR A SMARTER WORLD

Speed Up Automotive, Industrial, and IoT Applications with NXP Model-Based Design Toolbox

Daniel Scurtu

MATLAB EXPO 2021

A POSITION OF STRENGTH TO BETTER SERVE OUR 26,000+ CUSTOMERS

We accelerate breakthroughs that advance the world through our semiconductor technology leadership

EMPLOYEES IN

30+ COUNTRIES

Headquartered in Eindhoven, Netherlands

~29,000

EMPLOYEES

60+

Year History

~11,000

Engineers

9,500

Patent Families

$8.61B

Annual Revenue [1]

[1] Posted revenue for 2020 – Please refer to the Financial Information page of the Investor Relations section of our website at www.nxp.com/investor for additional information

A POSITION OF STRENGTH TO BETTER SERVE OUR 26,000+ CUSTOMERS

We accelerate breakthroughs that advance the world through our semiconductor technology leadership

EMPLOYEES IN

30+ COUNTRIES

Headquartered in Eindhoven, Netherlands

~29,000

EMPLOYEES

60+

Year History

~11,000

Engineers

9,500

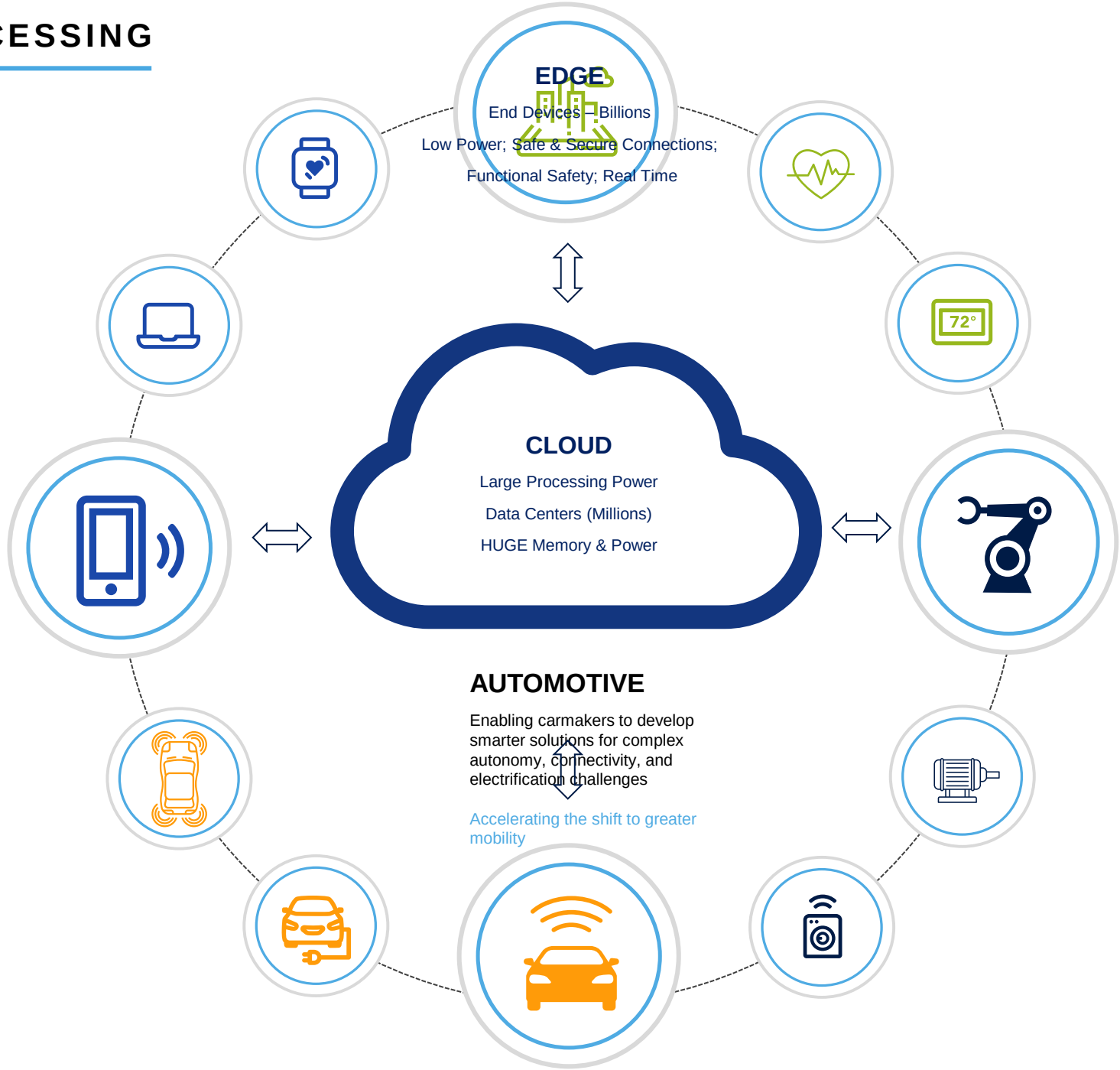
Patent Families

$8.61B

Annual Revenue [1]

[1] Posted revenue for 2020 – Please refer to the Financial Information page of the Investor Relations section of our website at www.nxp.com/investor for additional information

NXP - EDGE PROCESSING



MOBILE

Giving wearable and mobile devices easier access to the services that make modern life more convenient without compromising security and safety.

Transforming how people and devices connect

SMART CITY

Simplifying how people access and interact with local services to achieve new standards of sustainability, efficiency, mobility, and economic growth.

Anticipating the demands of tomorrow

COMMUNICATION INFRASTRUCTURE

Powering insights and inspiring performance with hardware solutions for handling 5G connectivity across the emerging communications spectrum.

Delivering real-time responsiveness at the speed of 5G

INDUSTRIAL

Reducing wasted time, money, and effort by helping business run more efficiently.

Enabling more efficient data processing

NXP - EDGE PROCESSING

MOBILE

Giving wearable and mobile devices easier access to the services that make modern life more convenient without compromising security and safety.

Transforming how people and devices connect

COMMUNICATION INFRASTRUCTURE

Powering insights and inspiring performance with hardware solutions for handling 5G connectivity across the emerging communications spectrum.

Delivering real-time responsiveness at the speed of 5G

SMART CITY

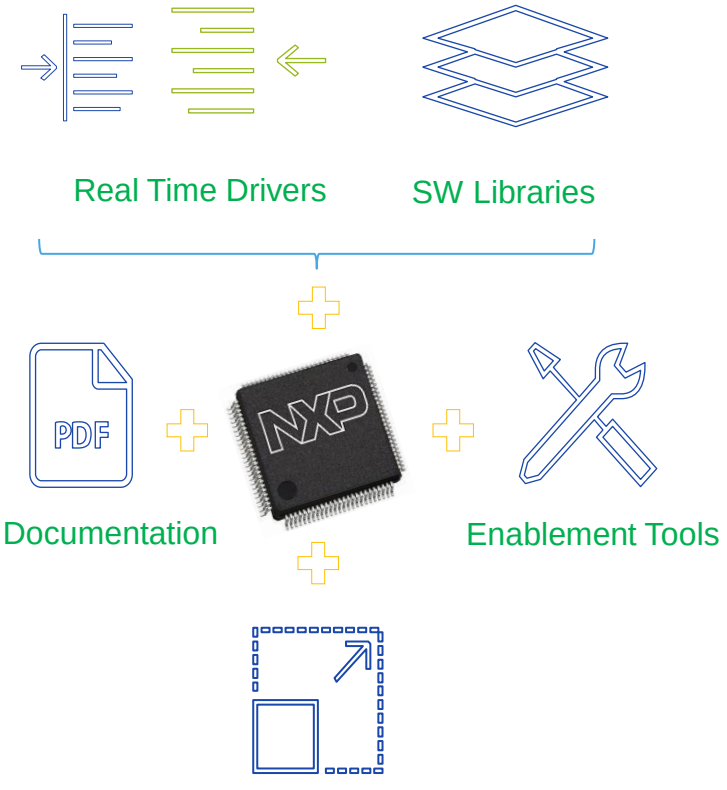
Simplifying how people access and interact with local services to achieve new standards of sustainability, efficiency, mobility, and economic growth.

Anticipating the demands of tomorrow

INDUSTRIAL

Reducing wasted time, money, and effort by helping business run more efficiently.

Enabling more efficient data processing


Real Time Drivers
SW Libraries
PDF
Documentation
Enablement Tools
Reference Design Solution

Real Time Drivers

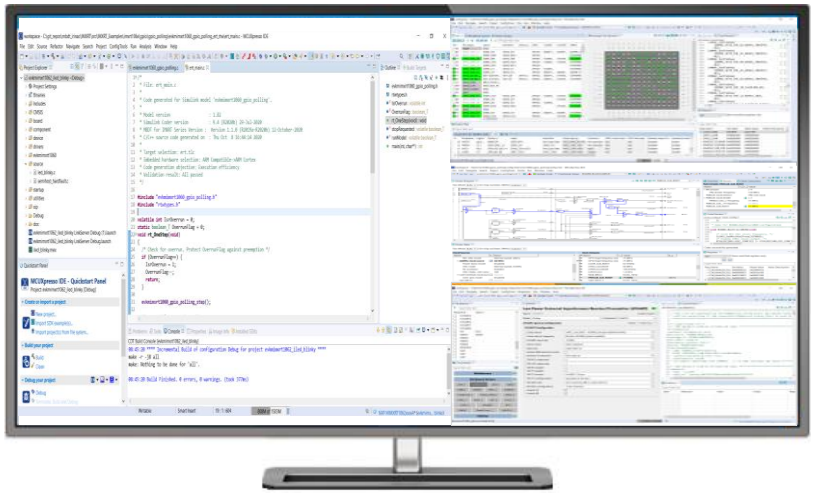
SW Libraries

Documentation

Enablement Tools

Reference Design Solution

MCUXpresso – IDE – Debugger - Toolchains



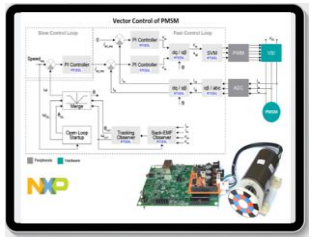
Pins Tool

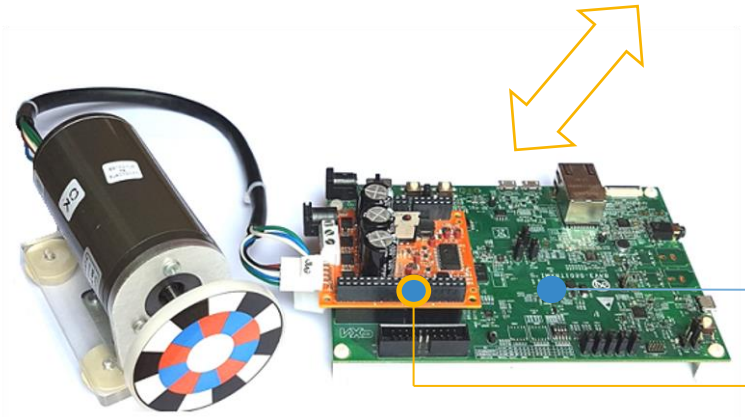
Clocks Tool

Peripheral Tool

FreeMASTER

FreeMASTER Lite



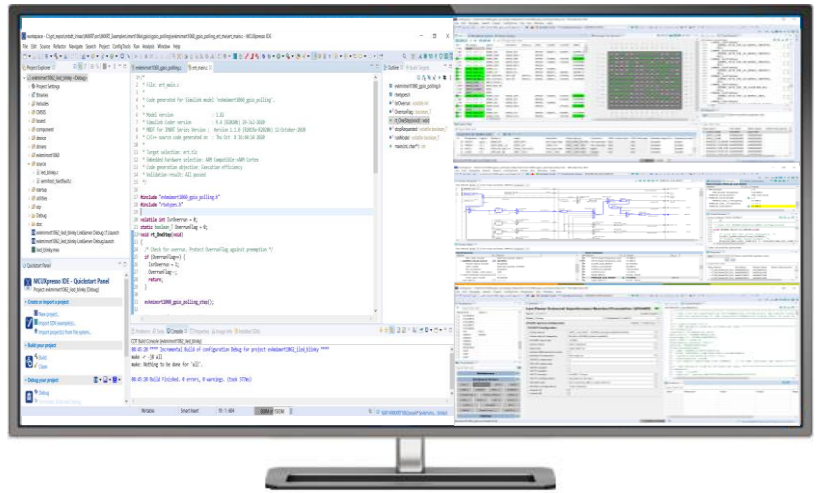


Serial Connection - UART

Debug Connection - JTAG

i.MX RT1060 EVK

MCUXpresso – IDE – Debugger - Toolchains



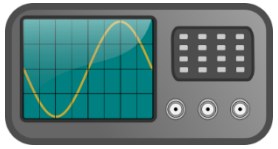
Pins Tool

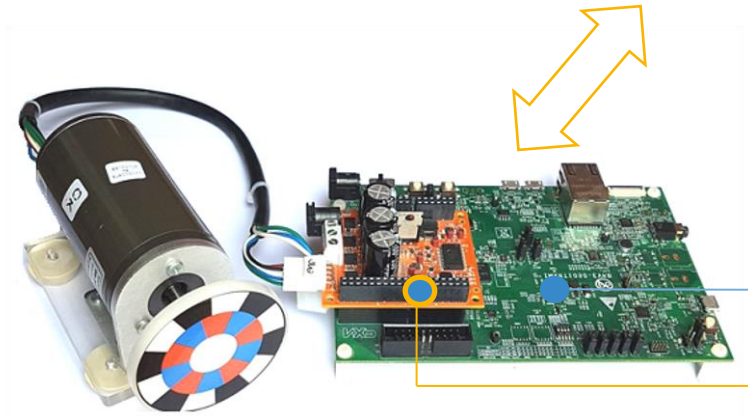
Clocks Tool

Peripheral Tool

FreeMASTER

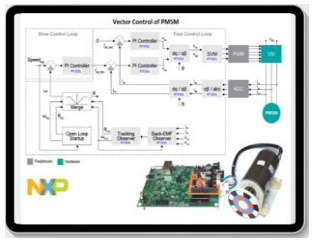
FreeMASTER Lite



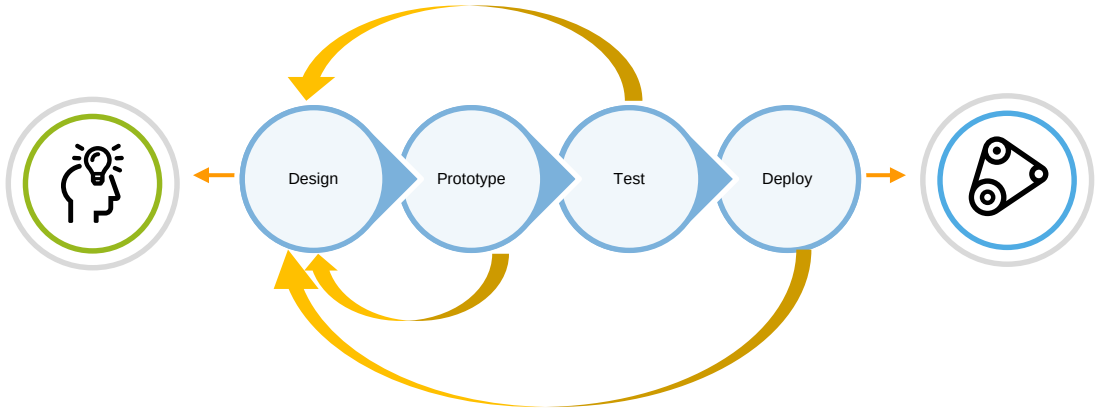


Serial Connection - UART

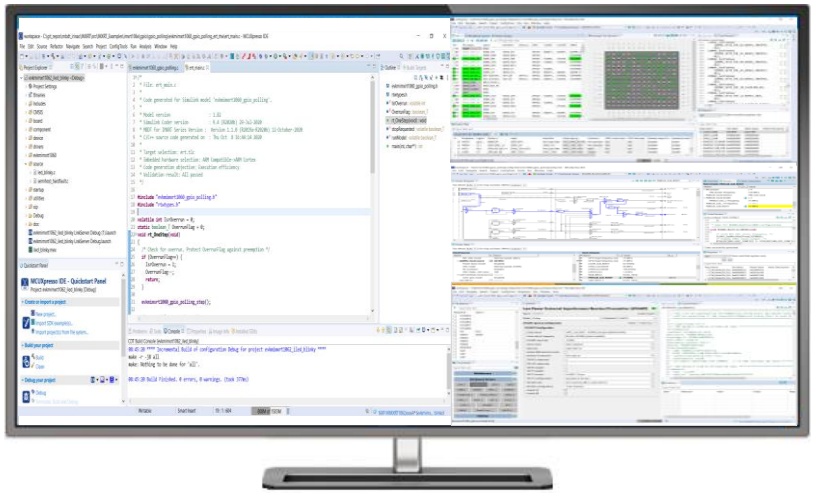
Debug Connection - JTAG



i.MX RT1060 EVK



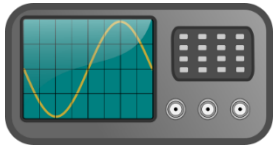
MCUXpresso – IDE – Debugger - Toolchains



Pins Tool

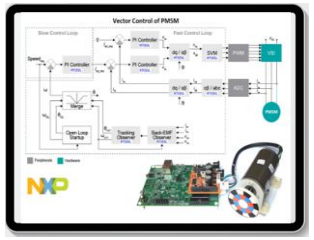
Clocks Tool

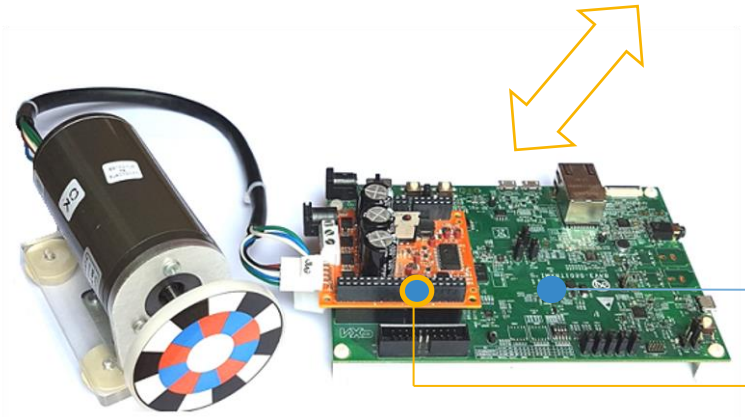
Peripheral Tool



FreeMASTER

FreeMASTER Lite



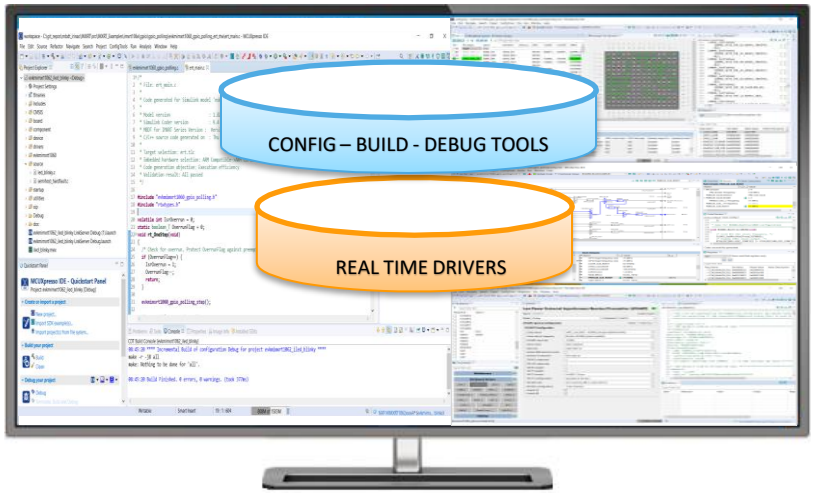


Serial Connection - UART

Debug Connection - JTAG

i.MX RT1060 EVK

MCUXpresso – IDE – Debugger - Toolchains



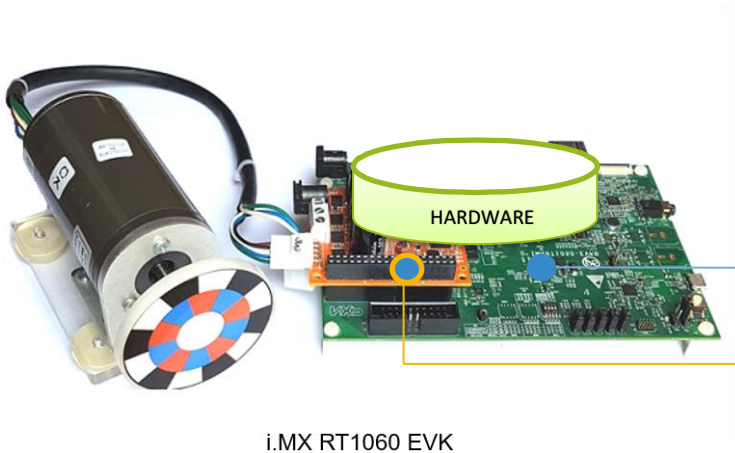
Pins Tool

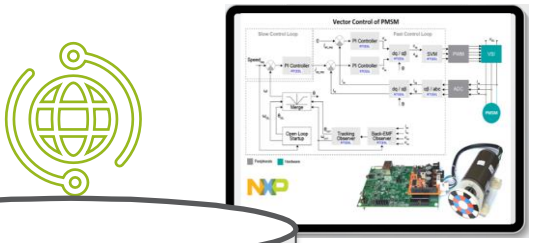
Clocks Tool

Peripheral Tool

FreeMASTER

FreeMASTER Lite



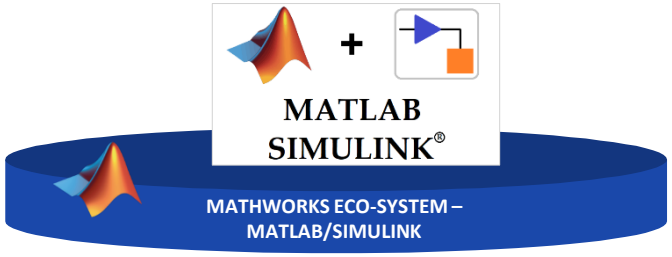


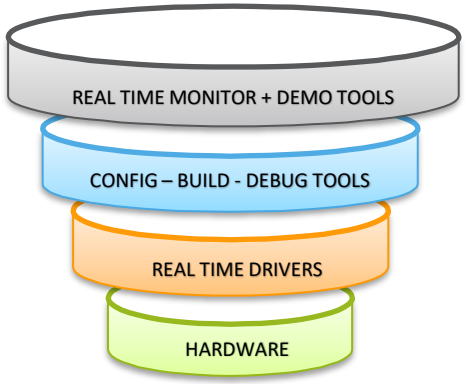
REAL TIME MONITOR + DEMO TOOLS

Serial Connection - UART

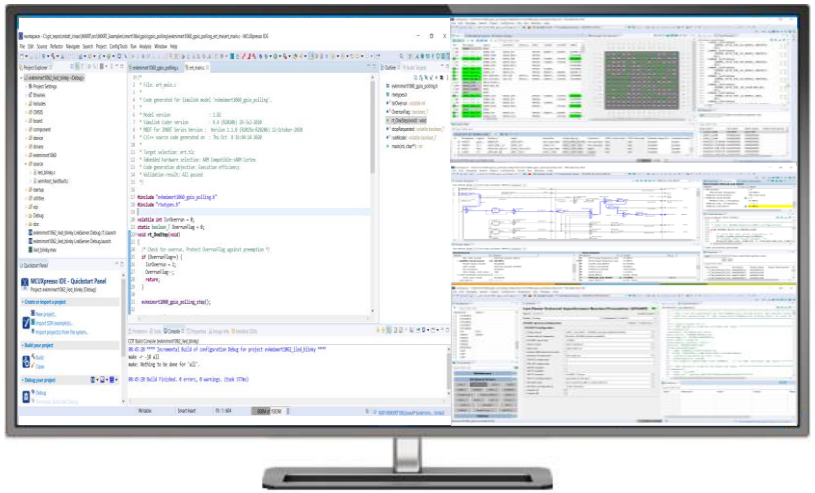
Debug Connection - JTAG

i.MX RT1060 EVK





MCUXpresso – IDE – Debugger - Toolchains



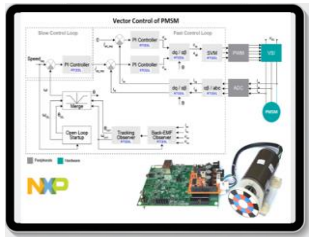
Pins Tool

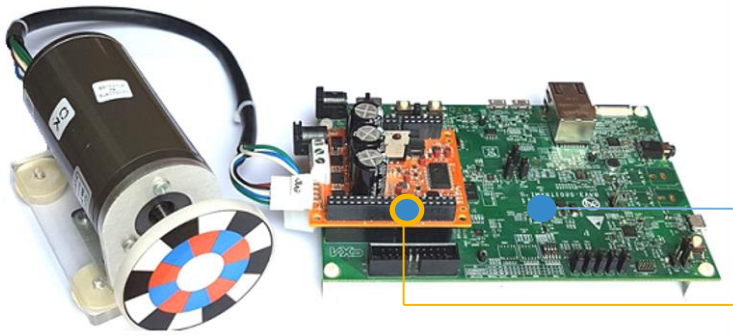
Clocks Tool

Peripheral Tool

FreeMASTER

FreeMASTER Lite





Serial Connection - UART

Debug Connection - JTAG

i.MX RT1060 EVK

MATLAB
SIMULINK®

MATHWORKS ECO-SYSTEM –
MATLAB/SIMULINK

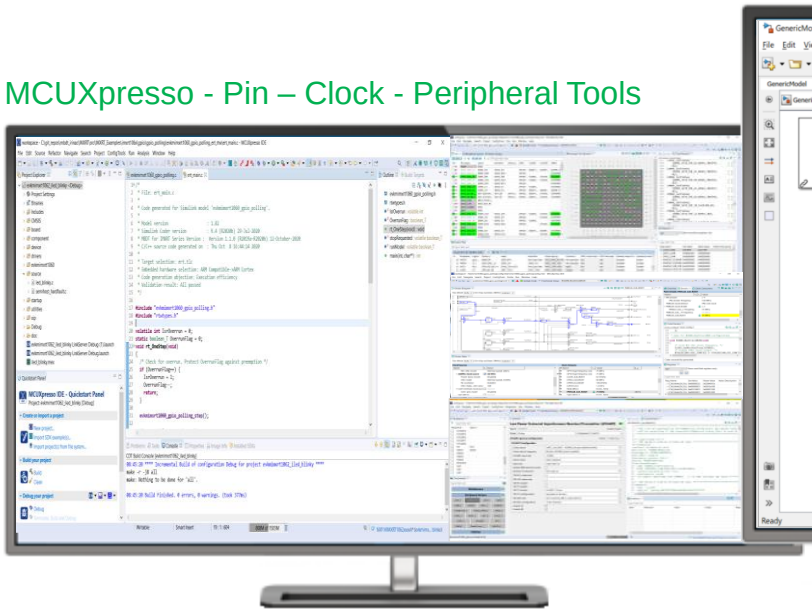
REAL TIME MONITOR + DEMO TOOLS

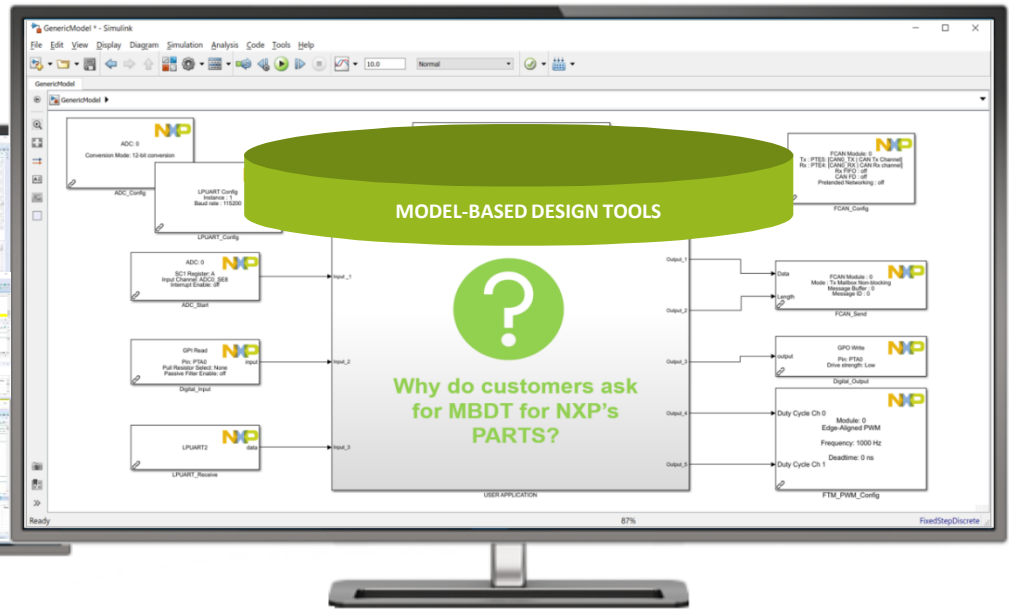
CONFIG – BUILD - DEBUG TOOLS

REAL TIME DRIVERS

HARDWARE

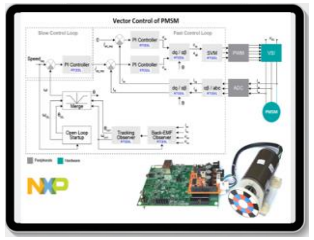
MCUXpresso - Pin – Clock - Peripheral Tools

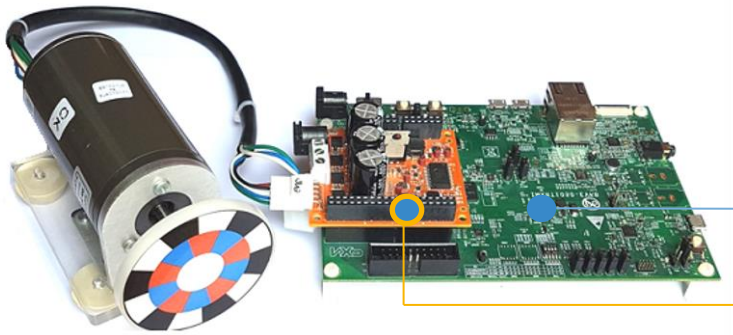




FreeMASTER

FreeMASTER Lite

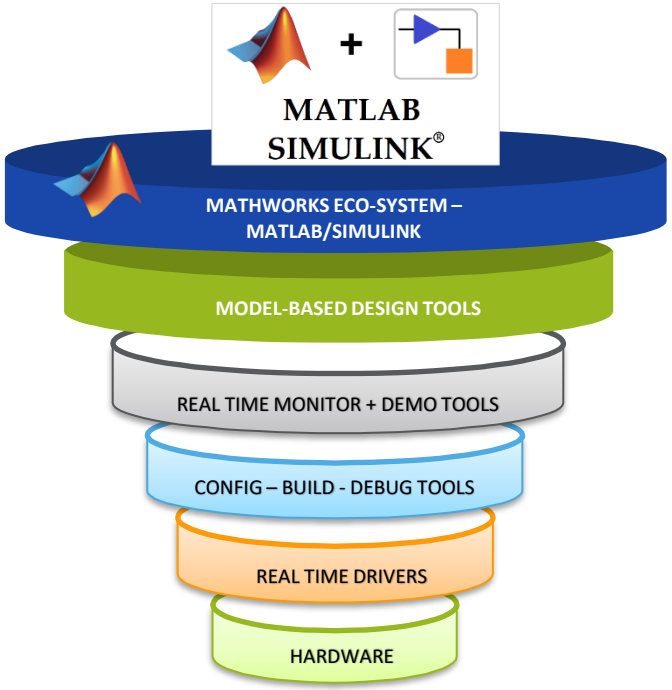




Serial Connection - UART

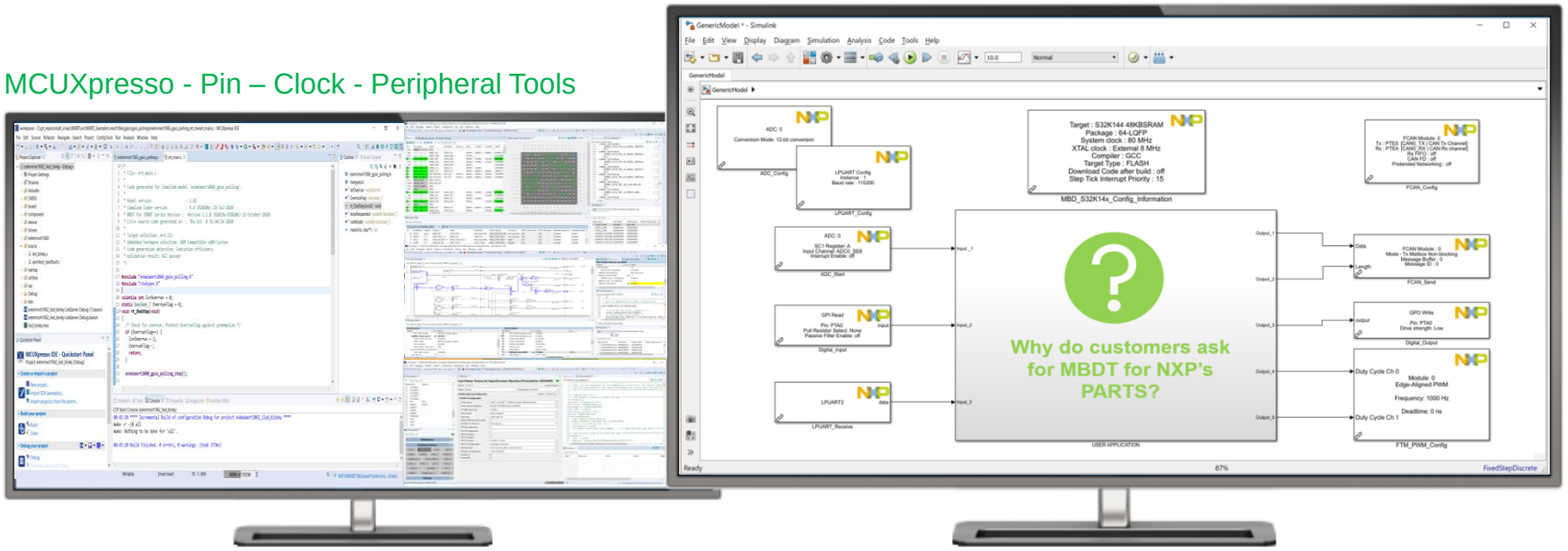
Debug Connection - JTAG

i.MX RT1060 EVK



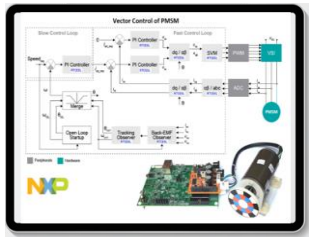
Model-Based Design Tools for Simulink

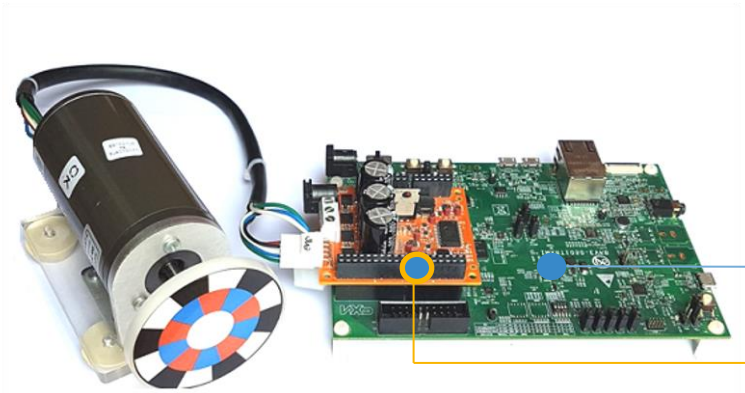
MCUXpresso - Pin – Clock - Peripheral Tools



FreeMASTER

FreeMASTER Lite

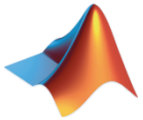




Serial Connection - UART

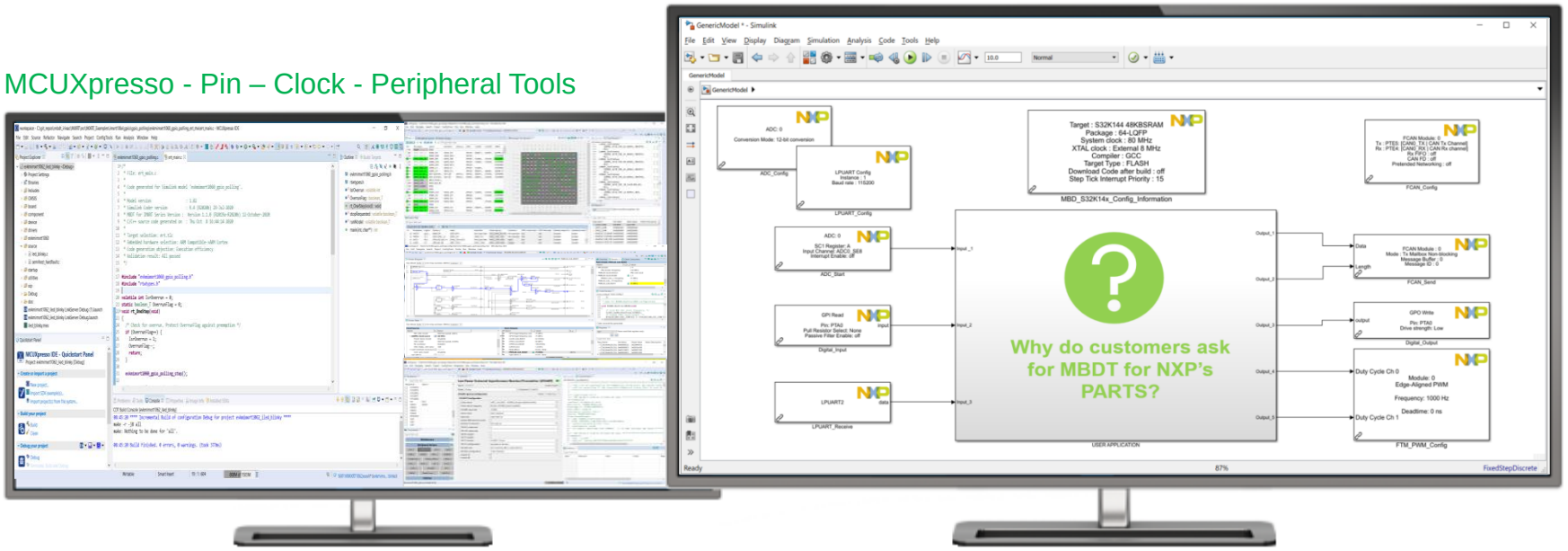
Debug Connection - JTAG

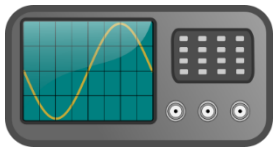
i.MX RT1060 EVK



Model-Based Design Tools for Simulink

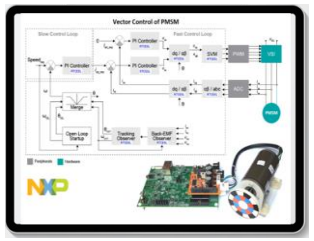
MCUXpresso - Pin – Clock - Peripheral Tools

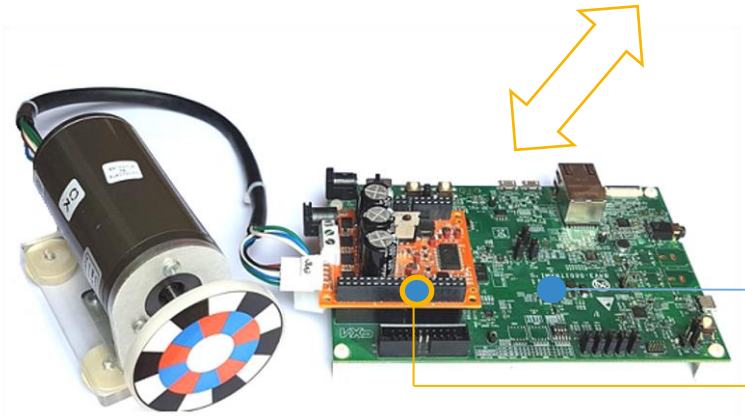




FreeMASTER

FreeMASTER Lite





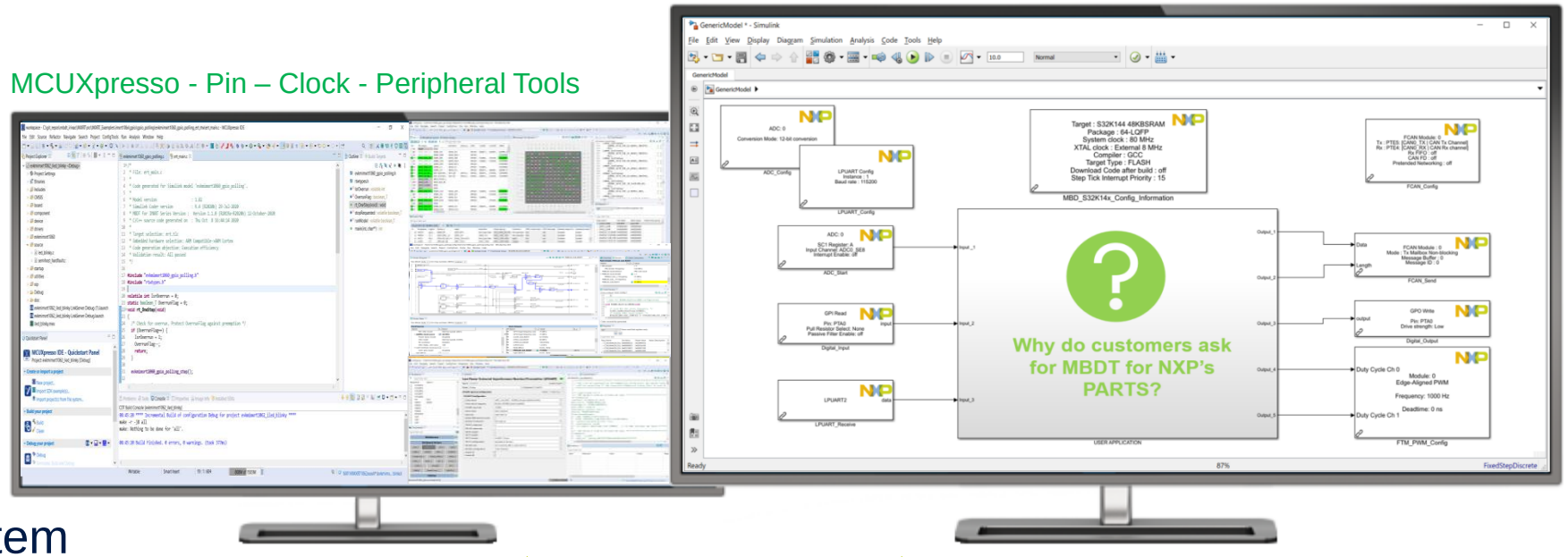
Serial Connection - UART

Debug Connection - JTAG

i.MX RT1060 EVK

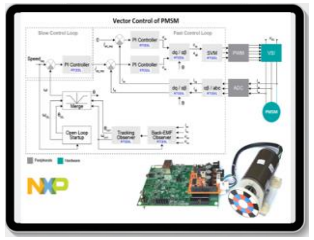
- FAST - Time To Market
- EASY To Use - Reuse
- SIMULATION
- RICH MATH IP/Libraries
- LEVERAGE NXP Eco-System

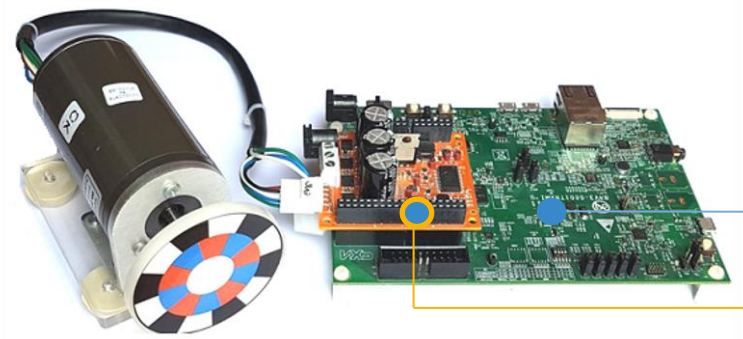
MCUXpresso - Pin – Clock - Peripheral Tools



FreeMASTER

FreeMASTER Lite



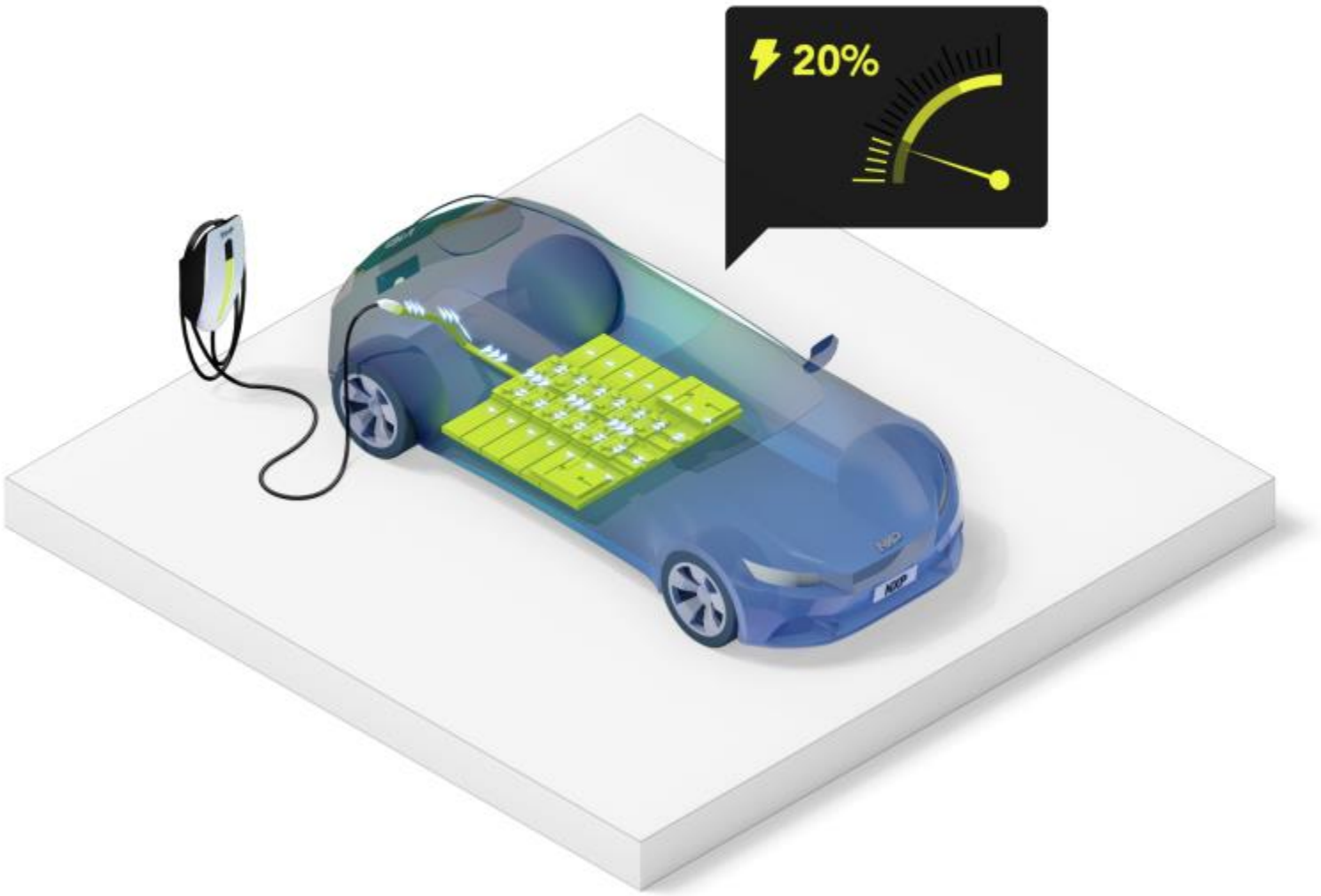


Serial Connection - UART

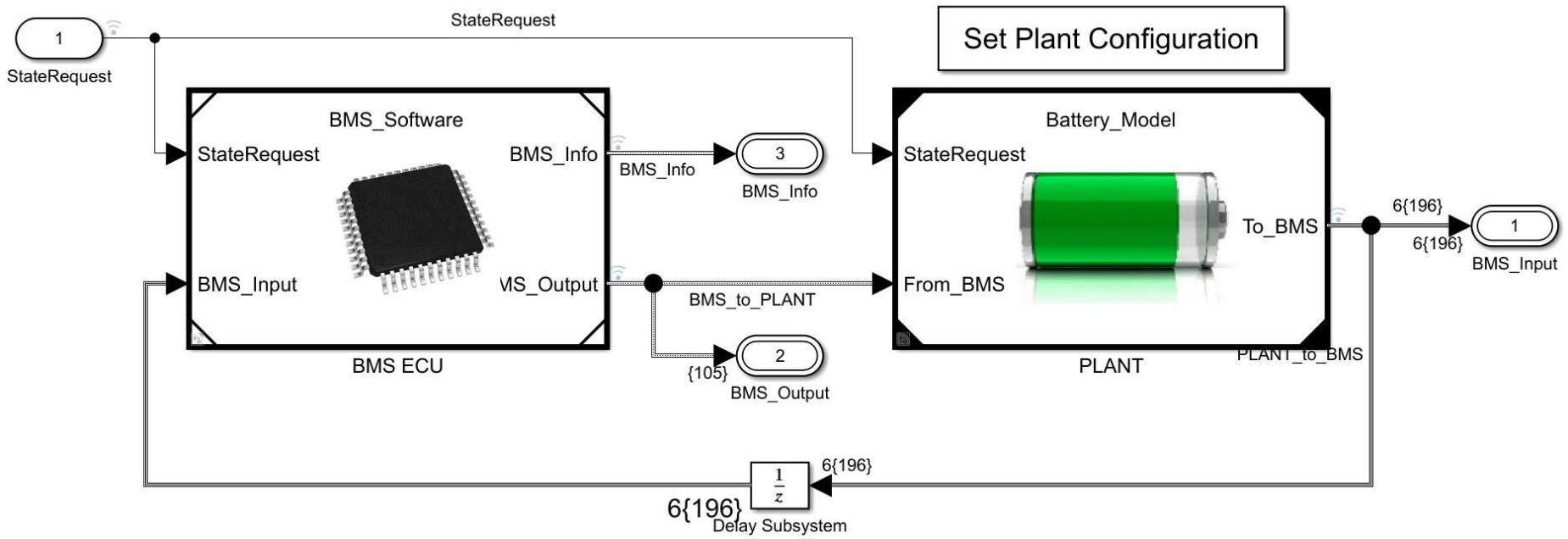
Debug Connection - JTAG

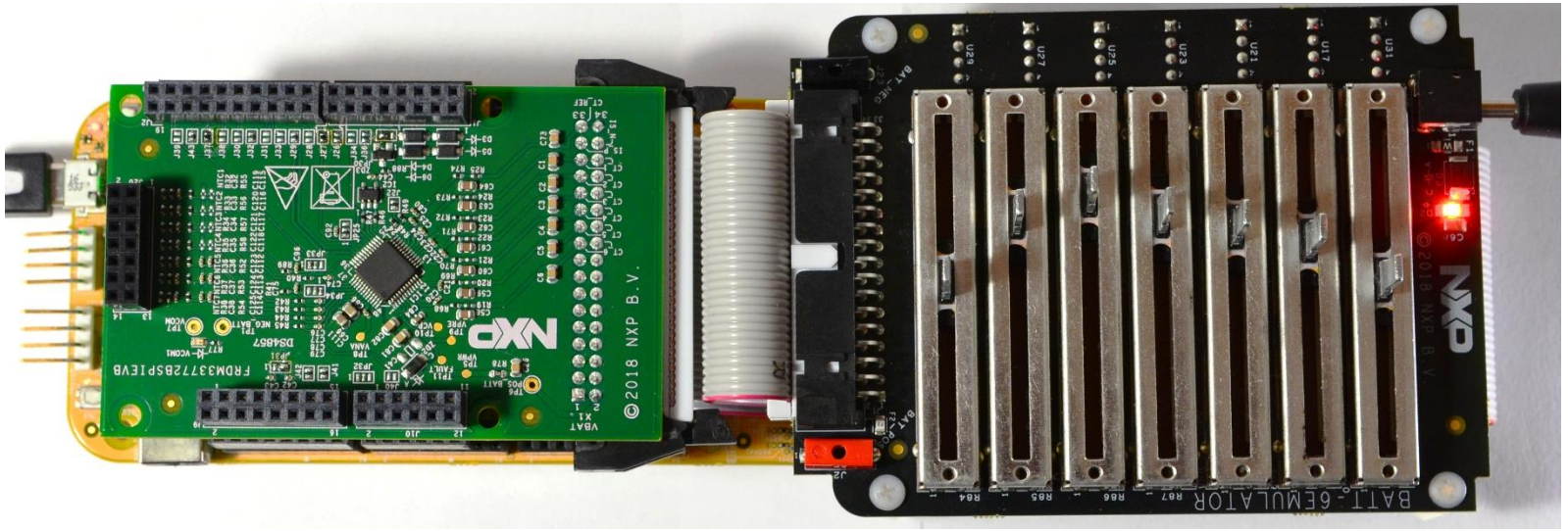
i.MX RT1060 EVK

BATTERY MANAGEMENT SYSTEM



BATTERY MANAGEMENT SYSTEM





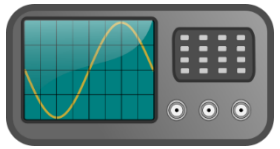
S32K142 + MC33772B

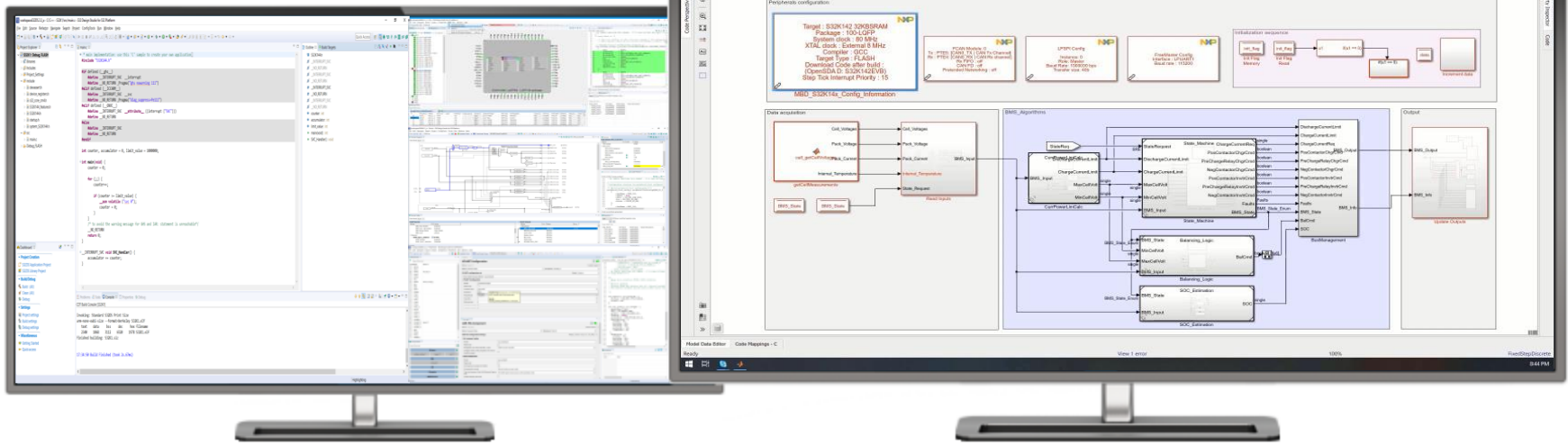
NXP BATT – 6EMULATOR

BATTERY MANAGEMENT SYSTEM

Model-Based Design Tools for Simulink

S32 Design Studio + Pin – Clock - Peripheral Tools

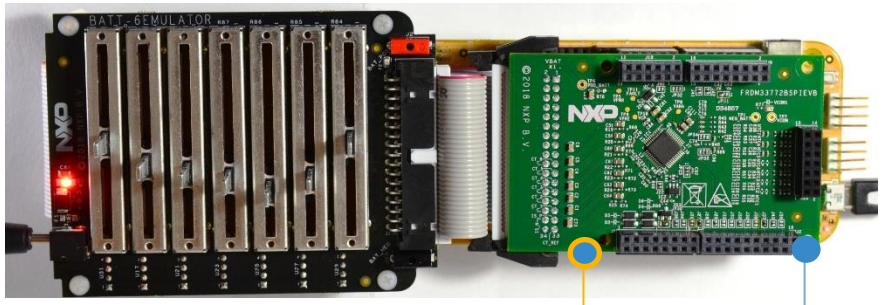


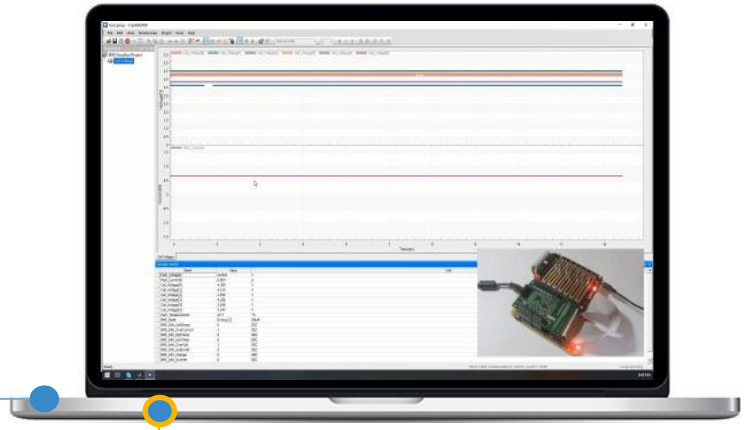


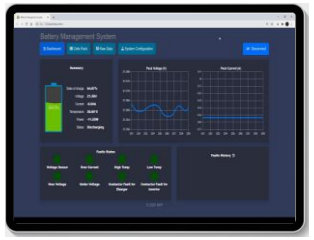
BMS Monitor

FreeMASTER

FreeMASTER Lite

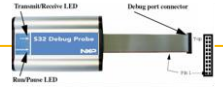






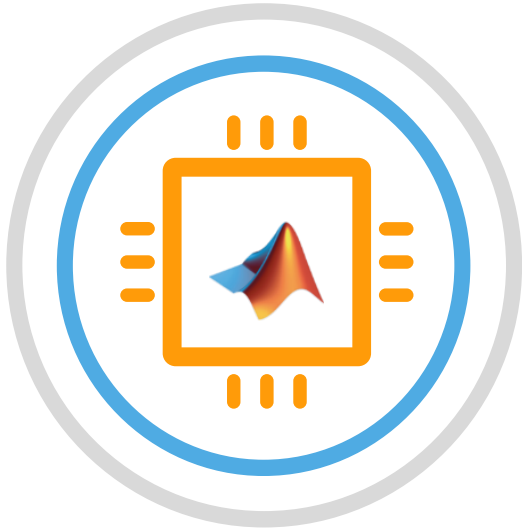
Serial Connection - UART

Debug Connection - JTAG



NXP – MATLAB SIMULINK TOOLBOXES

A COMPLETE SOLUTION



File Exchange - MATLAB Central

mathworks.com/matlabcentral/fileexchange/?q=NXP&sort=relevancy&source%5B%5D=community&type%5B%5D=toolboxes_and_products

MathWorks® Products Solutions Academia Support Community Events Get MATLAB

File Exchange

Clear Filters × NXP File Exchange

MATLAB Central | Files | Authors | My File Exchange | Contribute | About Trial software

Filter by Source
- Community 7

Filter by Category

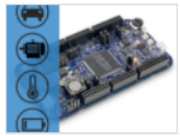
Workflows
- Code Generation 1

Applications
- Image Processing and Computer Vision 1
- AI, Data Science, and Statistics 1
- Signal Processing 1
- Control Systems 1

Filter by Type
- Toolboxes 7
- Hardware Support Packages 3
- Functions 7

Filter by Product Family
- MATLAB 7
- Simulink 2

7 RESULTS Subscribe Sort By: Relevancy



NXP Support Package MPC57xx version 1.2.0 by NXP Model-Based Design Toolbox Team

This package represents the MATLAB Installer add-on for the FREE of cost, NXP's Model-Based Design Toolboxes.

Following are the steps to install NXP's Model-Based Design Toolbox for MPC57xx Automotive Microprocessors family:1. Go to Add-On Manager in MATLAB and select the NXP Support Package MPC57xx

Toolbox

49 Downloads
Updated 14 Apr 2020

NXP Support Package S32K1xx version 2.2.0 by NXP Model-Based Design Toolbox Team

This package represents the MATLAB Installer add-on for the FREE of cost, NXP's Model-Based Design Toolboxes.

Note: It is recommended to uninstall and delete all files/folder of the older versions of NXP Model-Based Design S32K1xx Toolbox before installing the new versions.The steps to install NXP

Toolbox

96 Downloads
Updated 21 Jul 2020

NXP_Support_Package_S32V234 version 2.2.0 by NXP Model-Based Design Toolbox Team

This toolbox represents the MATLAB Installer Add-On for the NXP Vision Toolbox for S32V234

To install the NXP Vision Toolbox for S32V234 Automotive Vision Processor, please follow these steps:1. Go to MATLAB Add-On Manager and select the NXP Support Package S32V234 toolbox.2. Select Open

Toolbox

7 Downloads
Updated 14 Oct 2019

NXP Support Package KVx version 1.0.0 by NXP Model-Based Design Toolbox Team

This package represents the MATLAB Installer add-on for the FREE of cost, NXP's Model-Based Design Toolboxes.

Following are the steps to install NXP's Model-Based Design Toolbox for KVx Series of MCUs:1. Go to Add-On Manager in MATLAB and select the NXP Support Package KVx toolbox. Select Open Folder option

Toolbox

5 Downloads
Updated 21 Dec 2020

NXP_Support_Package_S32R version 1.5.0 by NXP Model-Based Design Toolbox Team

This toolbox represents the MATLAB Installer Add-On for the NXP RADAR Toolbox for S32R

To install the NXP RADAR Toolbox for S32R, please follow these steps:1. Go to MATLAB Add-On Manager and select the NXP Support Package S32R toolbox.2. Select Open Folder option to navigate to the

Toolbox

15 Downloads
Updated 30 Oct 2020

NXP Support Package S12ZVMx version 1.0.0 by NXP Model-Based Design Toolbox Team

This package represents the MATLAB Installer add-on for the FREE of cost, NXP's Model-Based Design Toolboxes.

Note: It is recommended to uninstall and delete all files/folders of the older versions of the NXP Model-Based Design S12ZVMx Toolbox before installing the new versions.The steps to install NXP

Toolbox

9 Downloads
Updated 9 Sep 2020

NXP Support Package IMXRT1xxx version 1.1.0 by NXP Model-Based Design Toolbox Team

This package represents the MATLAB Installer add-on for the FREE of cost, NXP's Model-Based Design Toolboxes.

Following are the steps to install NXP's Model-Based Design Toolbox for IMXRT 1xxx Series of Crossover MCUs:1. Go to Add-On Manager in MATLAB and select the NXP Support Package IMXRT1xxx toolbox

Toolbox

9 Downloads
Updated 12 Oct 2020

MATLAB R2020b

HOME PLOTS

New Script | New Live Script | New | Open

FILE

Current Folder

Name

Folder
- external_devices
- FreeMaster
- lic
- mbdtbx_s32k
- mbdtbx_s32k11x
- mbdtbx_s32k14x
- mbdtbx_s32k_as
- S32_Examples
- S32_Platform_SDK
- tools

Chrome HTML Document
- LA_OPT_NXP_Software_Lic

Function
- mbd_find_s32k_root.m
- mbd_s32k_path.m

Script
- Contents.m

PNG File
- nxp_logo.png

Text Document
- readme.txt
- Software_Content_Register

XML Document
- info.xml

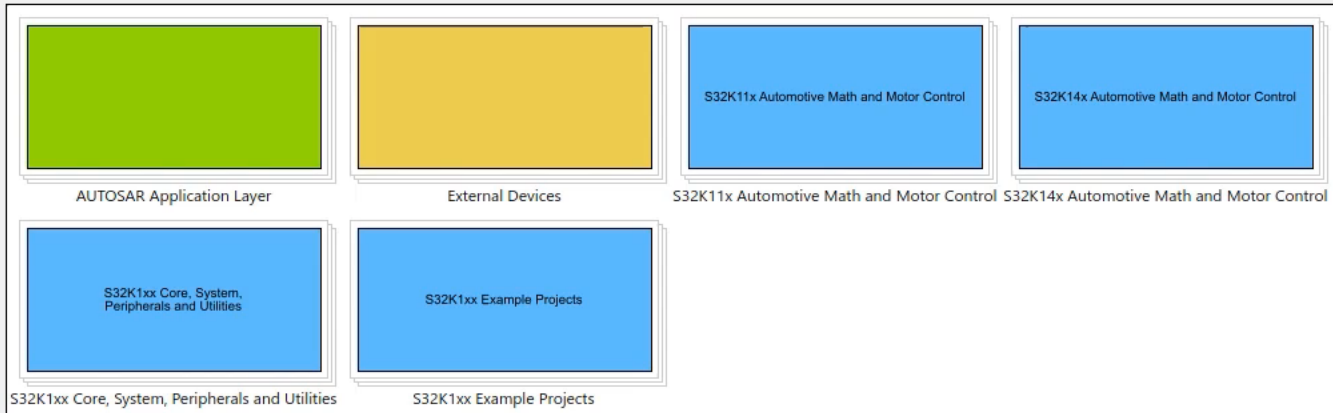
S32_Examples (Folder)

Simulink Library Browser

scope

NXP Model-Based Design Toolbox for S32K1xx MCUs

- NXP Model-Based Design Toolbox for i.MX RT MCUs
  - i.MX RT1xxx Core, System, Peripherals and Utilities
  - i.MX RT1xxx Example Projects
    - Generic Simulink Models
    - i.MX RT 101x Simulink Models
    - i.MX RT 106x Simulink Models
  - i.MX RT1xxx RTCESL
- NXP Model-Based Design Toolbox for MPC57xx MCUs
  - AUTOSAR Application Layer
  - External devices
  - MPC57xx Core, System, Peripherals and Utilities
  - MPC57xx Automotive Math and Motor Control
  - MPC57xx Example Projects
- NXP Model-Based Design Toolbox for S32K1xx MCUs
  - AUTOSAR Application Layer
  - External Devices
  - S32K11x Automotive Math and Motor Control
  - S32K14x Automotive Math and Motor Control
  - S32K1xx Core, System, Peripherals and Utilities
  - S32K1xx Example Projects
- Simulink
- Automated Driving Toolbox
- AUTOSAR Blockset
- Computer Vision Toolbox
- Control System Toolbox
- Deep Learning Toolbox
- DSP System Toolbox
- DSP System Toolbox HDL Support
- Embedded Coder
- Embedded Coder Support Package for ARM Cortex-M Processors
- Fixed-Point Designer
- HDL Coder
- Image Acquisition Toolbox
- Model Predictive Control Toolbox
- Motor Control Blockset
- NXP Model-Based Design Toolbox for Kinetis V series
  - Kinetis Vx Core, System, Peripherals and Utilities
  - Kinetis Vx Example Projects
  - Kinetis Vx RTCESL
- Phased Array System Toolbox
- Report Generator
- Sensor Fusion and Tracking Toolbox
- Simscape
- Simulink 3D Animation
- Simulink Coder
- Simulink Control Design
- Simulink Design Optimization
- Simulink Design Verifier
- Simulink Desktop Real-Time
- Simulink Extras
- Simulink Real-Time



Sign In

NXP Model-Based Design Tools

Model-Based Design Tools for Matlab and Simulink Support

S32K1xx

- How to
- Tutorials
- Videos

MPC57xx

- How to
- Tutorials
- Videos

S12ZVM

- How to
- Tutorials
- Videos

i.MX RT

- How to
- Tutorials
- Videos

Kinetis V

- How to
- Tutorials
- Videos

Other Solutions

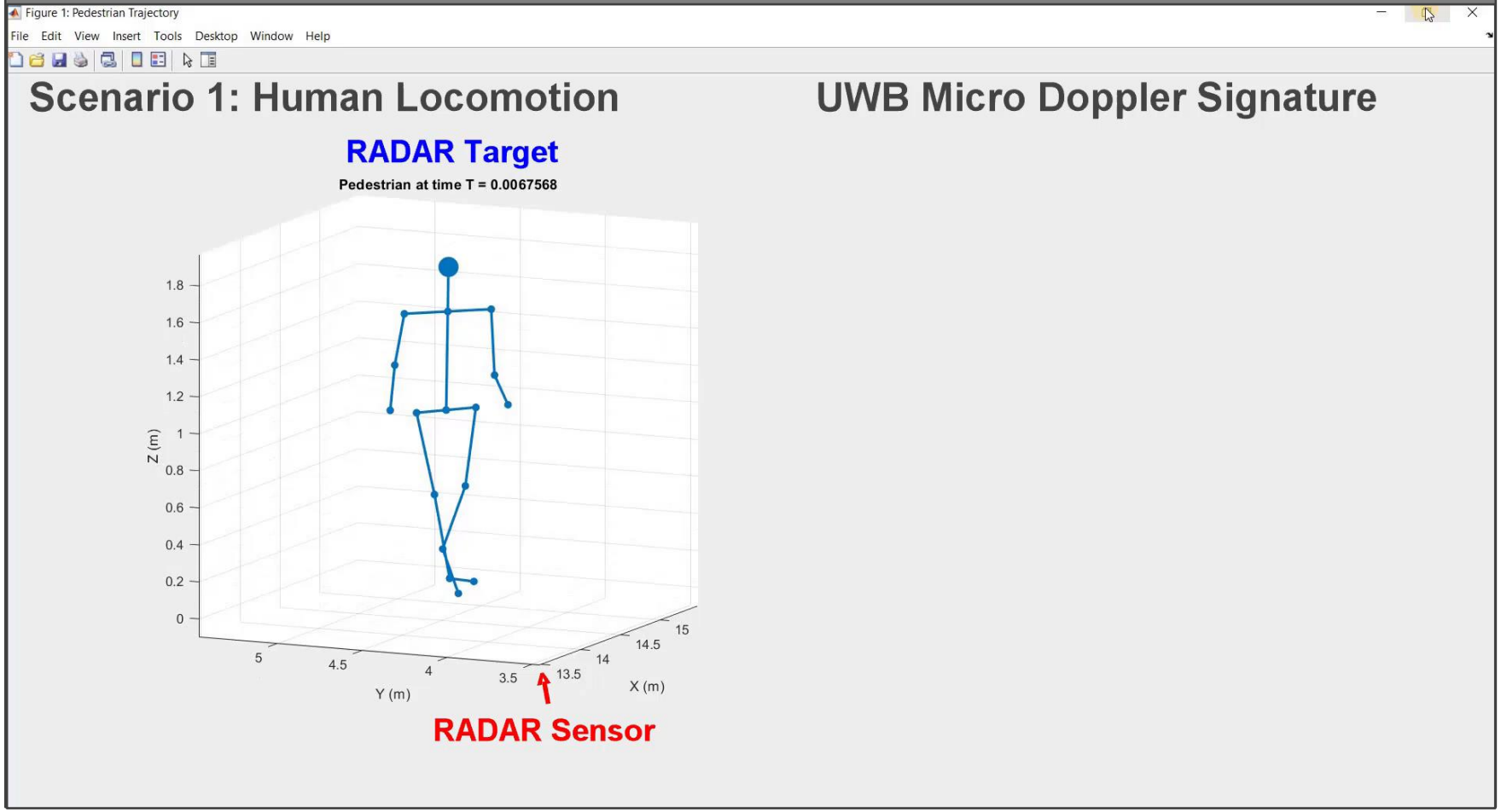
- Tips and Tricks

The Model-Based Design Toolbox provides an integrated development environment and toolchain for configuring and generating all of the

FIND OUT FOR MORE

- NXP BOOTH
- NXP.COM
- NXP COMMUNITY

MATLAB Simulation: RADAR Target Generation, Signal Acquisition, CNN Training & Predictions

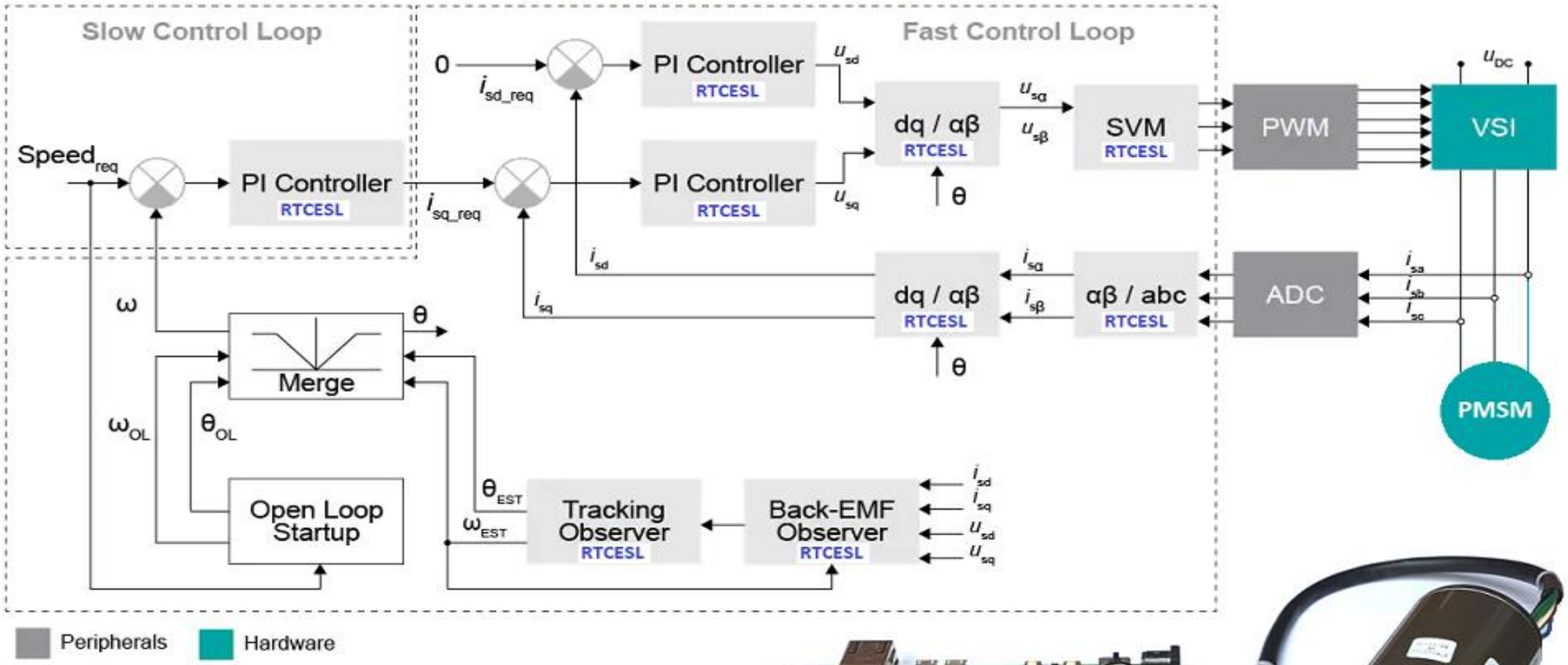


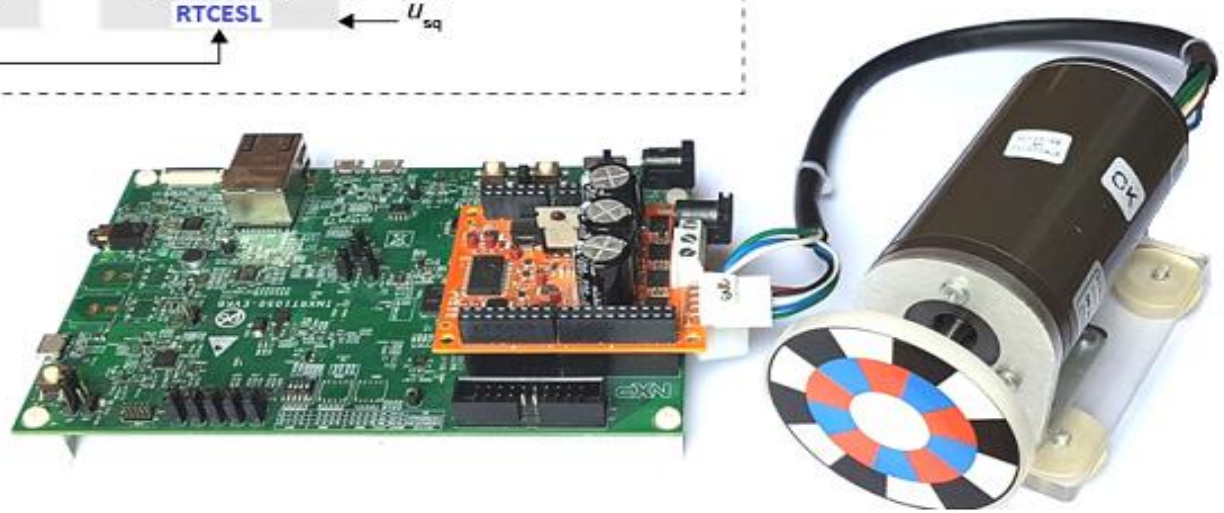
MATLAB EXPO 2021

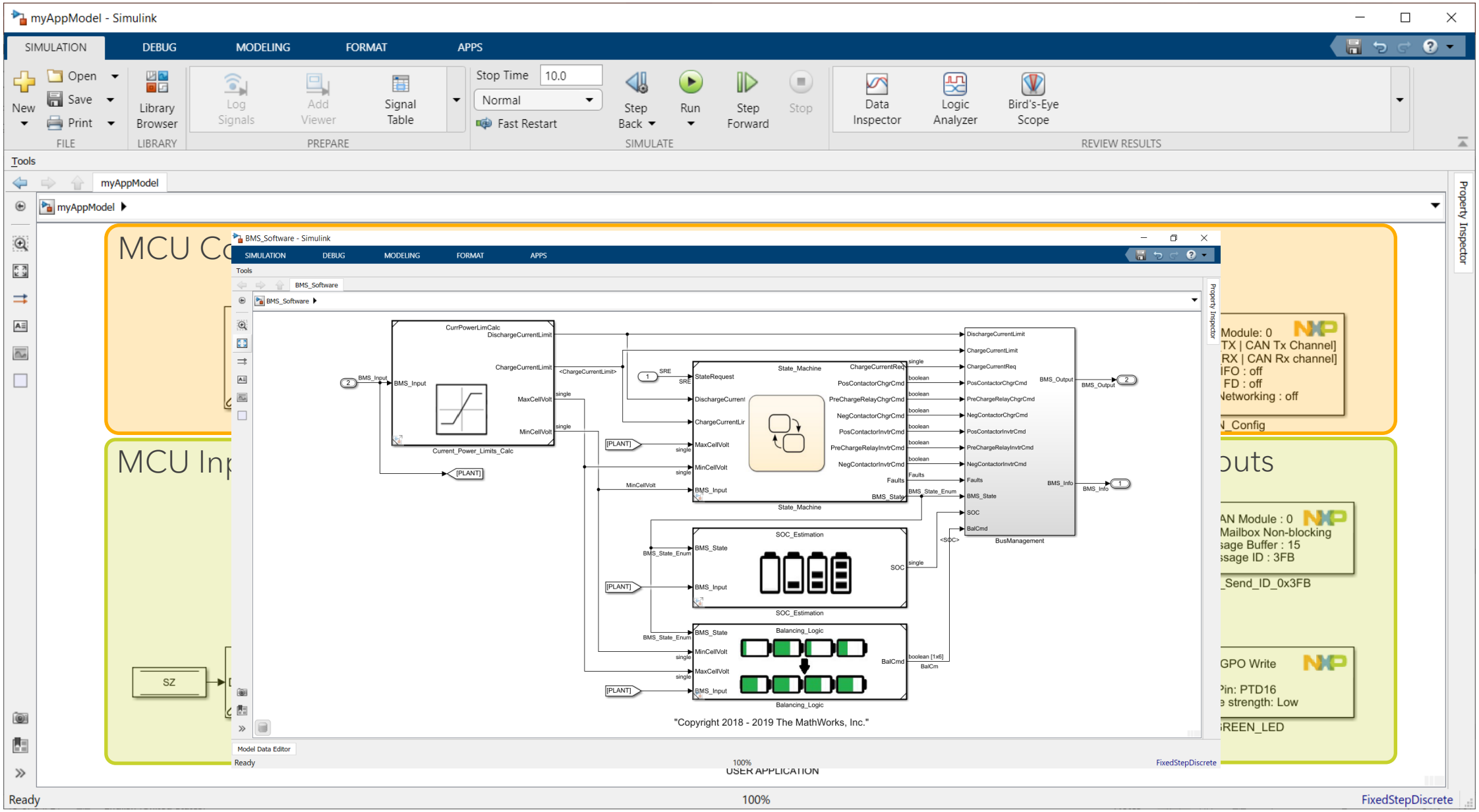
Thank you

i.MX RT1060 EVK

Vector Control of PMSM






myAppModel - Simulink
SIMULATION
DEBUG
MODELING
FORMAT
APPS
New
Open
Save
Print
FILE
Library Browser
LIBRARY
Log Signals
Add Viewer
Signal Table
PREPARE
Stop Time
10.0
Normal
Fast Restart
Step Back
Run
Step Forward
Stop
SIMULATE
Data Inspector
Logic Analyzer
Bird's-Eye Scope
REVIEW RESULTS
Tools
myAppModel
Property Inspector
MCU Co
MCU Inp
BMS_Software - Simulink
BMS_Software
CurrPowerLimCalc
Current_Power_Limits_Calc
State_Machine
SOC_Estimation
Balancing_Logic
BusManagement
"Copyright 2018 - 2019 The MathWorks, Inc."
Model Data Editor
Ready
100%
FixedStepDiscrete
USER APPLICATION
SZ
Module: 0
RX | CAN Rx channel]
FD : off
Networking : off
_Config
outs
AN Module : 0
Mailbox Non-blocking
sage Buffer : 15
ssage ID : 3FB
_Send_ID_0x3FB
GPO Write
Pin: PTD16
e strength: Low
REEN_LED
Ready
100%
FixedStepDiscrete

mc_pmsm - FreeMASTER

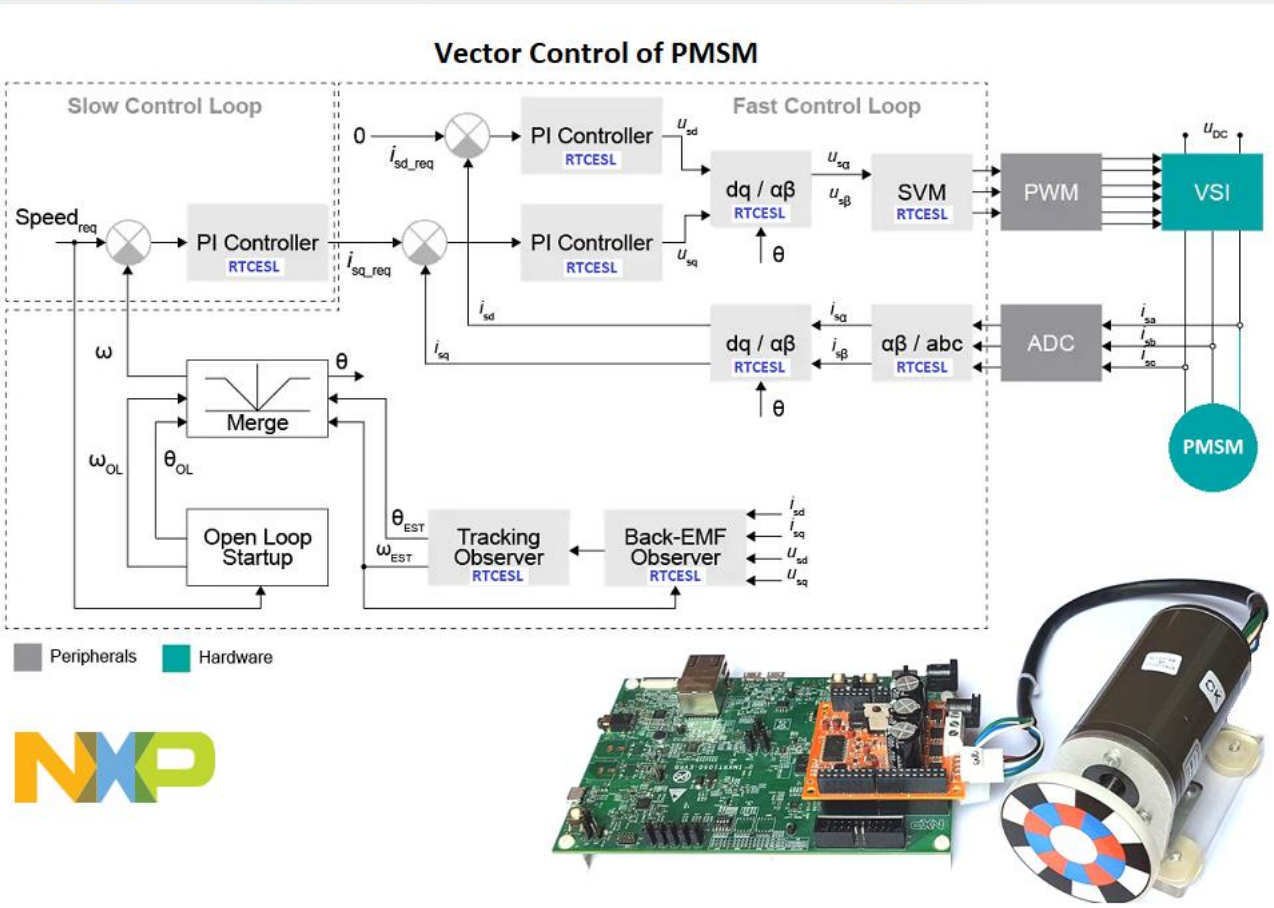
File Edit View Explorer Project Tools Help

Project Tree

- Vector Control of PMSM using MBDT
  - Debug
  - Speed
  - DQ Currents
  - PWM Duty Cycles
  - 3 Phase Currents - high Resolution
  - 3 Phase Currents - low resolution
  - 3 Phase Currents
  - Position

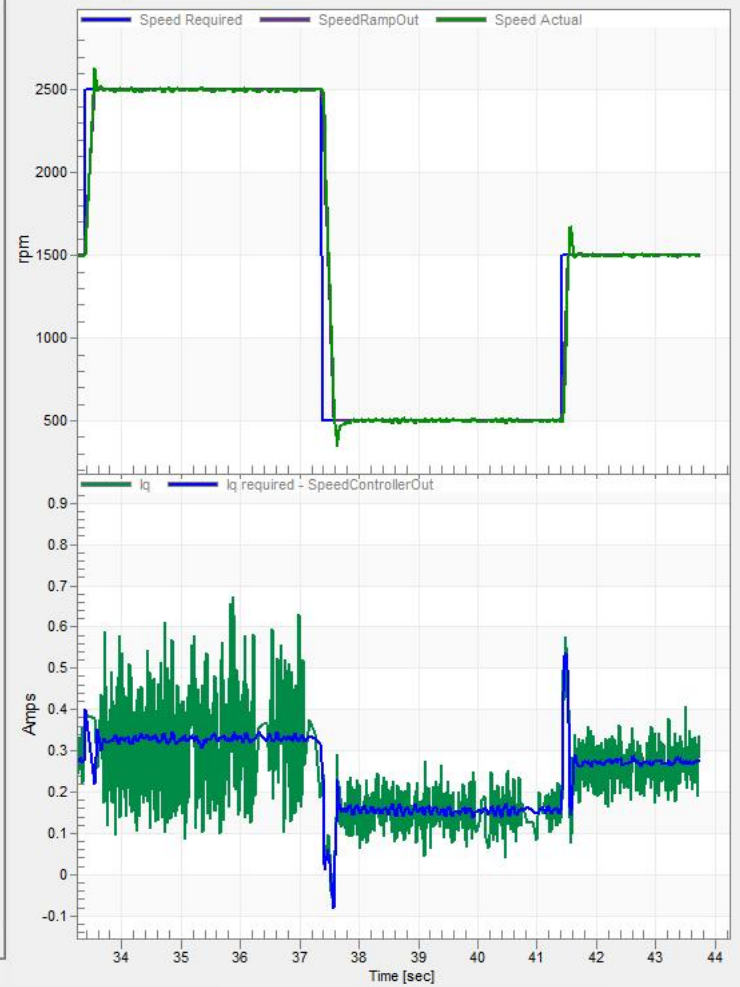
Variable Stimulus

- Speed Simulator [Speed Required]



control page

Oscilloscope - Speed



Variable Watch

Name	Value	Unit	Period
Control Mode	VECTOR CONTROL [4]	ENUM	1000
Vector Control Type	Speed [1]	ENUM	1000
Speed Required	1500	rpm	500
Speed Actual	1501.97	rpm	1000
Uq	0	Volt	100
Scalar Frequency Required	0	Hz	100
Iq Required	0	Amps	1000
Iq	0.265763	Amps	1000
Ud_req	-0.650648	Volts	1000
Uq_req	4.05735	Volts	1000
DCB Voltage	23.9744	Volt	200

Application Com... Variable Stimulus

Done

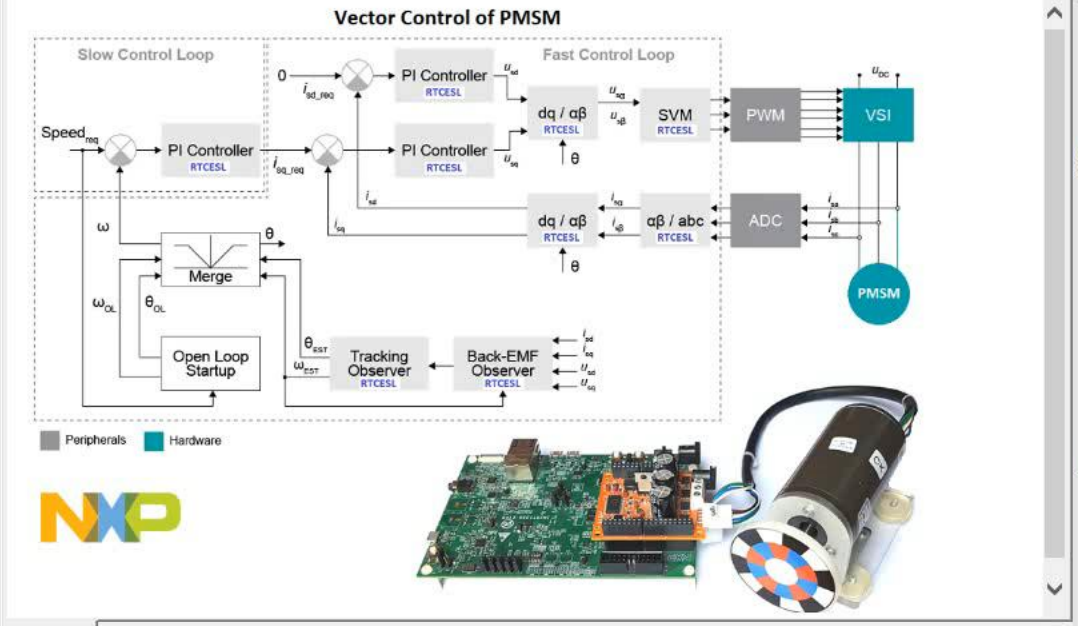
RS232 UART Communication; COM4; speed=115200

mc_pmsm - FreeMASTER

File Edit View Oscilloscope Project Tools Help

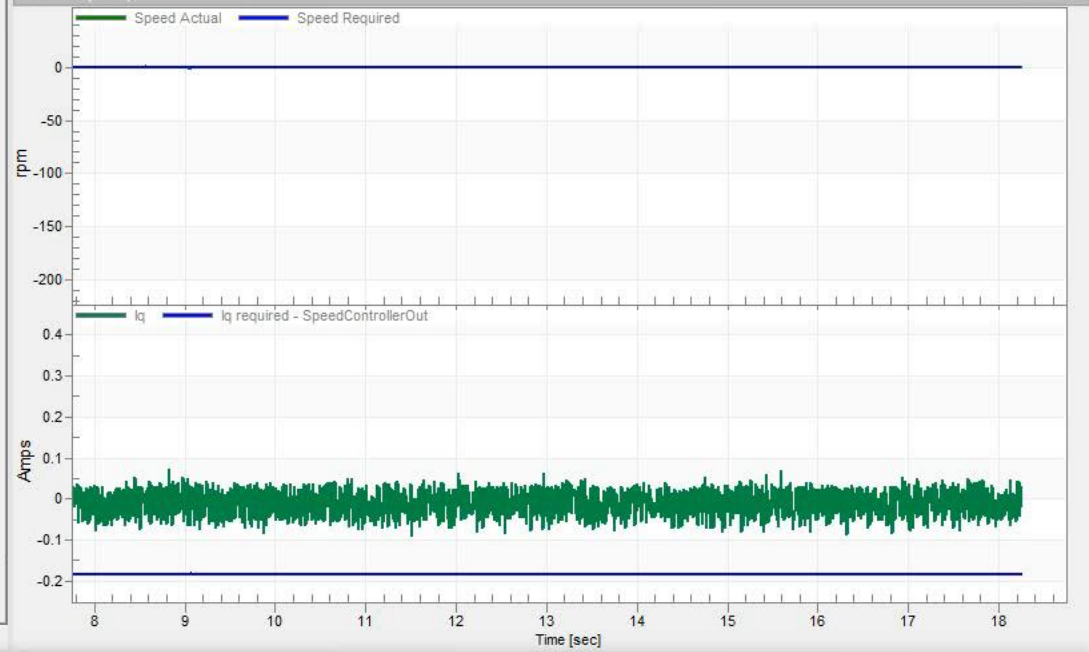
Project Tree

- Vector Control of PMSM using MBDT
  - Debug
  - Speed
  - DQ Currents
  - PWM Duty Cycles
  - 3 Phase Currents - high Resolution
  - 3 Phase Currents - low resolution
  - 3 Phase Currents



control page

Oscilloscope - Speed



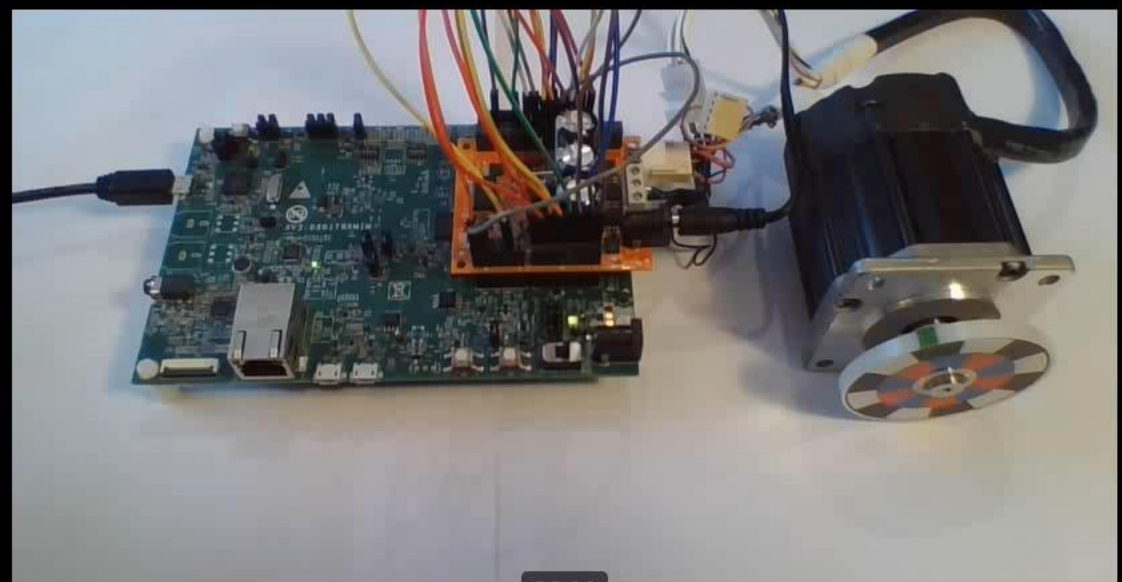
Variable Stimulus

Speed Simulator [Speed Required]

Variable Watch

Name	Value	Unit	
Control Mode	INIT [0]	ENUM	1000
Vector Control Type	Speed [1]	ENUM	1000
Speed Required	0	rpm	500
Speed Actual	-0.0031606	rpm	1000
Uq	0	Volt	100
Scalar Frequency Required	0	Hz	100
Iq Required	0	Amps	1000
Iq	0.0116288	Amps	1000
Ud_req	0.00244426	Volts	1000
Uq_req	0.0330027	Volts	1000
DCB Voltage	25.4301	Volt	200
mc_pmsm_rt1060_P.SpeedPIcontroller1_I	0.1	unit	1000
mc_pmsm_rt1060_P.SpeedPIcontroller1_P	0.01	unit	1000
tryMyRamp_4.fltRampDown	1	unit	1000
tryMyRamp_4.fltRampUp	1	unit	1000
Iq required - SpeedControllerOut	-0.183283	unit	1000

Camera



Application Co... Variable Stimulus

Done

11:35 AM
10/15/2020

workspace - C:\git_repos\mbdt_irinac\IMXRT\src\IMXRT_Examples\imxrt106x\gpio\gpio_polling\evkmimxrt1060_gpio_polling_ert_rtw\ert_main.c - MCUXpresso IDE

File Edit Source Refactor Navigate Search Project ConfigTools Run Analysis Window Help

Project Explorer

- evkmimxrt1062_iled_blinky <Debug>
  - Project Settings
  - Binaries
  - Includes
  - CMSIS
  - board
  - component
  - device
  - drivers
  - evkmimxrt1060
  - source
    - led_blinky.c
    - semihost_hardfault.c
  - startup
  - utilities
  - xip
  - Debug
  - doc
  - evkmimxrt1062_iled_blinky LinkServer Debug (1).launch
  - evkmimxrt1062_iled_blinky LinkServer Debug.launch
  - iled_blinky.mex

Quickstart Panel

MCUXpresso IDE - Quickstart Panel
Project: evkmimxrt1062_iled_blinky [Debug]

Create or import a project
- New project...
- Import SDK example(s)...
- Import project(s) from file system...

Build your project
- Build
- Clean

Debug your project
- Debug
- Terminate, Build and Debug

evkmimxrt1060_gpio_polling.c | ert_main.c

```
1  /*
2   * File: ert_main.c
3   *
4   * Code generated for Simulink model 'evkmimxrt1060_gpio_polling'.
5   *
6   * Model version                  : 1.82
7   * Simulink Coder version         : 9.4 (R2020b) 29-Jul-2020
8   * MBDT for IMXRT Series Version :  Version 1.1.0 (R2019a-R2020b) 12-October-2020
9   * C/C++ source code generated on  : Thu Oct  8 16:44:14 2020
10  *
11  * Target selection: ert.tlc
12  * Embedded hardware selection: ARM Compatible->ARM Cortex
13  * Code generation objective: Execution efficiency
14  * Validation result: All passed
15  */
16
17 #include "evkmimxrt1060_gpio_polling.h"
18 #include "rtwtypes.h"
19
20 volatile int IsrOverrun = 0;
21 static boolean_T OverrunFlag = 0;
22 void rt_OneStep(void)
23 {
24   /* Check for overrun. Protect OverrunFlag against preemption */
25   if (OverrunFlag++) {
26     IsrOverrun = 1;
27     OverrunFlag--;
28     return;
29   }
30
31   evkmimxrt1060_gpio_polling_step();
32
```

Outline | Build Targets

- evkmimxrt1060_gpio_polling.h
- rtwtypes.h
- IsrOverrun : volatile int
- OverrunFlag : boolean_T
- rt_OneStep(void) : void
- stopRequested : volatile boolean_T
- runModel : volatile boolean_T
- main(int, char**) : int

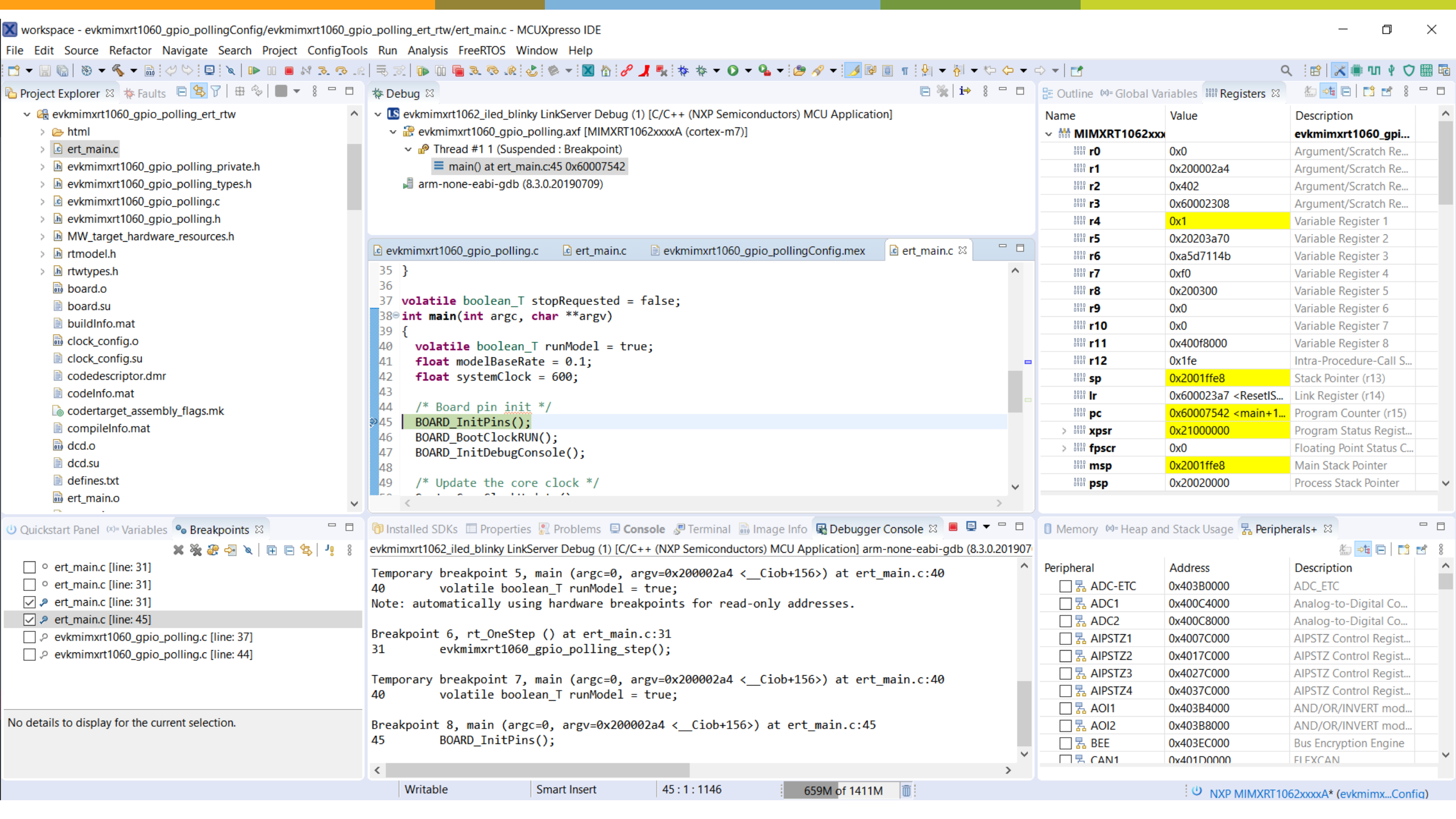
Problems | Tasks | Console | Properties | Image Info | Installed SDKs

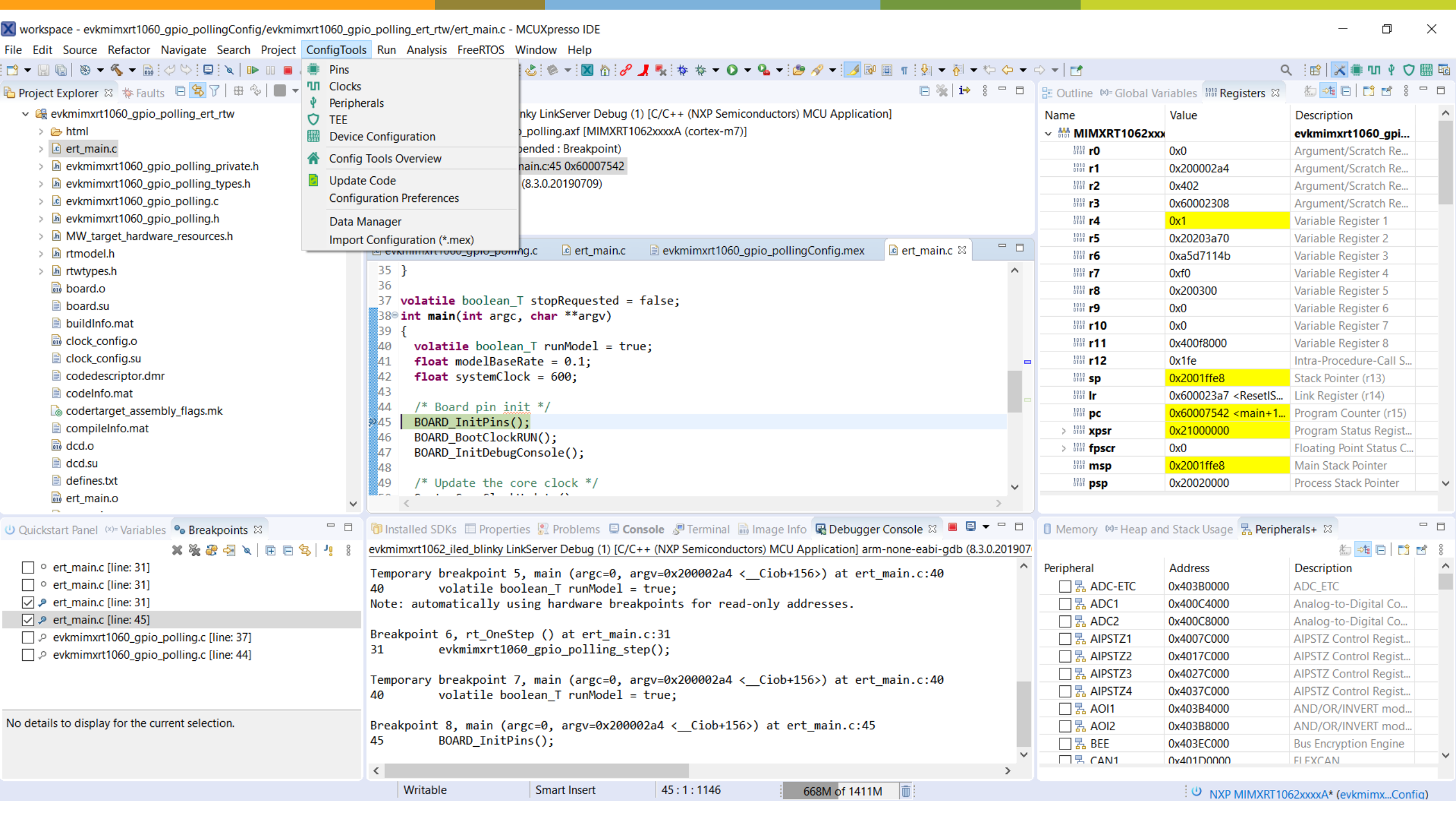
CDT Build Console [evkmimxrt1062_iled_blinky]

```
08:45:20 **** Incremental Build of configuration Debug for project evkmimxrt1062_iled_blinky ****
make -r -j8 all
make: Nothing to be done for 'all'.

08:45:20 Build Finished. 0 errors, 0 warnings. (took 377ms)
```

Writable | Smart Insert | 19 : 1 : 604 | 808M of 1503M | NXP MIMXRT1062xxxxA* (evkmimx... blinky)


workspace - evkmimxrt1060_gpio_pollingConfig/evkmimxrt1060_gpio_polling_ert_rtw/ert_main.c - MCUXpresso IDE
File Edit Source Refactor Navigate Search Project ConfigTools Run Analysis FreeRTOS Window Help
Project Explorer
evkmimxrt1060_gpio_polling_ert_rtw
html
ert_main.c
evkmimxrt1060_gpio_polling_private.h
evkmimxrt1060_gpio_polling_types.h
evkmimxrt1060_gpio_polling.c
evkmimxrt1060_gpio_polling.h
MW_target_hardware_resources.h
rtmodel.h
rtwtypes.h
board.o
board.su
buildInfo.mat
clock_config.o
clock_config.su
codedescriptor.dmr
codeInfo.mat
codertarget_assembly_flags.mk
compileInfo.mat
dcd.o
dcd.su
defines.txt
ert_main.o
Debug
evkmimxrt1062_iled_blinky LinkServer Debug (1) [C/C++ (NXP Semiconductors) MCU Application]
evkmimxrt1060_gpio_polling.axf [MIMXRT1062xxxxA (cortex-m7)]
Thread #1 1 (Suspended : Breakpoint)
main() at ert_main.c:45 0x60007542
arm-none-eabi-gdb (8.3.0.20190709)
Outline
Global Variables
Registers
Name
Value
Description
MIMXRT1062xxx
evkmimxrt1060_gpi...
r0 0x0 Argument/Scratch Re...
r1 0x200002a4 Argument/Scratch Re...
r2 0x402 Argument/Scratch Re...
r3 0x60002308 Argument/Scratch Re...
r4 0x1 Variable Register 1
r5 0x20203a70 Variable Register 2
r6 0xa5d7114b Variable Register 3
r7 0xf0 Variable Register 4
r8 0x200300 Variable Register 5
r9 0x0 Variable Register 6
r10 0x0 Variable Register 7
r11 0x400f8000 Variable Register 8
r12 0x1fe Intra-Procedure-Call S...
sp 0x2001ffe8 Stack Pointer (r13)
lr 0x600023a7 <ResetIS... Link Register (r14)
pc 0x60007542 <main+1... Program Counter (r15)
xpsr 0x21000000 Program Status Regist...
fpscr 0x0 Floating Point Status C...
msp 0x2001ffe8 Main Stack Pointer
psp 0x20020000 Process Stack Pointer
evkmimxrt1060_gpio_polling.c
ert_main.c
evkmimxrt1060_gpio_pollingConfig.mex
ert_main.c
35 }
36
37 volatile boolean_T stopRequested = false;
38 int main(int argc, char **argv)
39 {
40 volatile boolean_T runModel = true;
41 float modelBaseRate = 0.1;
42 float systemClock = 600;
43
44 /* Board pin init */
45 BOARD_InitPins();
46 BOARD_BootClockRUN();
47 BOARD_InitDebugConsole();
48
49 /* Update the core clock */
Quickstart Panel
Variables
Breakpoints
ert_main.c [line: 31]
ert_main.c [line: 31]
ert_main.c [line: 31]
ert_main.c [line: 45]
evkmimxrt1060_gpio_polling.c [line: 37]
evkmimxrt1060_gpio_polling.c [line: 44]
No details to display for the current selection.
Installed SDKs
Properties
Problems
Console
Terminal
Image Info
Debugger Console
evkmimxrt1062_iled_blinky LinkServer Debug (1) [C/C++ (NXP Semiconductors) MCU Application] arm-none-eabi-gdb (8.3.0.201907
Temporary breakpoint 5, main (argc=0, argv=0x200002a4 <__Ciob+156>) at ert_main.c:40
40 volatile boolean_T runModel = true;
Note: automatically using hardware breakpoints for read-only addresses.
Breakpoint 6, rt_OneStep () at ert_main.c:31
31 evkmimxrt1060_gpio_polling_step();
Temporary breakpoint 7, main (argc=0, argv=0x200002a4 <__Ciob+156>) at ert_main.c:40
40 volatile boolean_T runModel = true;
Breakpoint 8, main (argc=0, argv=0x200002a4 <__Ciob+156>) at ert_main.c:45
45 BOARD_InitPins();
Memory
Heap and Stack Usage
Peripherals+
Peripheral
Address
Description
ADC-ETC 0x403B0000 ADC_ETC
ADC1 0x400C4000 Analog-to-Digital Co...
ADC2 0x400C8000 Analog-to-Digital Co...
AIPSTZ1 0x4007C000 AIPSTZ Control Regist...
AIPSTZ2 0x4017C000 AIPSTZ Control Regist...
AIPSTZ3 0x4027C000 AIPSTZ Control Regist...
AIPSTZ4 0x4037C000 AIPSTZ Control Regist...
AOI1 0x403B4000 AND/OR/INVERT mod...
AOI2 0x403B8000 AND/OR/INVERT mod...
BEE 0x403EC000 Bus Encryption Engine
CAN1 0x401D0000 FLEXCAN
Writable
Smart Insert
45 : 1 : 1146
659M of 1411M
NXP MIMXRT1062xxxxA* (evkmimx...Config)


workspace - evkmimxrt1060_gpio_pollingConfig/evkmimxrt1060_gpio_polling_ert_rtw/ert_main.c - MCUXpresso IDE
File Edit Source Refactor Navigate Search Project ConfigTools Run Analysis FreeRTOS Window Help
Pins
Clocks
Peripherals
TEE
Device Configuration
Config Tools Overview
Update Code
Configuration Preferences
Data Manager
Import Configuration (*.mex)
Project Explorer
Faults
evkmimxrt1060_gpio_polling_ert_rtw
html
ert_main.c
evkmimxrt1060_gpio_polling_private.h
evkmimxrt1060_gpio_polling_types.h
evkmimxrt1060_gpio_polling.c
evkmimxrt1060_gpio_polling.h
MW_target_hardware_resources.h
rtmodel.h
rtwtypes.h
board.o
board.su
buildInfo.mat
clock_config.o
clock_config.su
codedescriptor.dmr
codeInfo.mat
codertarget_assembly_flags.mk
compileInfo.mat
dcd.o
dcd.su
defines.txt
ert_main.o
nky LinkServer Debug (1) [C/C++ (NXP Semiconductors) MCU Application]
_polling.axf [MIMXRT1062xxxxA (cortex-m7)]
pended : Breakpoint)
ain.c:45 0x60007542
(8.3.0.20190709)
ert_main.c
evkmimxrt1060_gpio_pollingConfig.mex
ert_main.c
35 }
36
37 volatile boolean_T stopRequested = false;
38 int main(int argc, char **argv)
39 {
40 volatile boolean_T runModel = true;
41 float modelBaseRate = 0.1;
42 float systemClock = 600;
43
44 /* Board pin init */
45 BOARD_InitPins();
46 BOARD_BootClockRUN();
47 BOARD_InitDebugConsole();
48
49 /* Update the core clock */
Outline
Global Variables
Registers
Name
Value
Description
MIMXRT1062xxx
evkmimxrt1060_gpi...
r0 0x0 Argument/Scratch Re...
r1 0x200002a4 Argument/Scratch Re...
r2 0x402 Argument/Scratch Re...
r3 0x60002308 Argument/Scratch Re...
r4 0x1 Variable Register 1
r5 0x20203a70 Variable Register 2
r6 0xa5d7114b Variable Register 3
r7 0xf0 Variable Register 4
r8 0x200300 Variable Register 5
r9 0x0 Variable Register 6
r10 0x0 Variable Register 7
r11 0x400f8000 Variable Register 8
r12 0x1fe Intra-Procedure-Call S...
sp 0x2001ffe8 Stack Pointer (r13)
lr 0x600023a7 <ResetIS... Link Register (r14)
pc 0x60007542 <main+1... Program Counter (r15)
xpsr 0x21000000 Program Status Regist...
fpscr 0x0 Floating Point Status C...
msp 0x2001ffe8 Main Stack Pointer
psp 0x20020000 Process Stack Pointer
Quickstart Panel
Variables
Breakpoints
ert_main.c [line: 31]
ert_main.c [line: 31]
ert_main.c [line: 31]
ert_main.c [line: 45]
evkmimxrt1060_gpio_polling.c [line: 37]
evkmimxrt1060_gpio_polling.c [line: 44]
No details to display for the current selection.
Installed SDKs
Properties
Problems
Console
Terminal
Image Info
Debugger Console
evkmimxrt1062_iled_blinky LinkServer Debug (1) [C/C++ (NXP Semiconductors) MCU Application] arm-none-eabi-gdb (8.3.0.201907
Temporary breakpoint 5, main (argc=0, argv=0x200002a4 <__Ciob+156>) at ert_main.c:40
40 volatile boolean_T runModel = true;
Note: automatically using hardware breakpoints for read-only addresses.
Breakpoint 6, rt_OneStep () at ert_main.c:31
31 evkmimxrt1060_gpio_polling_step();
Temporary breakpoint 7, main (argc=0, argv=0x200002a4 <__Ciob+156>) at ert_main.c:40
40 volatile boolean_T runModel = true;
Breakpoint 8, main (argc=0, argv=0x200002a4 <__Ciob+156>) at ert_main.c:45
45 BOARD_InitPins();
Memory
Heap and Stack Usage
Peripherals+
Peripheral
Address
Description
ADC-ETC 0x403B0000 ADC_ETC
ADC1 0x400C4000 Analog-to-Digital Co...
ADC2 0x400C8000 Analog-to-Digital Co...
AIPSTZ1 0x4007C000 AIPSTZ Control Regist...
AIPSTZ2 0x4017C000 AIPSTZ Control Regist...
AIPSTZ3 0x4027C000 AIPSTZ Control Regist...
AIPSTZ4 0x4037C000 AIPSTZ Control Regist...
AOI1 0x403B4000 AND/OR/INVERT mod...
AOI2 0x403B8000 AND/OR/INVERT mod...
BEE 0x403EC000 Bus Encryption Engine
CAN1 0x401D0000 FLEXCAN
Writable
Smart Insert
45 : 1 : 1146
668M of 1411M
NXP MIMXRT1062xxxxA* (evkmimx...Config)

workspace - evkmimxrt1060_gpio_pollingConfig/evkmimxrt1060_gpio_pollingConfig.mex - MCUXpresso IDE

File Edit Navigate Search Project ConfigTools Pins Run Window Help

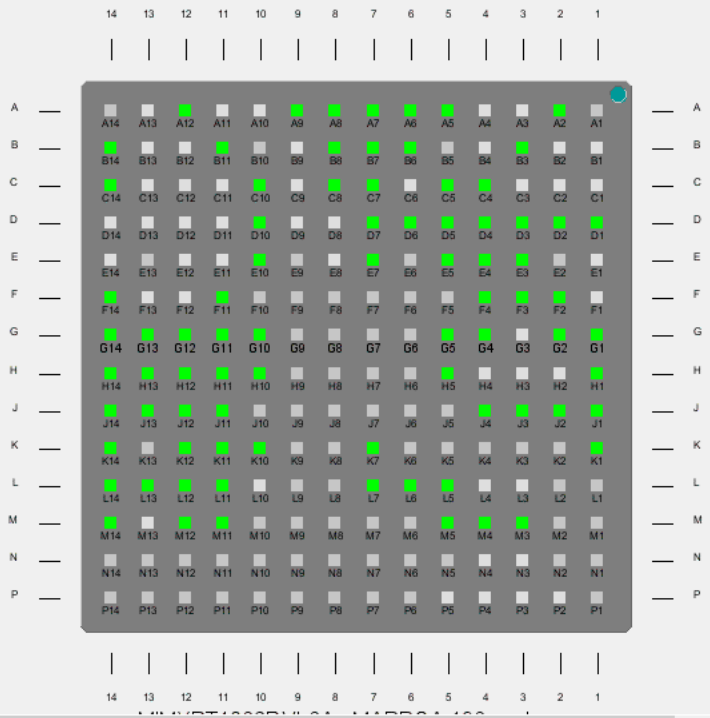
evkmimxrt1060_gpio_pollingConf | Update Code | Functional Group | BOARD_InitPins

Pins | Peripheral Signals | Power Groups

type filter text

Pin	Pin name	Label	Identifier	Arduino...	GPIO	FLEXIO	LPUART	PWM
A1	VSS0	GND						
B1	GPIO_EMC_15	SEMC_A6	SEMC_A6		GPIO4...	XBAR1_...	XBAR1...	XBAR1_X
C1	GPIO_EMC_21	SEMC_BA0	SEMC_BA0		GPIO4...			FLEXPWM
D1	GPIO_EMC_28	SEMC_WE	SEMC_WE		GPIO4...	FLEXIO...	LPUAR...	FLEXPWM
E1	GPIO_EMC_29	SEMC_CS0	SEMC_CS0		GPIO4...	FLEXIO...	LPUAR...	FLEXPWM
F1	GPIO_EMC_22	SEMC_BA1	SEMC_BA1		GPIO4...			FLEXPWM
G1	GPIO_EMC_10	SEMC_A1	SEMC_A1		GPIO4...	FLEXIO...		FLEXPWM
H1	GPIO_EMC_12	SEMC_A3	SEMC_A3		GPIO4...	XBAR1_...	XBAR1...	XBAR1_X
J1	GPIO_SD_B0_...	SD1_D0/J24[...	SD1_D0	J24[4] (...	GPIO3...	XBAR1_...	LPUAR...	FLEXPWM
K1	GPIO_SD_B0_...	SD1_D1/J24[...	SD1_D1	J24[5] (...	GPIO3...	XBAR1_...	LPUAR...	FLEXPWM
L1	DCDC_IN0	MCU_DCDC_I...						
M1	DCDC_LP0	VDD_SOC_IN						
N1	DCDC_GND0	GND						
P1	VSS1	GND						
A2	GPIO_EMC_27	SEMC_CKE	SEMC_CKE		GPIO4...	FLEXIO...	LPUAR...	FLEXPWM
B2	GPIO_EMC_18	SEMC_A9	SEMC_A9		GPIO4...		LPUAR...	FLEXPWM
C2	GPIO_EMC_09	SEMC_A0	SEMC_A0		GPIO4...	FLEXIO...		FLEXPWM
D2	GPIO_EMC_25	SEMC_RAS	SEMC_RAS		GPIO4...		LPUAR...	FLEXPWM
E2	VSS2	GND						
F2	GPIO_EMC_04	SEMC_D4	SEMC_D4		GPIO4...	XBAR1_...	XBAR1...	FLEXPWM
G2	GPIO_EMC_23	SEMC_A10	SEMC_A10		GPIO4...		LPUAR...	FLEXPWM

Package [Pins Bottom]



Overview | Code Preview

pin_mux.c | pin_mux.h

```
IOMUXC_SetPinMux(
    IOMUXC_GPIO_EMC_02_XBAR1_INOUT04,        /* Gl
    0U);                                     /* Se
IOMUXC_SetPinMux(
    IOMUXC_GPIO_EMC_03_XBAR1_INOUT05,        /* Gl
    0U);                                     /* Se
IOMUXC_SetPinMux(
    IOMUXC_GPIO_EMC_04_XBAR1_INOUT06,        /* Gl
    0U);                                     /* Se
IOMUXC_SetPinMux(
    IOMUXC_GPIO_EMC_05_XBAR1_INOUT07,        /* Gl
    0U);                                     /* Se
IOMUXC_SetPinMux(
    IOMUXC_GPIO_EMC_06_XBAR1_INOUT08,        /* Gl
    0U);                                     /* Se
IOMUXC_SetPinMux(
    IOMUXC_GPIO_EMC_10_FLEXCAN2_RX,          /* Gl
    0U);                                     /* Se
IOMUXC_SetPinMux(
    IOMUXC_GPIO_EMC_12_XBAR1_IN24,           /* Gl
    0U);                                     /* Se
IOMUXC_SetPinMux(
```

Registers

all | Show modified registers only

type filter text

Reg. Name	Set Value	Reset Value	Value Description
CCM_CCGR2	0xffffffff	0xfc3fffff	
GPIO1_GDIR	0xf0000200	0x00000000	
GPIO3_GDIR	0x0000000f	0x00000000	
IOMUXC_FLEXPWM	0x00000003	0x00000000	
IOMUXC_FLEXPWM	0x00000001	0x00000000	
IOMUXC_GPR_GPR	0xcdfb0004	0x00000000	
IOMUXC_GPT2_IPP	0x00000001	0x00000000	

Routed Pins

type filter text

Routed Pins for BOARD_InitP... 105

#	Peripheral	Signal	Route to	Label	Identifier	Power group	Direction	GPIO initial state	GPIO interrupt	Software Input On	Hysteresis enat
L6	GPIO5	gpio_...	WAKEUP	USER_BTN	Not Specified	VDD_SNVS_IN (0V)	Not Specified	n/a	n/a	Disabled	Enable
A..	PWM1	B, 3	GPIO_EMC_13	SEMC_A4	SEMC_A4	NVCC_EMC (0V)	Not Specified	n/a	n/a	Disabled	Disable
H.	ADC1	IN, 3	GPIO_AD_B0_14	CAN2_TX/U12[1]	Not Specified	NVCC_GPIO (0V)	Input	n/a	n/a	Disabled	Disable
A..	CAN2	TX	GPIO_B1_08	ENET_TXD1	ENET_TXD1	NVCC_GPIO (0V)	Output	n/a	n/a	Disabled	Disable

evkmimxrt1060_gpio_pollingConfig | 689M of 1343M | NXP MIMXRT1062xxxxA* (evkmimx...Config)

workspace - evkmimxrt1060_gpio_pollingConfig/evkmimxrt1060_gpio_pollingConfig.mex - MCUXpresso IDE

File Edit Navigate Search Project ConfigTools Pins Run Window Help

evkmimxrt1060_gpio_pollingConf | Update Code | Functional Group | BOARD_InitPins

Pins | Peripheral Signals | Power Groups

type filter text

- ADC1
  - IN, 0 » [J13] GPIO_AD_B1_11
  - IN, 1 » [K14] GPIO_AD_B0_12
  - IN, 2 » [L14] GPIO_AD_B0_13
  - IN, 3 » [H14] GPIO_AD_B0_14
  - IN, 4 » [L10] GPIO_AD_B
  - IN, 5 » [J11] GPIO_AD_B
  - IN, 6 » [K11] GPIO_AD_B
  - IN, 7 » [L11] GPIO_AD_B
  - IN, 8 » [M12] GPIO_AD_B
  - IN, 9 » [L12] GPIO_AD_B
  - IN, 10 » [K12] GPIO_AD_
  - IN, 11 » [J12] GPIO_AD_B
  - IN, 12 » [K10] GPIO_AD_
  - IN, 13 » [H13] GPIO_AD_
  - IN, 14 » [M13] GPIO_AD_
  - IN, 15 » [L13] GPIO_AD_B
- ADC2
- ADC_ETC
- AOI1
- AOI2
- ARM
- CAN1
- CAN2

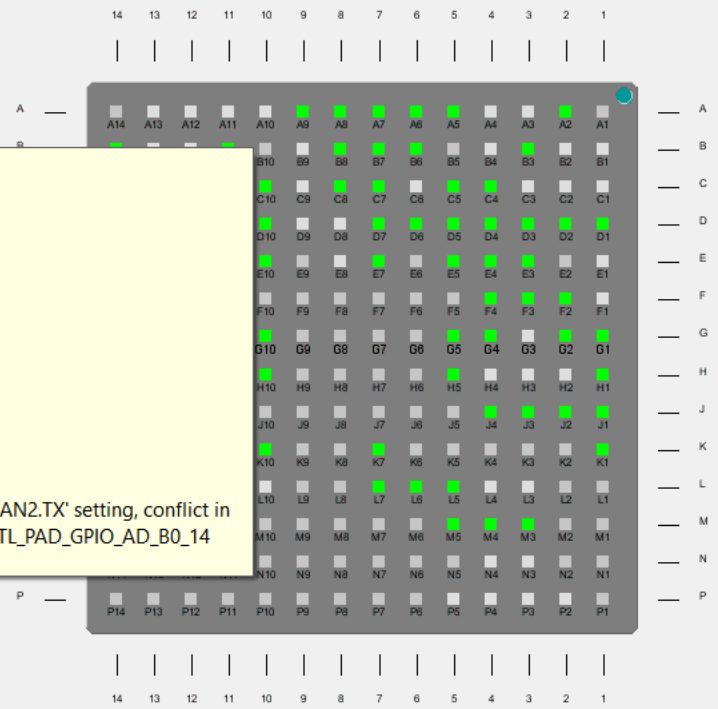
Signal IN, 3
ADC input channel 3; Analog; Input

Routed by default pins / signal routes:
[H14] GPIO_AD_B0_14

Signal is routed to pins:
[H14] GPIO_AD_B0_14
Signal is routed in functions:
BOARD_InitPins

ERRORS:
#H14-ADC1.IN.3 setting in BOARD_InitPins:
– Selected value is in conflict with 'Route to' value in '#H14-CAN2.TX' setting, conflict in configuration of MUX_MODE bit-field of IOMUXC_SW_MUX_CTL_PAD_GPIO_AD_B0_14 register.

Package [Pins Bottom]



MIMXRT1062DVL6A - MAPBGA 196 package

Overview | Code Preview

pin_mux.c | pin_mux.h

```
319      .direction = kGPIO_DigitalInput,
320      .outputLogic = 0U,
321      .interruptMode = kGPIO_NoIntmode
322  };
323  /* Initialize GPIO functionality on GPIO_EMC_34
324  GPIO_PinInit(GPIO3, 20U, &GPIO3_20_config);
325
326  /* GPIO configuration of GPIO3_23 on GPIO_EMC_37
327  gpio_pin_config_t GPIO3_23_config = {
328      .direction = kGPIO_DigitalInput,
329      .outputLogic = 0U,
330      .interruptMode = kGPIO_NoIntmode
331  };
332  /* Initialize GPIO functionality on GPIO_EMC_37
333  GPIO_PinInit(GPIO3, 23U, &GPIO3_23_config);
334
335  /* GPIO configuration of GPIO3_24 on GPIO_EMC_38
336  gpio_pin_config_t GPIO3_24_config = {
337      .direction = kGPIO_DigitalInput,
338      .outputLogic = 0U,
```

Source code generated with warning(s)

Registers

all | Show modified registers only

type filter text

Reg. Name	Set Value	Reset Value	Value Description
CCM_CCGR2	0xffffffff	0xfc3fffff	
GPIO1_GDIR	0xf0000200	0x00000000	
GPIO3_GDIR	0x0000000f	0x00000000	
IOMUXC_FLEXPWM	0x00000003	0x00000000	
IOMUXC_FLEXPWM	0x00000001	0x00000000	
IOMUXC_GPR_GPR	0xcdfb0004	0x00000000	
IOMUXC_GPT2_IPP	0x00000001	0x00000000	

Routed Pins

type filter text

Routed Pins for BOARD_InitP... 105

#	Peripheral	Signal	Route to	Label	Identifier	Power group	Direction	GPIO initial state	GPIO interrupt	Software Input On	Hysteresis enat
E..	FLEXIO1	IO, 00	GPIO_EMC_00	SEMC_D0	SEMC_D0	NVCC_EMC (0V)	Not Specified	n/a	n/a	Disabled	Disable
L...	LPUART1	RX	GPIO_AD_B0_13	UART1_RXD	UART1_RXD	NVCC_GPIO (0V)	Input	n/a	n/a	Disabled	Disable
J...	ADC1	IN, 0	GPIO_AD_B1_11	SAI1_RX_BCLK/CSI_D6/J...	CSI_D6	NVCC_GPIO (0V)	Input	n/a	n/a	Disabled	Disable
H.	ADC1	IN, 3	GPIO_AD_B0_14	CAN2_TX/U12[1]	Not Specified	NVCC_GPIO (0V)	Input	n/a	n/a	Disabled	Disable

ERRORS: evkmimxrt1060_gpio_pollingConfig: There are errors in the configuration, generated source code might not be complete.

931M of 1386M

NXP MIMXRT1062xxxxA* (evkmimx...Config)

workspace - evkmimxrt1060_gpio_pollingConfig/evkmimxrt1060_gpio_pollingConfig.mex - MCUXpresso IDE

File Edit Navigate Search Project ConfigTools Pins Run Window Help

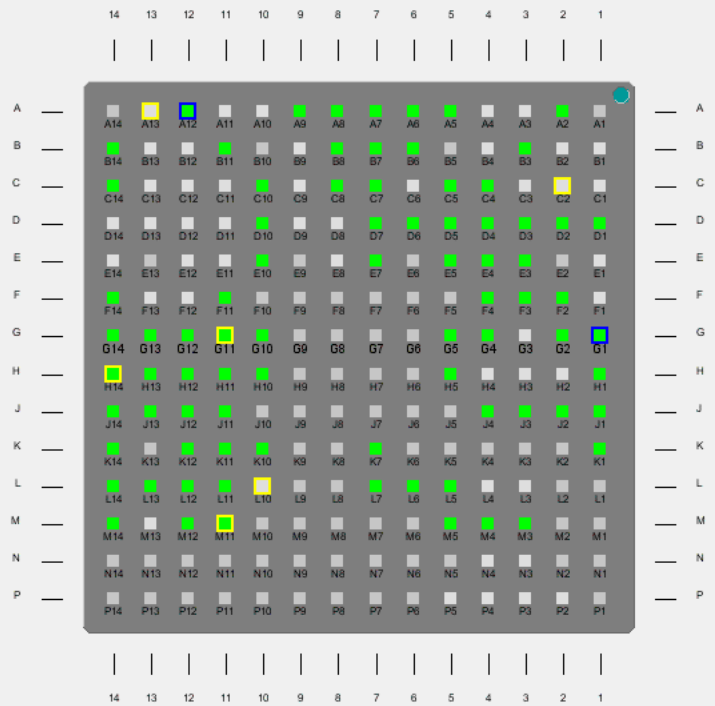
evkmimxrt1060_gpio_pollingConf | Update Code | Functional Group | BOARD_InitPins

Pins | Peripheral Signals | Power Groups

type filter text

- ADC1
  - IN, 0 » [J13] GPIO_AD_B1_11
  - IN, 1 » [K14] GPIO_AD_B0_12
  - IN, 2 » [L14] GPIO_AD_B0_13
  - IN, 3 » [H14] GPIO_AD_B0_14
  - IN, 4 » [L10] GPIO_AD_B0_15
  - IN, 5 » [J11] GPIO_AD_B1_00
  - IN, 6 » [K11] GPIO_AD_B1_01
  - IN, 7 » [L11] GPIO_AD_B1_02
  - IN, 8 » [M12] GPIO_AD_B1_03
  - IN, 9 » [L12] GPIO_AD_B1_04
  - IN, 10 » [K12] GPIO_AD_B1_05
  - IN, 11 » [J12] GPIO_AD_B1_06
  - IN, 12 » [K10] GPIO_AD_B1_07
  - IN, 13 » [H13] GPIO_AD_B1_08
  - IN, 14 » [M13] GPIO_AD_B1_09
  - IN, 15 » [L13] GPIO_AD_B1_10
- ADC2
- ADC_ETC
- AOI1
- AOI2
- ARM
- CAN1
- CAN2

Package [Pins Bottom]



MIMXRT1062DVL6A - MAPBGA 196 package

Overview | Code Preview

pin_mux.c | pin_mux.h

```
498     IOMUXC_GPIO_EMC_02_XBAR1_INOUT04,        /* GI
499     0U);                                     /* SI
500 IOMUXC_SetPinMux(
501     IOMUXC_GPIO_EMC_03_XBAR1_INOUT05,        /* GI
502     0U);                                     /* SI
503 IOMUXC_SetPinMux(
504     IOMUXC_GPIO_EMC_04_XBAR1_INOUT06,        /* GI
505     0U);                                     /* SI
506 IOMUXC_SetPinMux(
507     IOMUXC_GPIO_EMC_05_XBAR1_INOUT07,        /* GI
508     0U);                                     /* SI
509 IOMUXC_SetPinMux(
510     IOMUXC_GPIO_EMC_06_XBAR1_INOUT08,        /* GI
511     0U);                                     /* SI
512 IOMUXC_SetPinMux(
513     IOMUXC_GPIO_EMC_10_FLEXCAN2_RX,          /* GI
514     0U);                                     /* SI
515 IOMUXC_SetPinMux(
516     IOMUXC_GPIO_EMC_12_XBAR1_IN24,           /* GI
517     0U);                                     /* SI
518 IOMUXC_SetPinMux(
```

Registers

all | Show modified registers only

type filter text

Reg. Name	Set Value	Reset Value	Value Description
CCM_CCGR2	0xffffffff	0xfc3fffff	
GPIO1_GDIR	0xf0000200	0x00000000	
GPIO3_GDIR	0x0000000f	0x00000000	
IOMUXC_FLEXPWM	0x00000003	0x00000000	
IOMUXC_FLEXPWM	0x00000001	0x00000000	
IOMUXC_GPR_GPR	0xcdfb0004	0x00000000	
IOMUXC_GPT2_IPP	0x00000001	0x00000000	

Routed Pins

type filter text

Routed Pins for BOARD_InitP... 105

#	Peripheral	Signal	Route to	Label	Identifier	Power group	Direction	GPIO initial state	GPIO interrupt	Software Input On	Hysteresis enat
L6	GPIO5	gpio_...	WAKEUP	USER_BTN	Not Specified	VDD_SNVS_IN (0V)	Not Specified	n/a	n/a	Disabled	Enable
A..	PWM1	B, 3	GPIO_EMC_13	SEMC_A4	SEMC_A4	NVCC_EMC (0V)	Not Specified	n/a	n/a	Disabled	Disable
H.	ADC1	IN, 3	GPIO_AD_B0_14	CAN2_TX/U12[1]	Not Specified	NVCC_GPIO (0V)	Input	n/a	n/a	Disabled	Disable
A..	CAN2	TX	GPIO_B1_08	ENET_TXD1	ENET_TXD1	NVCC_GPIO (0V)	Output	n/a	n/a	Disabled	Disable

evkmimxrt1060_gpio_pollingConfig

852M of 1379M

NXP MIMXRT1062xxxxA* (evkmimx...Config)

workspace - evkmimxrt1060_gpio_pollingConfig/evkmimxrt1060_gpio_pollingConfig.mex - MCUXpresso IDE

File Edit Navigate Search Project ConfigTools Pins Run Window Help

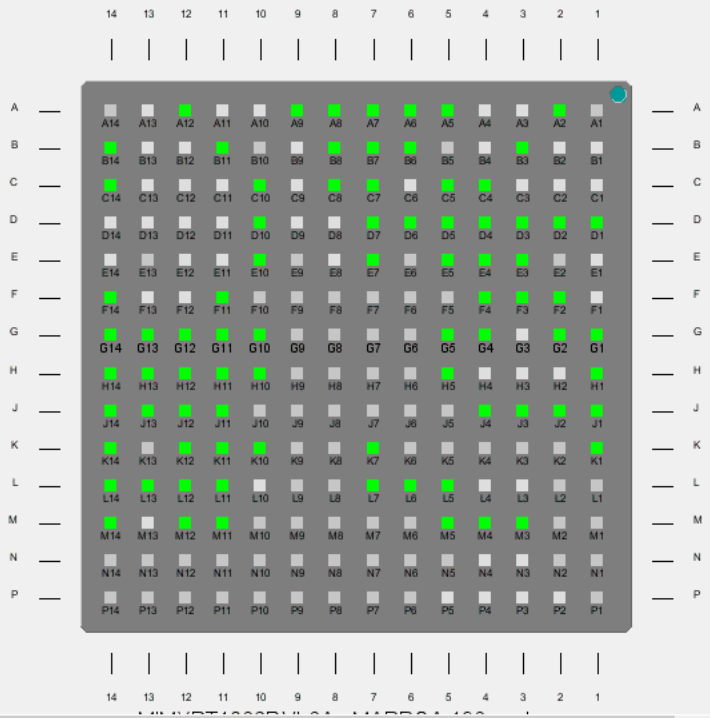
evkmimxrt1060_gpio_pollingConf | Update Code | Functional Group | BOARD_InitPins

Pins | Peripheral Signals | Power Groups

type filter text

Pin	Pin name	Label	Identifier	Arduino...	GPIO	FLEXIO	LPUART	PWM
A1	VSS0	GND						
B1	GPIO_EMC_15	SEMC_A6	SEMC_A6		GPIO4...	XBAR1_...	XBAR1...	XBAR1_X
C1	GPIO_EMC_21	SEMC_BA0	SEMC_BA0		GPIO4...			FLEXPWM
D1	GPIO_EMC_28	SEMC_WE	SEMC_WE		GPIO4...	FLEXIO...	LPUAR...	FLEXPWM
E1	GPIO_EMC_29	SEMC_CS0	SEMC_CS0		GPIO4...	FLEXIO...	LPUAR...	FLEXPWM
F1	GPIO_EMC_22	SEMC_BA1	SEMC_BA1		GPIO4...			FLEXPWM
G1	GPIO_EMC_10	SEMC_A1	SEMC_A1		GPIO4...	FLEXIO...		FLEXPWM
H1	GPIO_EMC_12	SEMC_A3	SEMC_A3		GPIO4...	XBAR1_...	XBAR1...	XBAR1_X
J1	GPIO_SD_B0_...	SD1_D0/J24[...	SD1_D0	J24[4] (...	GPIO3...	XBAR1_...	LPUAR...	FLEXPWM
K1	GPIO_SD_B0_...	SD1_D1/J24[...	SD1_D1	J24[5] (...	GPIO3...	XBAR1_...	LPUAR...	FLEXPWM
L1	DCDC_IN0	MCU_DCDC_I...						
M1	DCDC_LP0	VDD_SOC_IN						
N1	DCDC_GND0	GND						
P1	VSS1	GND						
A2	GPIO_EMC_27	SEMC_CKE	SEMC_CKE		GPIO4...	FLEXIO...	LPUAR...	FLEXPWM
B2	GPIO_EMC_18	SEMC_A9	SEMC_A9		GPIO4...		LPUAR...	FLEXPWM
C2	GPIO_EMC_09	SEMC_A0	SEMC_A0		GPIO4...	FLEXIO...		FLEXPWM
D2	GPIO_EMC_25	SEMC_RAS	SEMC_RAS		GPIO4...		LPUAR...	FLEXPWM
E2	VSS2	GND						
F2	GPIO_EMC_04	SEMC_D4	SEMC_D4		GPIO4...	XBAR1_...	XBAR1...	FLEXPWM
G2	GPIO_EMC_23	SEMC_A10	SEMC_A10		GPIO4...		LPUAR...	FLEXPWM

Package [Pins Bottom]



Overview | Code Preview

pin_mux.c | pin_mux.h

```
IOMUXC_SetPinMux(
    IOMUXC_GPIO_EMC_02_XBAR1_INOUT04,        /* Gl
    0U);                                     /* Se
IOMUXC_SetPinMux(
    IOMUXC_GPIO_EMC_03_XBAR1_INOUT05,        /* Gl
    0U);                                     /* Se
IOMUXC_SetPinMux(
    IOMUXC_GPIO_EMC_04_XBAR1_INOUT06,        /* Gl
    0U);                                     /* Se
IOMUXC_SetPinMux(
    IOMUXC_GPIO_EMC_05_XBAR1_INOUT07,        /* Gl
    0U);                                     /* Se
IOMUXC_SetPinMux(
    IOMUXC_GPIO_EMC_06_XBAR1_INOUT08,        /* Gl
    0U);                                     /* Se
IOMUXC_SetPinMux(
    IOMUXC_GPIO_EMC_10_FLEXCAN2_RX,          /* Gl
    0U);                                     /* Se
IOMUXC_SetPinMux(
    IOMUXC_GPIO_EMC_12_XBAR1_IN24,           /* Gl
    0U);                                     /* Se
IOMUXC_SetPinMux(
```

Registers

all | Show modified registers only

type filter text

Reg. Name	Set Value	Reset Value	Value Description
CCM_CCGR2	0xffffffff	0xfc3fffff	
GPIO1_GDIR	0xf0000200	0x00000000	
GPIO3_GDIR	0x0000000f	0x00000000	
IOMUXC_FLEXPWM	0x00000003	0x00000000	
IOMUXC_FLEXPWM	0x00000001	0x00000000	
IOMUXC_GPR_GPR	0xcdfb0004	0x00000000	
IOMUXC_GPT2_IPP	0x00000001	0x00000000	

Routed Pins

type filter text

Routed Pins for BOARD_InitP... 105

#	Peripheral	Signal	Route to	Label	Identifier	Power group	Direction	GPIO initial state	GPIO interrupt	Software Input On	Hysteresis enat
L6	GPIO5	gpio_...	WAKEUP	USER_BTN	Not Specified	VDD_SNVS_IN (0V)	Not Specified	n/a	n/a	Disabled	Enable
A..	PWM1	B, 3	GPIO_EMC_13	SEMC_A4	SEMC_A4	NVCC_EMC (0V)	Not Specified	n/a	n/a	Disabled	Disable
H.	ADC1	IN, 3	GPIO_AD_B0_14	CAN2_TX/U12[1]	Not Specified	NVCC_GPIO (0V)	Input	n/a	n/a	Disabled	Disable
A..	CAN2	TX	GPIO_B1_08	ENET_TXD1	ENET_TXD1	NVCC_GPIO (0V)	Output	n/a	n/a	Disabled	Disable

evkmimxrt1060_gpio_pollingConfig | 689M of 1343M | NXP MIMXRT1062xxxxA* (evkmimx...Config)

workspace - evkmimxrt1060_gpio_pollingConfig/evkmimxrt1060_gpio_pollingConfig.mex - MCUXpresso IDE

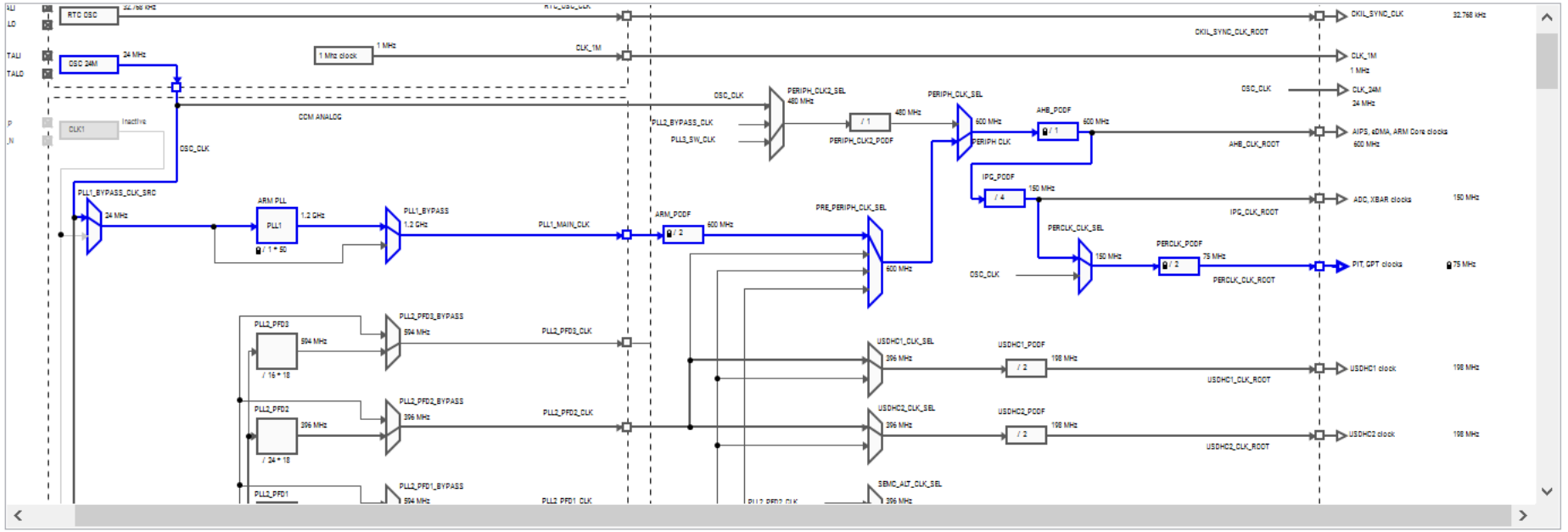
File Edit Navigate Search Project ConfigTools Clocks Run Window Help

evkmimxrt1060_gpio_pollingConf | Update Code | Functional Group | BOARD_BootClockRUN

Clocks Diagram

PERCLK_CLK_ROOT

Run Mode RUN | On-chip oscillator 24MHz Enabled



Clocks Table

Run Mode RUN | On-chip oscillator 24MHz Enabled

Clock Sources

Name	C..	Value
RTC OSC mode		External crystal 32kHz
24MHz clock source	☑	**24 MHz**
Power down mode		Disabled
OSC mode		External crystal 24 MHz
RC oscillator		Enabled
OSC ready ...nter value		128
CLK1 external clock sourc	☐	Inactive
CLK1 pins mode		Disabled
SAI1 MCLK	☐	Inactive

Clock Outputs

Name	L...	Value	A...y
GPT1 high frequency cloc		75 MHz	
GPT2 high frequency cloc		75 MHz	
LCDIF_CLK_ROOT		67.5 MHz	
LPI2C_CLK_ROOT		60 MHz	
LPSPI_CLK_ROOT		105.6 MHz	
LVDS1_CLK		1.2 GHz	
MQS MCLK		63.52... MHz	
PERCLK_CLK_ROOT	🔒	**75 MHz**	±0.1%
SAI1 MCLK 1		63.52... MHz	

Overview | Details | Clock Consumers

Path Details: PERCLK_CLK_ROOT

Name	C..	L...	Value
IPG divider			/ 4
IPG divider Frequency			150 MHz
PERCLK clock selector			IPG root clock
PERCLK clock divider		🔒	/ 2
PERCLK cloc...r Frequency			75 MHz
PERCLK_CLK_...T Frequency			75 MHz
PERCLK_CLK_ROOT		🔒	75 MHz

Code Preview

clock_config.h | clock_config.c

```
155     };
156 /*******************************************************
157  * Code for BOARD_BootClockRUN configuration
158  *******************************************************
159 void BOARD_BootClockRUN(void)
160 {
161     /* Init RTC OSC clock frequency. */
162     CLOCK_SetRtcXtalFreq(32768U);
163     /* Enable 1MHz clock output. */
164     XTALOSC24M->OSC_CONFIG2 |= XTALOSC24M_OSC_CONFI
```

Code successfully generated.

Registers

all | ☑ Show modified registers only

type filter text

Reg. Name	Set Value	Reset Value	Value Description
CCM_ANALOG_PLL	0x00000032	0x2964619c	
CCM_ANALOG_PLL	0x00000001	0x05f5e100	
CCM_ANALOG_PLL	0x00313001	0x00011001	
CCM_ANALOG_PLL	0x00002001	0x00013001	

evkmimxrt1060_gpio_pollingConfig | 990M of 1252M | NXP MIMXRT1062xxxxA* (evkmimx...Config)

workspace - evkmimxrt1060_gpio_pollingConfig/evkmimxrt1060_gpio_pollingConfig.mex - MCUXpresso IDE

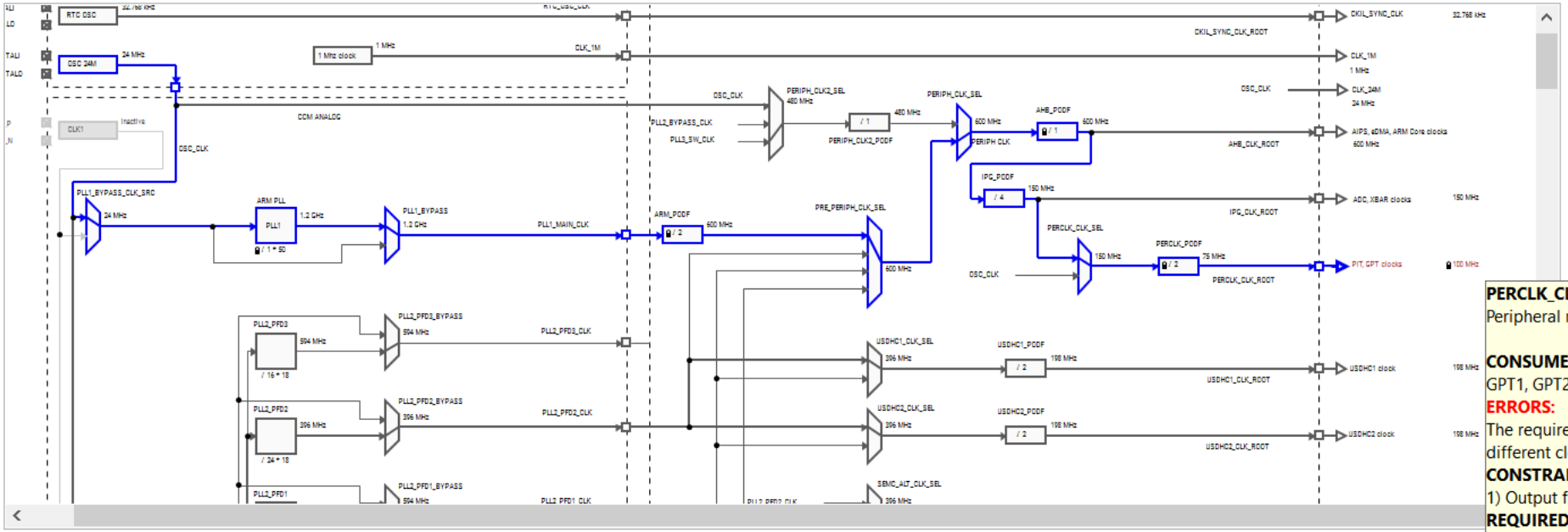
File Edit Navigate Search Project ConfigTools Clocks Run Window Help

evkmimxrt1060_gpio_pollingConf | Update Code | Functional Group | BOARD_BootClockRUN

Clocks Diagram

Run Mode RUN | On-chip oscillator 24MHz Enabled

PERCLK_CLK_ROOT



Clocks Table

Run Mode RUN | On-chip oscillator 24MHz Enabled

Clock Sources

Name	C..	Value
RTC OSC mode		External crystal 32kHz
24MHz clock source	☑	**24 MHz**
Power down mode		Disabled
OSC mode		External crystal 24 MHz
RC oscillator		Enabled
OSC ready ...nter value		128
CLK1 external clock sourc	☐	Inactive
CLK1 pins mode		Disabled
SAI1 MCLK	☐	Inactive

Clock Outputs

Name	L...	Value	A...y
GPT1 high frequency cloc		75 MHz	
GPT2 high frequency cloc		75 MHz	
LCDIF_CLK_ROOT		67.5 MHz	
LPI2C_CLK_ROOT		60 MHz	
LPSPI_CLK_ROOT		105.6 MHz	
LVDS1_CLK		1.2 GHz	
MQS MCLK		63.52... MHz	
PERCLK_CLK_ROOT	🔒	**100 MHz [75 MHz]**	±0.1%
SAI1 MCLK 1		63.52... MHz	

Overview | Details | Clock Consumers

Path Details: PERCLK_CLK_ROOT

Name	C..	L...	Value
Peripheral main clock select			Pre-peripheral clock output
AHB divider		🔒	/ 1
AHB divider Frequency			600 MHz
IPG divider			/ 4
IPG divider Frequency			150 MHz
PERCLK clock selector			IPG root clock
PERCLK clock divider		🔒	/ 2
PERCLK cloc...r Frequency			75 MHz
PERCLK_CLK_...T Frequency			75 MHz
PERCLK_CLK_ROOT		🔒	**100 MHz [75 MHz]**

PERCLK_CLK_ROOT [type:clock output, id: PERCLK_CLK_ROOT]
Peripheral root clock

CONSUMED BY:
GPT1, GPT2, PIT
ERRORS:
The requirement cannot be satisfied or is in conflict with other requirements. Try to select different clock path/mode or unlock/change some of the required settings.
CONSTRAINTS:
1) Output frequency must be lower than or equal to: 75 MHz
REQUIRED: (value is locked and cannot be changed by computation engine)
100 MHz ±0.1%
VALUE:
75 MHz

Code generation failed

Registers

all ☑ Show modified registers only

type filter text

Reg. Name	Set Value	Reset Value	Value Description
CCM_ANALOG_PFD	0x13111021	0x1311100c	
CCM_ANALOG_PLL	0x00002064	0x00013063	

ERRORS: evkmimxrt1060_gpio_pollingConfig: Requirement(s) not satisfiable

894M of 1188M

NXP MIMXRT1062xxxxA* (evkmimx...Config)

workspace - evkmimxrt1060_gpio_pollingConfig/evkmimxrt1060_gpio_pollingConfig.mex - MCUXpresso IDE

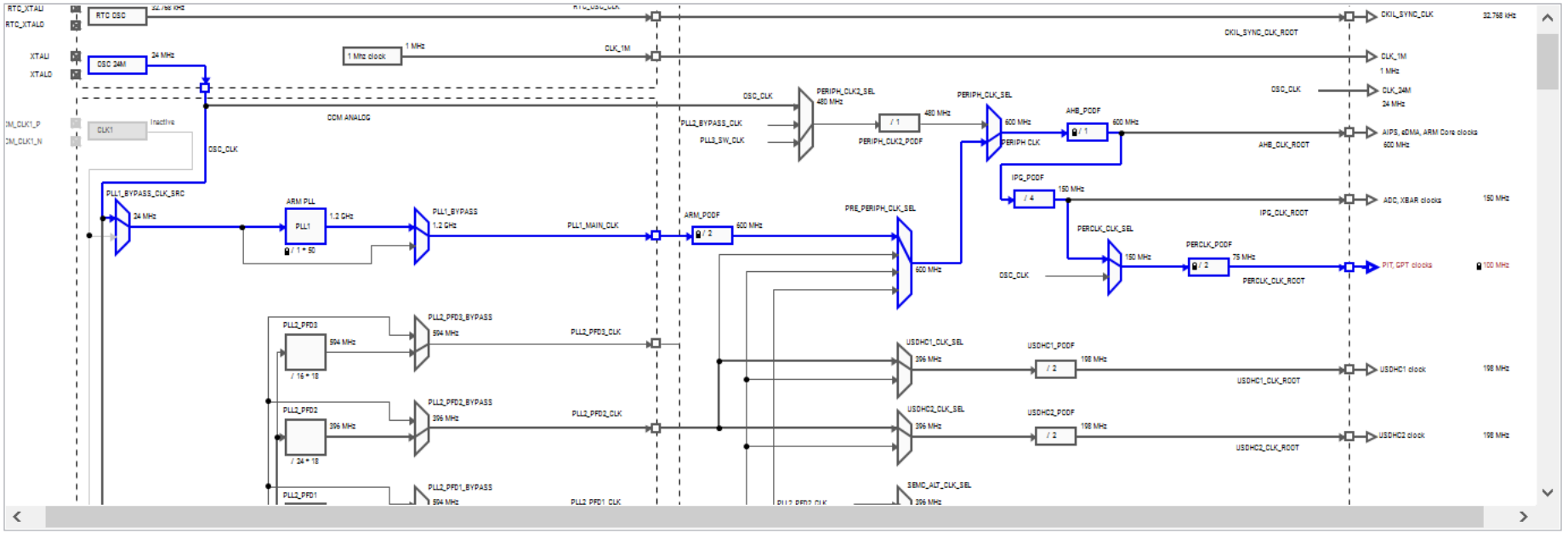
File Edit Navigate Search Project ConfigTools Clocks Run Window Help

evkmimxrt1060_gpio_pollingConf | Update Code | Functional Group | BOARD_BootClockRUN

Clocks Diagram

Run Mode RUN | On-chip oscillator 24MHz Enabled

PERCLK_CLK_ROOT



Clocks Table

Run Mode RUN | On-chip oscillator 24MHz Enabled

Clock Sources

Name	C..	Value
RTC OSC mode		External crystal 32kHz
24MHz clock source	☑	**24 MHz**
Power down mode		Disabled
OSC mode		External crystal 24 MHz
RC oscillator		Enabled
OSC ready ...nter value		128
CLK1 external clock sourc	☐	Inactive
CLK1 pins mode		Disabled
SAI1 MCLK	☐	Inactive

Clock Outputs

Name	L...	Value	A...y
GPT1 high frequency cloc		75 MHz	
GPT2 high frequency cloc		75 MHz	
LCDIF_CLK_ROOT		67.5 MHz	
LPI2C_CLK_ROOT		60 MHz	
LPSPI_CLK_ROOT		105.6 MHz	
LVDS1_CLK		1.2 GHz	
MQS MCLK		63.52... MHz	
PERCLK_CLK_ROOT	🔒	**100 MHz [75 MHz]**	±0.1%
SAI1 MCLK 1		63.52... MHz	

Overview | Details | Clock Consumers

Path Details: PERCLK_CLK_ROOT

Name	C..	L...	Value
PERCLK clock selector			IPG root clock
PERCLK clock divider		🔒	/ 2
PERCLK cloc...r Frequency			75 MHz
PERCLK_CLK_...T Frequency			75 MHz
PERCLK_CLK_ROOT		🔒	**100 MHz [75 MHz]**

Unlock
Find Near Valid Value

Code Preview

clock_config.h | clock_config.c

```
22 processor_version: 8.0.2
23 board: MIMXRT1060-EVK
24 * BE CAREFUL MODIFYING THIS COMMENT - IT IS YAML S
25
26 #include "clock_config.h"
27 #include "fsl_iomuxc.h"
28
29 /*******************************************************
30 * Definitions
31 *******************************************************
32
```

Code generation failed

Registers

all | Show modified registers only

type filter text

Reg. Name	Set Value	Reset Value	Value Description
CCM_ANALOG_PLL	0x00000032	0x2964619c	
CCM_ANALOG_PLL	0x00000001	0x05f5e100	
CCM_ANALOG_PLL	0x00313001	0x00011001	
CCM_ANALOG_PLL	0x00002001	0x00013001	

ERRORS: evkmimxrt1060_gpio_pollingConfig: Requirement(s) not satisfiable

810M of 1264M

NXP MIMXRT1062xxxxA* (evkmimx...Config)

workspace - evkmimxrt1060_gpio_pollingConfig/evkmimxrt1060_gpio_pollingConfig.mex - MCUXpresso IDE

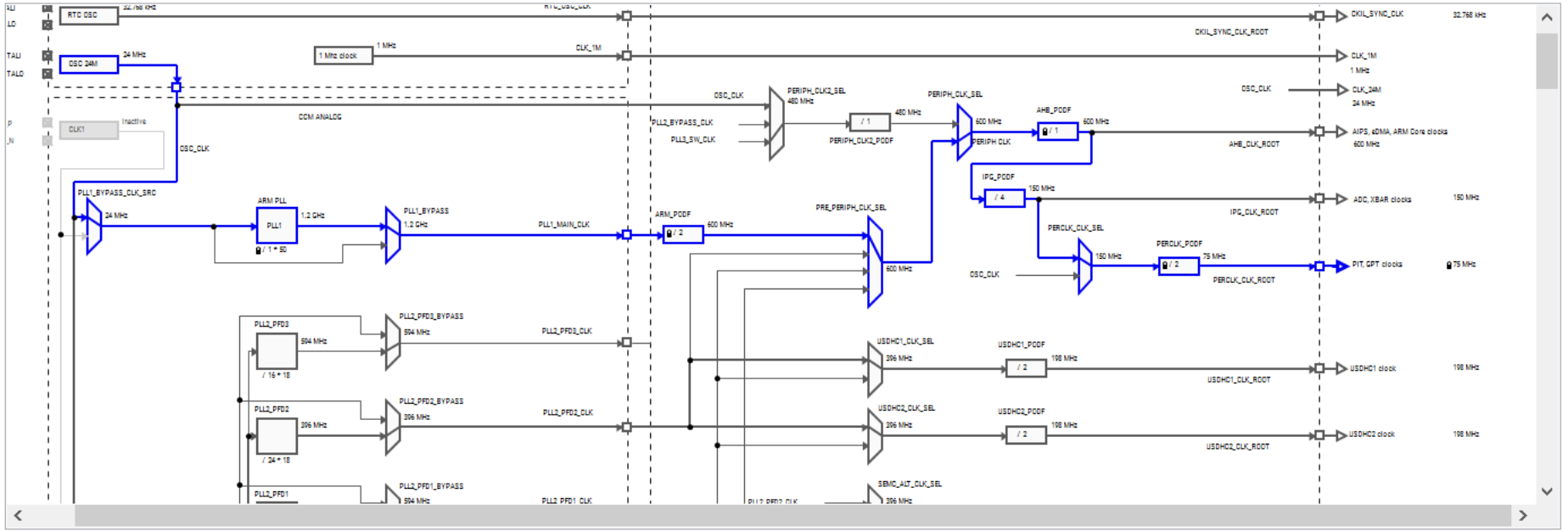
File Edit Navigate Search Project ConfigTools Clocks Run Window Help

evkmimxrt1060_gpio_pollingConf | Update Code | Functional Group | BOARD_BootClockRUN

Clocks Diagram

PERCLK_CLK_ROOT

Run Mode RUN | On-chip oscillator 24MHz Enabled



Clocks Table

Run Mode RUN | On-chip oscillator 24MHz Enabled

Clock Sources

Name	C..	Value
RTC OSC mode		External crystal 32kHz
24MHz clock source	☑	**24 MHz**
Power down mode		Disabled
OSC mode		External crystal 24 MHz
RC oscillator		Enabled
OSC ready ...nter value		128
CLK1 external clock sourc	☐	Inactive
CLK1 pins mode		Disabled
SAI1 MCLK	☐	Inactive

Clock Outputs

Name	L...	Value	A...y
GPT1 high frequency cloc		75 MHz	
GPT2 high frequency cloc		75 MHz	
LCDIF_CLK_ROOT		67.5 MHz	
LPI2C_CLK_ROOT		60 MHz	
LPSPI_CLK_ROOT		105.6 MHz	
LVDS1_CLK		1.2 GHz	
MQS MCLK		63.52... MHz	
PERCLK_CLK_ROOT	🔒	**75 MHz**	±0.1%
SAI1 MCLK 1		63.52... MHz	

Overview | Details | Clock Consumers

Path Details: PERCLK_CLK_ROOT

Name	C..	L...	Value
IPG divider			/ 4
IPG divider Frequency			150 MHz
PERCLK clock selector			IPG root clock
PERCLK clock divider		🔒	/ 2
PERCLK cloc...r Frequency			75 MHz
PERCLK_CLK_...T Frequency			75 MHz
PERCLK_CLK_ROOT		🔒	75 MHz

Code Preview

clock_config.h | clock_config.c

```
155     };
156 /*******************************************************
157  * Code for BOARD_BootClockRUN configuration
158  *******************************************************
159 void BOARD_BootClockRUN(void)
160 {
161     /* Init RTC OSC clock frequency. */
162     CLOCK_SetRtcXtalFreq(32768U);
163     /* Enable 1MHz clock output. */
164     XTALOSC24M->OSC_CONFIG2 |= XTALOSC24M_OSC_CONFI
```

Code successfully generated.

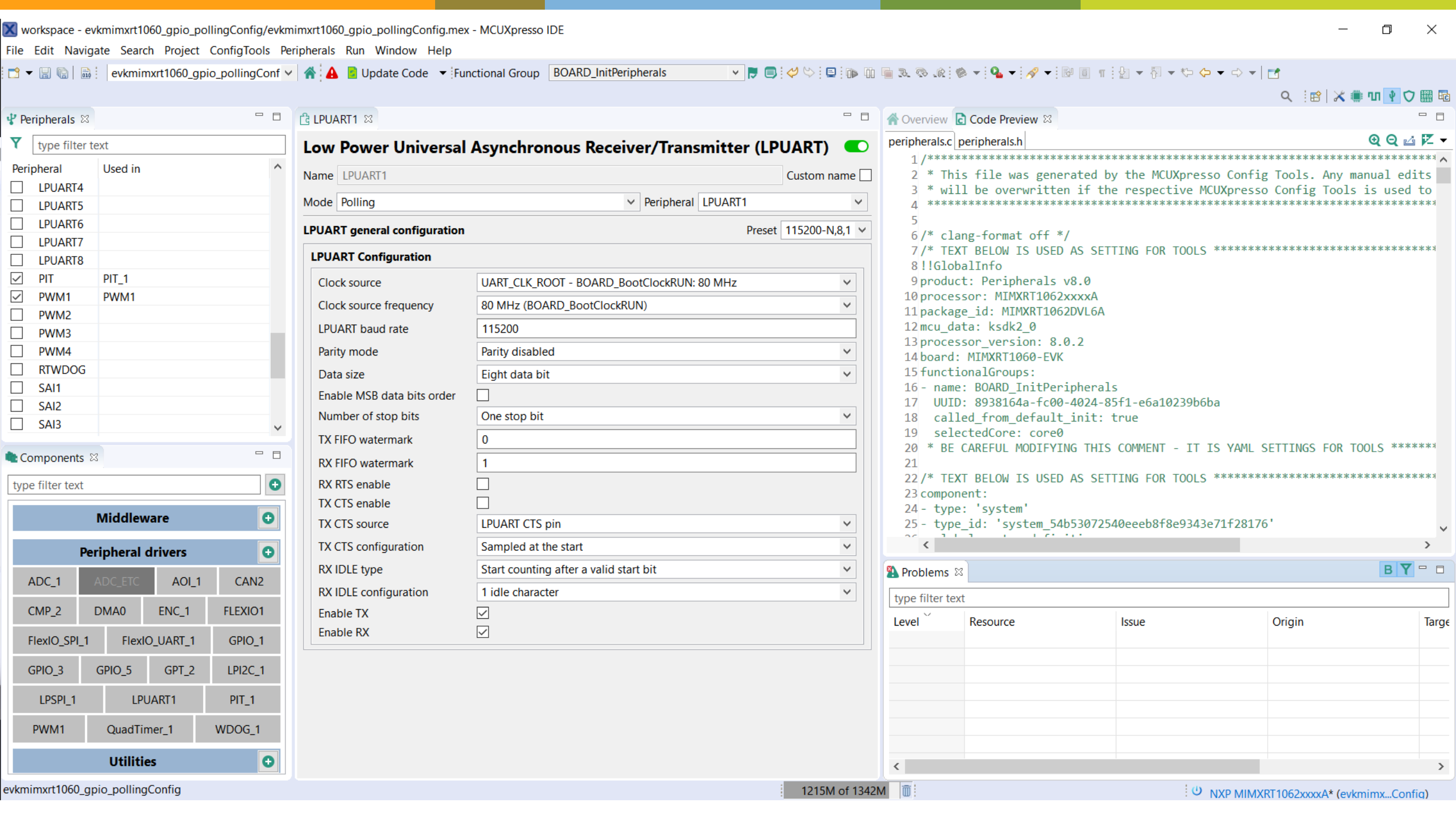
Registers

all | ☑ Show modified registers only

type filter text

Reg. Name	Set Value	Reset Value	Value Description
CCM_ANALOG_PLL	0x00000032	0x2964619c	
CCM_ANALOG_PLL	0x00000001	0x05f5e100	
CCM_ANALOG_PLL	0x00313001	0x00011001	
CCM_ANALOG_PLL	0x00002001	0x00013001	

evkmimxrt1060_gpio_pollingConfig | 990M of 1252M | NXP MIMXRT1062xxxxA* (evkmimx...Config)


workspace - evkmimxrt1060_gpio_pollingConfig/evkmimxrt1060_gpio_pollingConfig.mex - MCUXpresso IDE
File Edit Navigate Search Project ConfigTools Peripherals Run Window Help
evkmimxrt1060_gpio_pollingConf
Update Code
Functional Group
BOARD_InitPeripherals
Peripherals
type filter text
Peripheral
Used in
LPUART4
LPUART5
LPUART6
LPUART7
LPUART8
PIT
PIT_1
PWM1
PWM1
PWM2
PWM3
PWM4
RTWDOG
SAI1
SAI2
SAI3
Components
type filter text
Middleware
Peripheral drivers
ADC_1
ADC_ETC
AOI_1
CAN2
CMP_2
DMA0
ENC_1
FLEXIO1
FlexIO_SPI_1
FlexIO_UART_1
GPIO_1
GPIO_3
GPIO_5
GPT_2
LPI2C_1
LPSPI_1
LPUART1
PIT_1
PWM1
QuadTimer_1
WDOG_1
Utilities
LPUART1
Low Power Universal Asynchronous Receiver/Transmitter (LPUART)
Name
LPUART1
Custom name
Mode
Polling
Peripheral
LPUART1
LPUART general configuration
Preset
115200-N,8,1
LPUART Configuration
Clock source
UART_CLK_ROOT - BOARD_BootClockRUN: 80 MHz
Clock source frequency
80 MHz (BOARD_BootClockRUN)
LPUART baud rate
115200
Parity mode
Parity disabled
Data size
Eight data bit
Enable MSB data bits order
Number of stop bits
One stop bit
TX FIFO watermark
0
RX FIFO watermark
1
RX RTS enable
TX CTS enable
TX CTS source
LPUART CTS pin
TX CTS configuration
Sampled at the start
RX IDLE type
Start counting after a valid start bit
RX IDLE configuration
1 idle character
Enable TX
Enable RX
Overview
Code Preview
peripherals.c
peripherals.h
1 /***
2 * This file was generated by the MCUXpresso Config Tools. Any manual edits
3 * will be overwritten if the respective MCUXpresso Config Tools is used to
4 ***
5
6 /* clang-format off */
7 /* TEXT BELOW IS USED AS SETTING FOR TOOLS ********************************
8 !!GlobalInfo
9 product: Peripherals v8.0
10 processor: MIMXRT1062xxxxA
11 package_id: MIMXRT1062DVL6A
12 mcu_data: ksdk2_0
13 processor_version: 8.0.2
14 board: MIMXRT1060-EVK
15 functionalGroups:
16 - name: BOARD_InitPeripherals
17 UUID: 8938164a-fc00-4024-85f1-e6a10239b6ba
18 called_from_default_init: true
19 selectedCore: core0
20 * BE CAREFUL MODIFYING THIS COMMENT - IT IS YAML SETTINGS FOR TOOLS *******
21
22 /* TEXT BELOW IS USED AS SETTING FOR TOOLS ********************************
23 component:
24 - type: 'system'
25 - type_id: 'system_54b53072540eeeb8f8e9343e71f28176'
Problems
type filter text
Level
Resource
Issue
Origin
Targe
evkmimxrt1060_gpio_pollingConfig
1215M of 1342M
NXP MIMXRT1062xxxxA* (evkmimx...Config)

workspace - evkmimxrt1060_gpio_pollingConfig/evkmimxrt1060_gpio_pollingConfig.mex - MCUXpresso IDE

File Edit Navigate Search Project ConfigTools Peripherals Run Window Help

evkmimxrt1060_gpio_pollingConf | Update Code | Functional Group | BOARD_InitPeripherals

Peripherals

type filter text

Peripheral	Used in
LPUART4	
LPUART5	
LPUART6	
LPUART7	
LPUART8	
PIT	PIT_1
PWM1	PWM1
PWM2	
PWM3	
PWM4	
RTWDOG	
SAI1	
SAI2	
SAI3	

Components

type filter text

Middleware

Peripheral drivers

ADC_1	ADC_ETC	AOI_1	CAN2
CMP_2	DMA0	ENC_1	FLEXIO1
FlexIO_SPI_1	FlexIO_UART_1	GPIO_1	
GPIO_3	GPIO_5	GPT_2	LPI2C_1
LPSPI_1	LPUART1	PIT_1	
PWM1	QuadTimer_1	WDOG_1	

Utilities

LPUART1

Low Power Universal Asynchronous Receiver/Transmitter (LPUART)

Name: LPUART1 | Custom name

Mode: Polling | Peripheral: LPUART1

LPUART general configuration | Preset: 115200-N,8,1

LPUART Configuration

Clock source	UART_CLK_ROOT - BOARD_BootClockRUN: 80 MHz
Clock source frequency	80 MHz (BOARD_BootClockRUN)
LPUART baud rate	115200
Parity mode	Parity disabled
Data size	Eight data bit
Enable MSB data bits order	
Number of stop bits	One stop bit
TX FIFO watermark	0
RX FIFO watermark	1
RX RTS enable	
TX CTS enable	
TX CTS source	LPUART CTS pin
TX CTS configuration	Sampled at the start
RX IDLE type	Start counting after a valid start bit
RX IDLE configuration	
Enable TX	
Enable RX	

WARNINGS:
LPUART1 / lpuartConfig_t / lpuartConfig / enableRx: Signal RX of the peripheral LPUART1 is not routed.

Overview | Code Preview

peripherals.c | peripherals.h

```
1358       - rxIdleType: 'kLPUART_IdleTypeStartBit'
1359       - rxIdleConfig: 'kLPUART_IdleCharacter1'
1360       - enableTx: 'true'
1361       - enableRx: 'true'
1362     - quick_selection: 'QuickSelection1'
1363 * BE CAREFUL MODIFYING THIS COMMENT - IT IS YAML SETTINGS FOR TOOLS *******
1364 /* clang-format on */
1365 const lpuart_config_t LPUART1_config = {
1366   .baudRate_Bps = 115200,
1367   .parityMode = kLPUART_ParityDisabled,
1368   .dataBitsCount = kLPUART_EightDataBits,
1369   .isMsb = false,
1370   .stopBitCount = kLPUART_OneStopBit,
1371   .txFifoWatermark = 0,
1372   .rxFifoWatermark = 1,
1373   .enableRxRTS = false,
1374   .enableTxCTS = false,
1375   .txCtsSource = kLPUART_CtsSourcePin,
1376   .txCtsConfig = kLPUART_CtsSampleAtStart,
1377   .rxIdleType = kLPUART_IdleTypeStartBit,
1378   .rxIdleConfig = kLPUART_IdleCharacter1,
1379   .enableTx = true,
1380   .enableRx = true
1381 };
1382
```

Problems

Level	Resource	Issue	Origin	Targe
Warning	LPUART1.uart_tx	Signal TX of the peripheral ...	Peripherals:BOARD_InitPeri...	Pins:
Warning	LPUART1.uart_rx	Signal RX of the peripheral ...	Peripherals:BOARD_InitPeri...	Pins:

WARNINGS: evkmimxrt1060_gpio_pollingConfig: Signal RX of the peripheral LPUART1 is not routed. Signal TX of the peripheral LPUART1 is not routed.

909M of 1335M

NXP MIMXRT1062xxxxA* (evkmimx...Config)

workspace - evkmimxrt1060_gpio_pollingConfig/evkmimxrt1060_gpio_pollingConfig.mex - MCUXpresso IDE

File Edit Navigate Search Project ConfigTools Peripherals Run Window Help

evkmimxrt1060_gpio_pollingConf | Update Code | Functional Group | BOARD_InitPeripherals

Peripherals

type filter text

Peripheral	Used in
LPUART4	
LPUART5	
LPUART6	
LPUART7	
LPUART8	
PIT	PIT_1
PWM1	PWM1
PWM2	
PWM3	
PWM4	
RTWDOG	
SAI1	
SAI2	
SAI3	

Components

type filter text

Middleware

Peripheral drivers

ADC_1	ADC_ETC	AOI_1	CAN2
CMP_2	DMA0	ENC_1	FLEXIO1
FlexIO_SPI_1	FlexIO_UART_1	GPIO_1	
GPIO_3	GPIO_5	GPT_2	LPI2C_1
LPSPI_1	LPUART1	PIT_1	
PWM1	QuadTimer_1	WDOG_1	

Utilities

LPUART1

Low Power Universal Asynchronous Receiver/Transmitter (LPUART)

Name: LPUART1 | Custom name

Mode: Polling | Peripheral: LPUART1

LPUART general configuration | Preset: 115200-N,8,1

LPUART Configuration

Clock source	UART_CLK_ROOT - BOARD_BootClockRUN: 80 MHz
Clock source frequency	80 MHz (BOARD_BootClockRUN)
LPUART baud rate	115200
Parity mode	Parity disabled
Data size	Eight data bit
Enable MSB data bits order	☐
Number of stop bits	One stop bit
TX FIFO watermark	0
RX FIFO watermark	1
RX RTS enable	☐
TX CTS enable	☐
TX CTS source	LPUART CTS pin
TX CTS configuration	Sampled at the start
RX IDLE type	Start counting after a valid start bit
RX IDLE configuration	1 idle character
Enable TX	☑
Enable RX	☑

Overview | Code Preview

peripherals.c | peripherals.h

```
1 /***********************************************************************************
2  * This file was generated by the MCUXpresso Config Tools. Any manual edits
3  * will be overwritten if the respective MCUXpresso Config Tools is used to
4  ***********************************************************************************
5
6 /* clang-format off */
7 /* TEXT BELOW IS USED AS SETTING FOR TOOLS ********************************
8 !!GlobalInfo
9 product: Peripherals v8.0
10 processor: MIMXRT1062xxxxA
11 package_id: MIMXRT1062DVL6A
12 mcu_data: ksdk2_0
13 processor_version: 8.0.2
14 board: MIMXRT1060-EVK
15 functionalGroups:
16 - name: BOARD_InitPeripherals
17   UUID: 8938164a-fc00-4024-85f1-e6a10239b6ba
18   called_from_default_init: true
19   selectedCore: core0
20 * BE CAREFUL MODIFYING THIS COMMENT - IT IS YAML SETTINGS FOR TOOLS *******
21
22 /* TEXT BELOW IS USED AS SETTING FOR TOOLS ********************************
23 component:
24 - type: 'system'
25 - type_id: 'system_54b53072540eeeb8f8e9343e71f28176'
```

Problems

type filter text

Level	Resource	Issue	Origin	Target
Warning	LPUART1.uart_tx	Signal TX of the peripheral ...	Peripherals:BOARD_InitPeri...	Pins:
Warning	LPUART1.uart_rx	Signal RX of the peripheral ...	Peripherals:BOARD_InitPeri...	Pins:

Issue: Signal TX of the peripheral LPUART1 is not routed.
Level: Warning
Type: Validation
Tool: Pins
Origin: Peripherals:BOARD_InitPeripherals
Target: Pins: BOARD_InitPins
Resource: LPUART1.uart_tx

There is a quick-fix available for the problem, see context menu for details.

WARNINGS: evkmimxrt1060_gpio_pollingConfig: Signal RX of the peripheral LPUART1 is not routed. Signal TX of the peripheral LPUART1 is not routed.

834M of 1327M

workspace - evkmimxrt1060_gpio_pollingConfig/evkmimxrt1060_gpio_pollingConfig.mex - MCUXpresso IDE

File Edit Navigate Search Project ConfigTools Pins Run Window Help

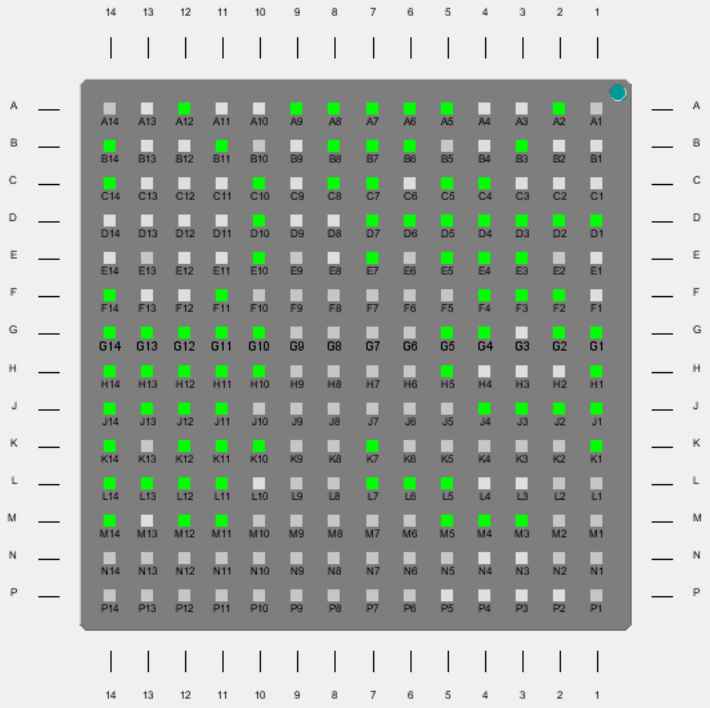
evkmimxrt1060_gpio_pollingConf | Update Code | Functional Group | BOARD_InitPins

Pins | Peripheral Signals | Power Groups

type filter text

- LPSPI1
- LPSPI2
- LPSPI3
- LPSPI4
- LPUART1
  - CTS_B » [H14] GPIO_AD_B0_14
  - RTS_B » [L10] GPIO_AD_B0_15
  - RX » [L14] GPIO_AD_B0_13
  - *TRG » 46 pins, 62 signals*
  - TX » [K14] GPIO_AD_B0_12
- LPUART2
- LPUART3
- LPUART4
- LPUART5
- LPUART6
- LPUART7
- LPUART8
- MQS
- PIT
- PWM1
  - A, 0 » [G2] GPIO_EMC_23 / 2 pins
  - A, 1 » [D2] GPIO_EMC_25 / 2 pins
  - A, 2 » [A2] GPIO_EMC_27 / 2 pins
  - A, 3 » [G13] GPIO_AD_B0_10 / 5 pins

Package [Pins Bottom]



Overview | Code Preview

pin_mux.c | pin_mux.h

```
/***********************************************
 * This file was generated by the MCUXpresso Confi
 * will be overwritten if the respective MCUXpress
 ***********************************************

/*
 * TEXT BELOW IS USED AS SETTING FOR TOOLS *******
!!GlobalInfo
product: Pins v8.0
processor: MIMXRT1062xxxxA
package_id: MIMXRT1062DVL6A
mcu_data: ksdk2_0
processor_version: 8.0.2
board: MIMXRT1060-EVK
pin_labels:
- {pin_num: D5, pin_signal: GPIO_EMC_32, label: GP
- {pin_num: C4, pin_signal: GPIO_EMC_33, label: GP
- {pin_num: D4, pin_signal: GPIO_EMC_34, label: GP
- {pin_num: E4, pin_signal: GPIO_EMC_37, label: GP
- {pin_num: D6, pin_signal: GPIO_EMC_38, label: GP
- {pin_num: B7, pin_signal: GPIO_EMC_39, label: GP
- {pin_num: H10, pin_signal: GPIO_AD_B0_01, label:
```

Registers

all | Show modified registers only

type filter text

Reg. Name	Set Value	Reset Value	Value Description
IOMUXC_FLEXPWM	0x00000003	0x00000000	
IOMUXC_FLEXPWM	0x00000001	0x00000000	
IOMUXC_GPR_GPR	0xcdfb0004	0x00000000	
IOMUXC_GPT2_IPP	0x00000001	0x00000000	
IOMUXC_GPT2_IPP	0x00000001	0x00000000	
IOMUXC_LPI2C1_S	0x00000001	0x00000000	
IOMUXC_LPI2C1_SI	0x00000001	0x00000000	

Routed Pins

type filter text

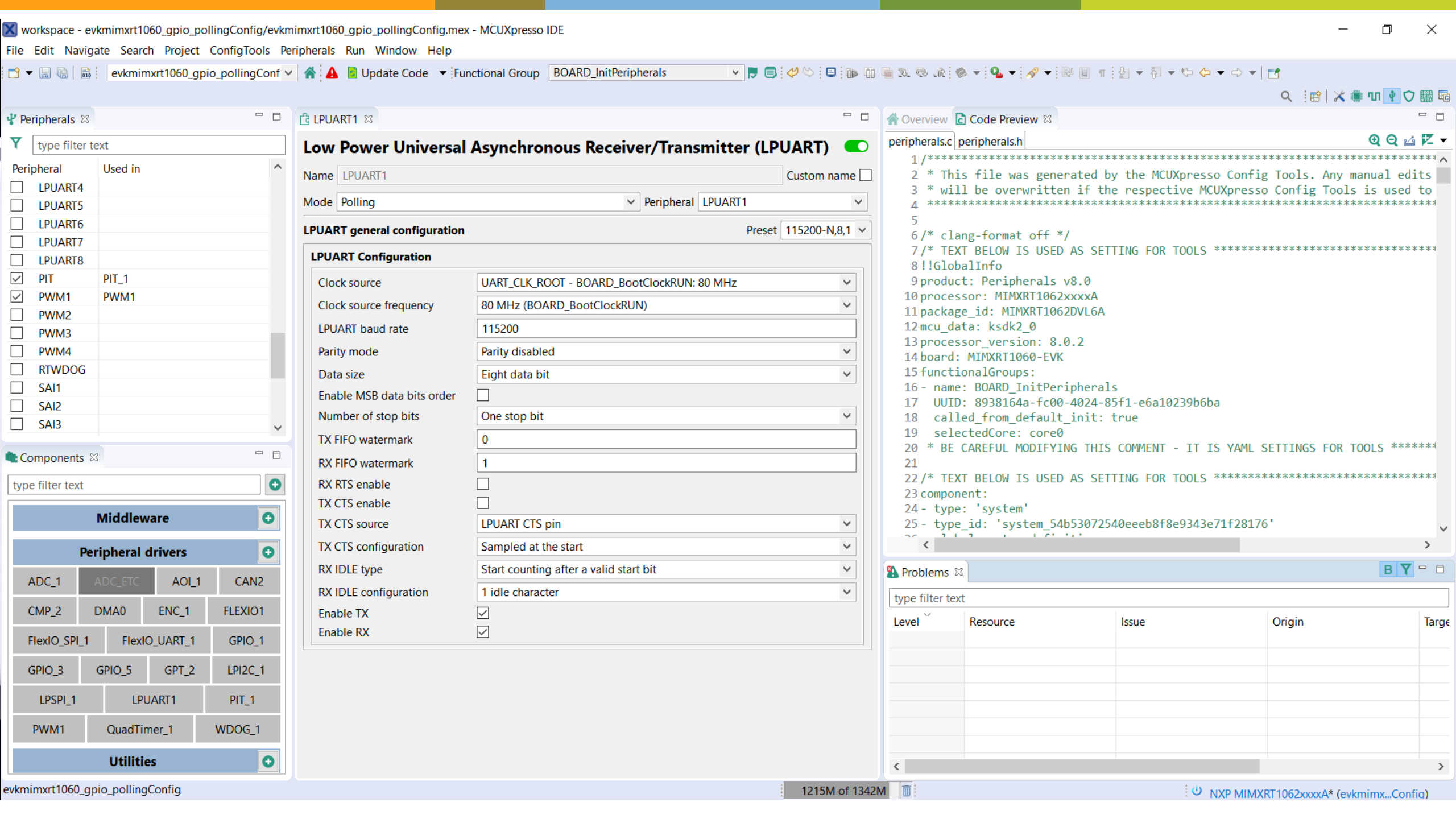
Routed Pins for BOARD_InitP... 105

#	Peripheral	Signal	Route to	Label	Identifier	Power group	Direction	GPIO initial state	GPIO interrupt	Software Input On	Hysteresis enat
L13	ADC1	IN, 15	GPIO_AD_B1_10	SAI1_RX_SYNC/CSI_D7/...	CSI_D7	*NVCC_GPIO (0V)*	*Input*	*n/a*	*n/a*	*Disabled*	*Disable*
C8	FLEXIO2	IO, 04	GPIO_B0_04	LCDIF_D0/BT_CFG[0]	LCDIF_D0	*NVCC_GPIO (0V)*	*Not Specified*	*n/a*	*n/a*	*Disabled*	*Disable*
B8	FLEXIO2	IO, 05	GPIO_B0_05	LCDIF_D1/BT_CFG[1]	LCDIF_D1	*NVCC_GPIO (0V)*	*Not Specified*	*n/a*	*n/a*	*Disabled*	*Disable*
A8	FLEXIO2	IO, 06	GPIO_B0_06	LCDIF_D2/BT_CFG[2]	LCDIF_D2	*NVCC_GPIO (0V)*	*Not Specified*	*n/a*	*n/a*	*Disabled*	*Disable*

evkmimxrt1060_gpio_pollingConfig

987M of 1394M

NXP MIMXRT1062xxxxA* (evkmimx...Config)


workspace - evkmimxrt1060_gpio_pollingConfig/evkmimxrt1060_gpio_pollingConfig.mex - MCUXpresso IDE
File Edit Navigate Search Project ConfigTools Peripherals Run Window Help
evkmimxrt1060_gpio_pollingConf
Update Code
Functional Group
BOARD_InitPeripherals
Peripherals
type filter text
Peripheral
Used in
LPUART4
LPUART5
LPUART6
LPUART7
LPUART8
PIT
PIT_1
PWM1
PWM1
PWM2
PWM3
PWM4
RTWDOG
SAI1
SAI2
SAI3
Components
type filter text
Middleware
Peripheral drivers
ADC_1
ADC_ETC
AOI_1
CAN2
CMP_2
DMA0
ENC_1
FLEXIO1
FlexIO_SPI_1
FlexIO_UART_1
GPIO_1
GPIO_3
GPIO_5
GPT_2
LPI2C_1
LPSPI_1
LPUART1
PIT_1
PWM1
QuadTimer_1
WDOG_1
Utilities
LPUART1
Low Power Universal Asynchronous Receiver/Transmitter (LPUART)
Name
LPUART1
Custom name
Mode
Polling
Peripheral
LPUART1
LPUART general configuration
Preset
115200-N,8,1
LPUART Configuration
Clock source
UART_CLK_ROOT - BOARD_BootClockRUN: 80 MHz
Clock source frequency
80 MHz (BOARD_BootClockRUN)
LPUART baud rate
115200
Parity mode
Parity disabled
Data size
Eight data bit
Enable MSB data bits order
Number of stop bits
One stop bit
TX FIFO watermark
0
RX FIFO watermark
1
RX RTS enable
TX CTS enable
TX CTS source
LPUART CTS pin
TX CTS configuration
Sampled at the start
RX IDLE type
Start counting after a valid start bit
RX IDLE configuration
1 idle character
Enable TX
Enable RX
Overview
Code Preview
peripherals.c
peripherals.h
1 /***
2 * This file was generated by the MCUXpresso Config Tools. Any manual edits
3 * will be overwritten if the respective MCUXpresso Config Tools is used to
4 ***
5
6 /* clang-format off */
7 /* TEXT BELOW IS USED AS SETTING FOR TOOLS ********************************
8 !!GlobalInfo
9 product: Peripherals v8.0
10 processor: MIMXRT1062xxxxA
11 package_id: MIMXRT1062DVL6A
12 mcu_data: ksdk2_0
13 processor_version: 8.0.2
14 board: MIMXRT1060-EVK
15 functionalGroups:
16 - name: BOARD_InitPeripherals
17 UUID: 8938164a-fc00-4024-85f1-e6a10239b6ba
18 called_from_default_init: true
19 selectedCore: core0
20 * BE CAREFUL MODIFYING THIS COMMENT - IT IS YAML SETTINGS FOR TOOLS *******
21
22 /* TEXT BELOW IS USED AS SETTING FOR TOOLS ********************************
23 component:
24 - type: 'system'
25 - type_id: 'system_54b53072540eeeb8f8e9343e71f28176'
Problems
type filter text
Level
Resource
Issue
Origin
Targe
evkmimxrt1060_gpio_pollingConfig
1215M of 1342M
NXP MIMXRT1062xxxxA* (evkmimx...Config)

Google "model based design"

All Images Books News Shopping More Settings Tools

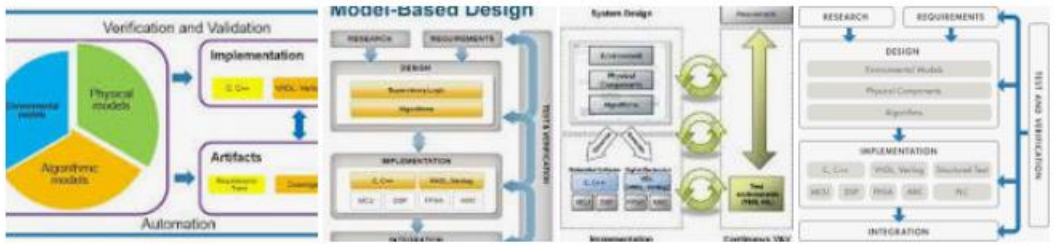
About 1,670,000 results (0.90 seconds)

Scholarly articles for **"model based design"**

A **model-based design** methodology for cyber-physical … - Jensen - Cited by 255

Model-based design and evaluation of interactive … - Paterno - Cited by 1243

Model-based design of experiments for parameter … - Franceschini - Cited by 580

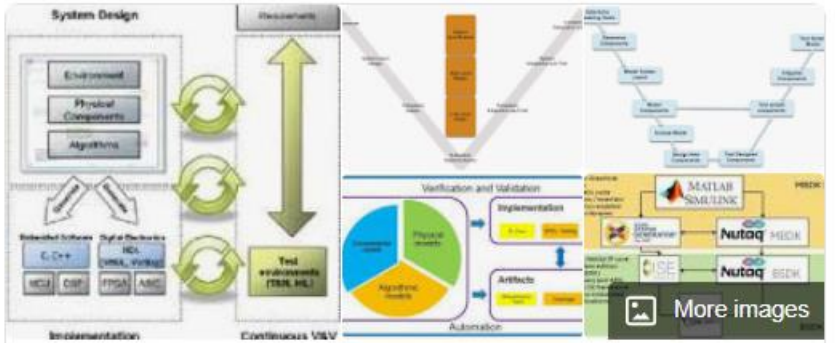


Model-Based Design (MBD) is a mathematical and visual method of addressing problems associated with designing complex control, signal processing and communication systems. It is used in many motion control, industrial equipment, aerospace, and automotive applications.

en.wikipedia.org › wiki › Model-based_design

Model-based design - Wikipedia

About Featured Snippets Feedback

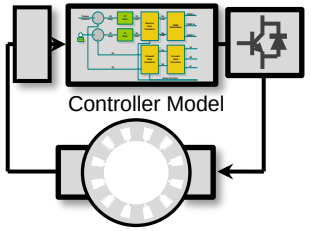


Model-based design

Model-Based Design is a mathematical and visual method of addressing problems associated with designing complex control, signal processing and communication systems. It is used in many motion control, industrial equipment, aerospace, and automotive applications. Wikipedia

Feedback

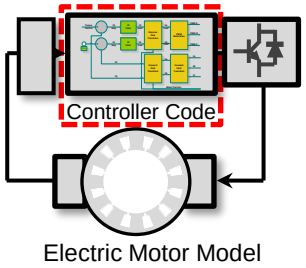
Idea Incubation



PC Environment

Automatic Code Generation

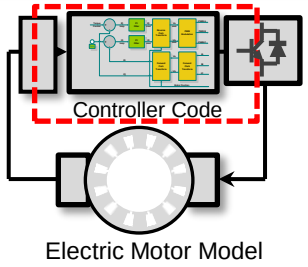
To SIL



PC Environment

Code Validation

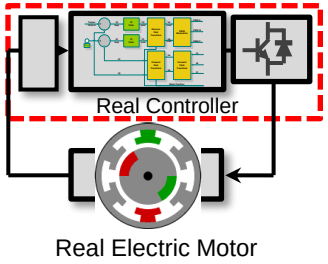
To PIL



PC Environment + MCU

Final Product

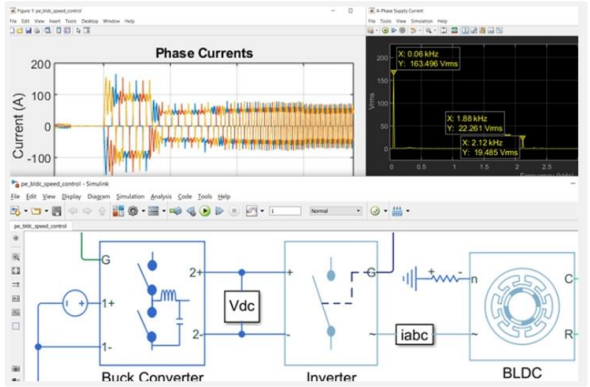
To MCU



MCU with Embedded Control Module (ECM)

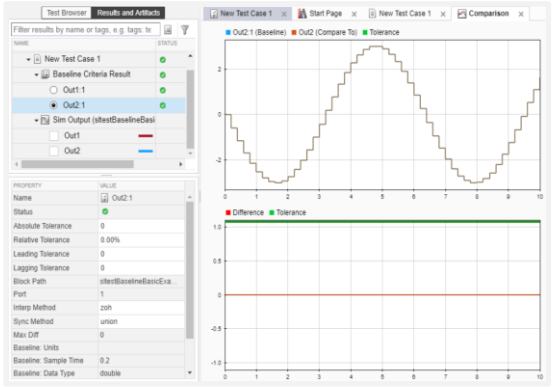
Step 1 – System Requirements
Model-in-the-Loop

- Software requirements
- Control system requirements
- Overall application control strategy



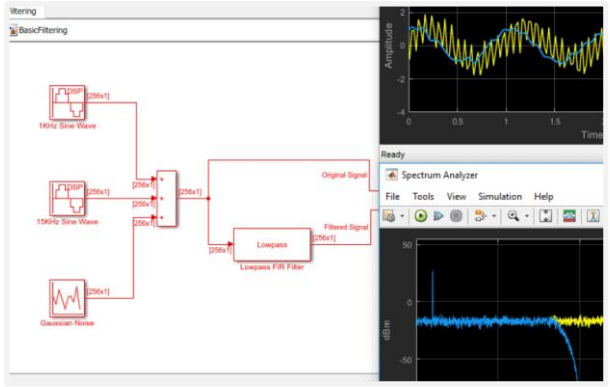
Step 2 – Modeling/Simulation
Software-in-the-Loop

- Control algorithm design
- Code generation preparation
- Control system design
- Start testing algorithm



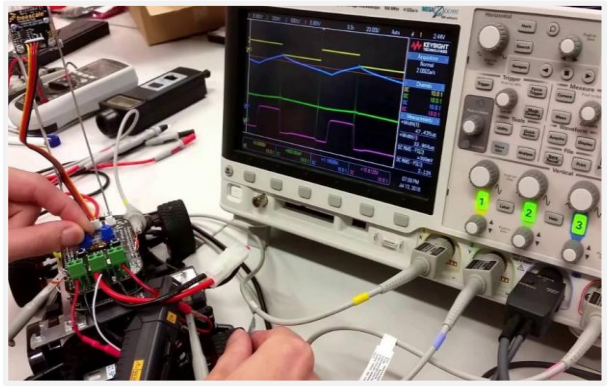
Step 3 – Rapid Prototype
Processor-in-the-Loop

- Controller code generation
- Determine execution time on MCU
- Verify algorithm on MCU
- See memory/stack usage on MCU



Step 4 – Target MCU Implementation
MCU Final Application

- Validation/verification phase
- Controller code generation
- Test system in target environment using tools for data logging and parameter tuning

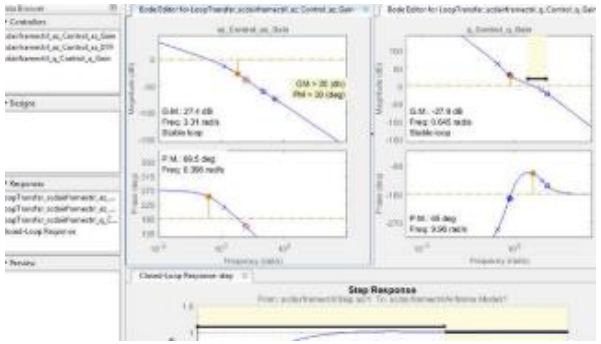


MATHWORKS EXTENSIVE TOOLS ECOSYSTEM

Control & Design

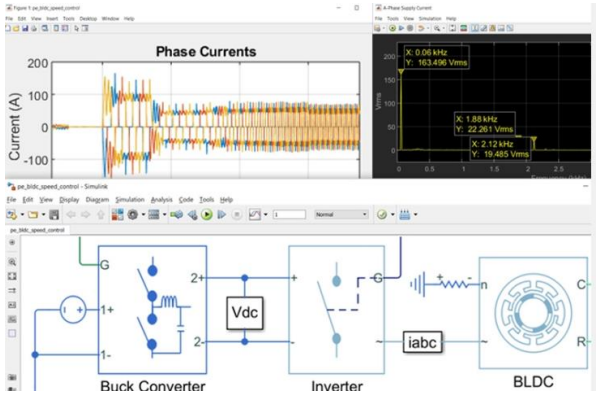
- Control Design

  Tuning & Auto tuning, Frequency Response



- Simscape

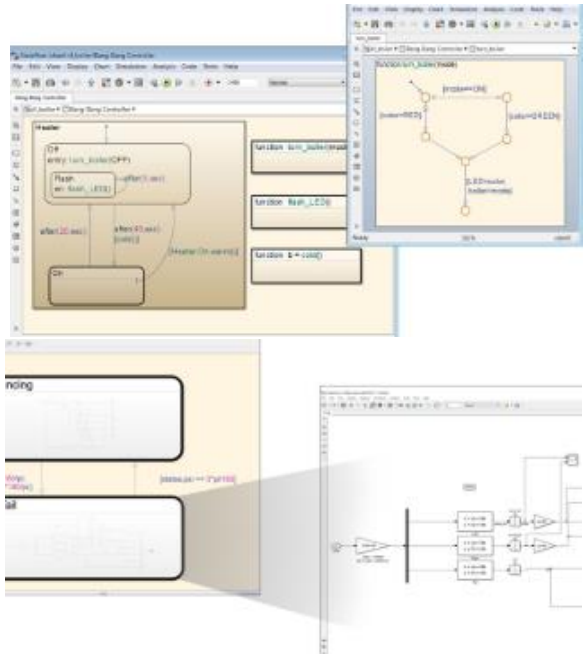
  Motors, IGBT, Diodes, Thermal, Spice



Event Based Modeling

- Stateflow

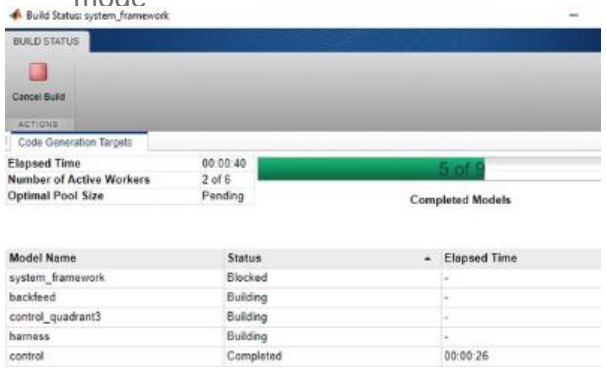
  Logic design, Scheduling



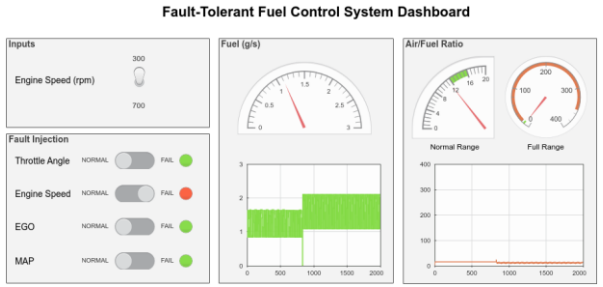
Code Generation & Interfacing

- Coders

  Code generation, legacy code integration, XCP, HIL, PIL, External mode



- Tuning & Visualizing



Certification & Validation

- IEC Certification Kit

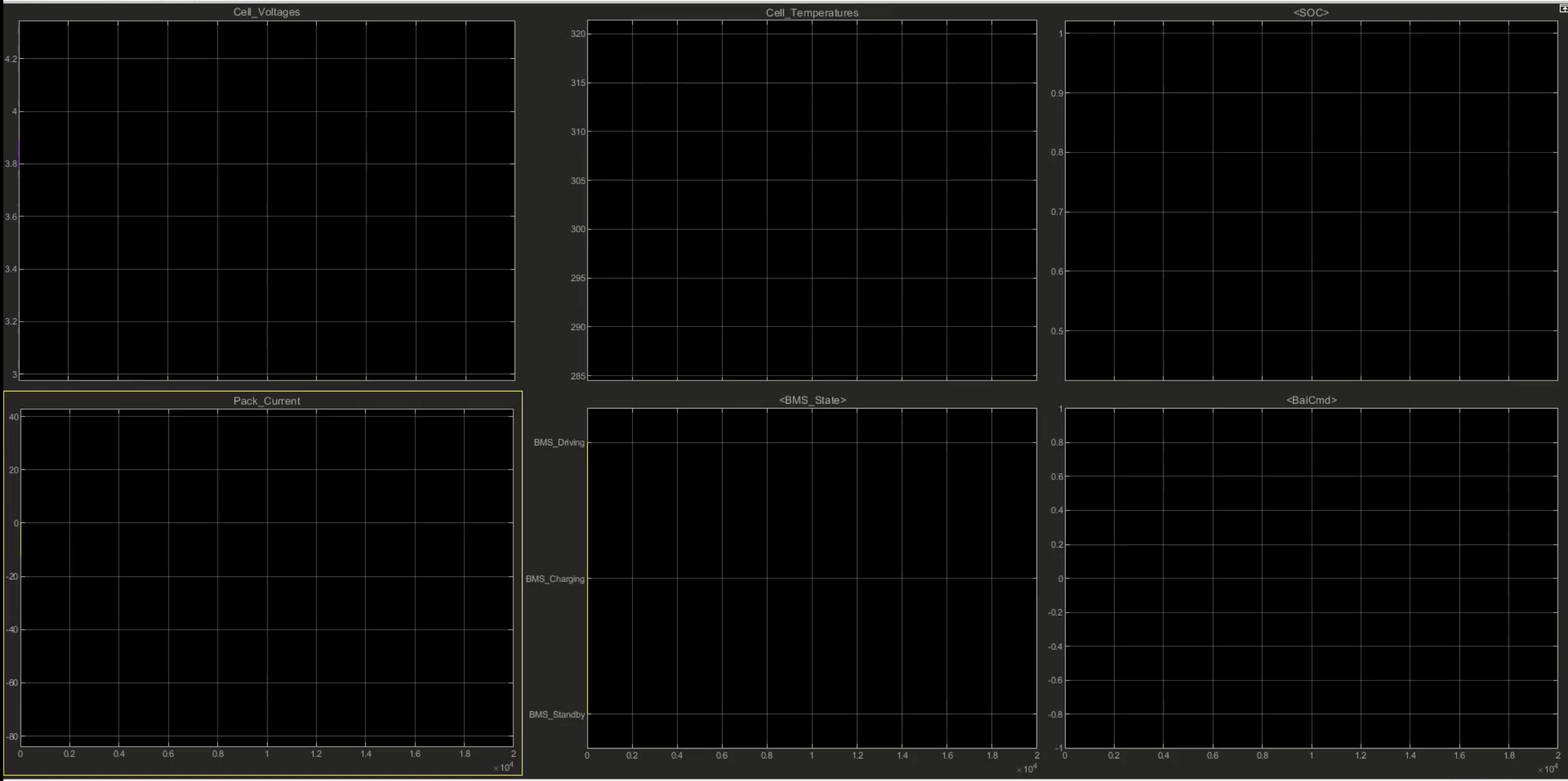
  IEC 61508, ISO26262, EN50128, IEC62304

- Simulink Requirements

  Requirements, Trace PRD, Track Status

Viewer: Scope (Cell_Voltages, Pack_Current, Cell_Temperatures, <BMS_State>, <SOC>, <BalCmd>)

File Tools View Simulation Help



Running

Sample based T=24.500

Battery Management System

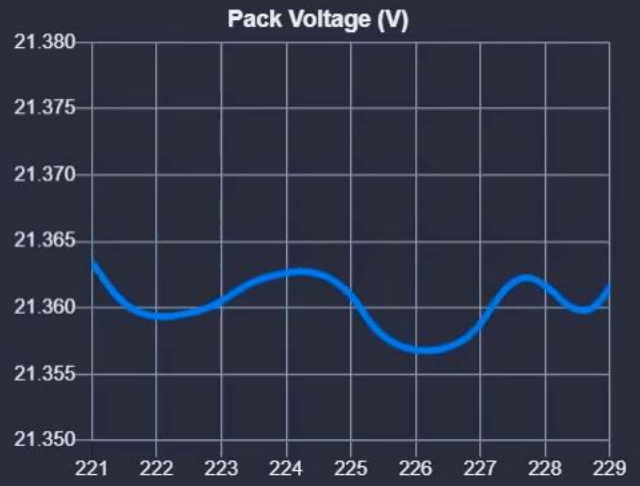
File | C:/build/index.html

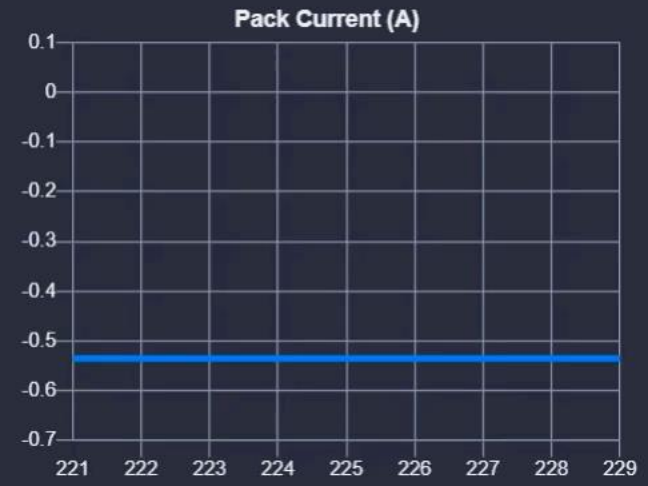
Battery Management System

Dashboard | Cells Pack | Raw Data | System Configuration | Disconnect

Summary

State of charge	**64.87%**
Voltage	**21.36V**
Current	**-0.54A**
Temperature	**26.60°C**
Power	**-11.53W**
Status	**Discharging**





Faults Status

Voltage Sensor | Over Current | High Temp | Low Temp

Over Voltage | Under Voltage | Contactor Fault for Charger | Contactor Fault for Inverter

Faults History

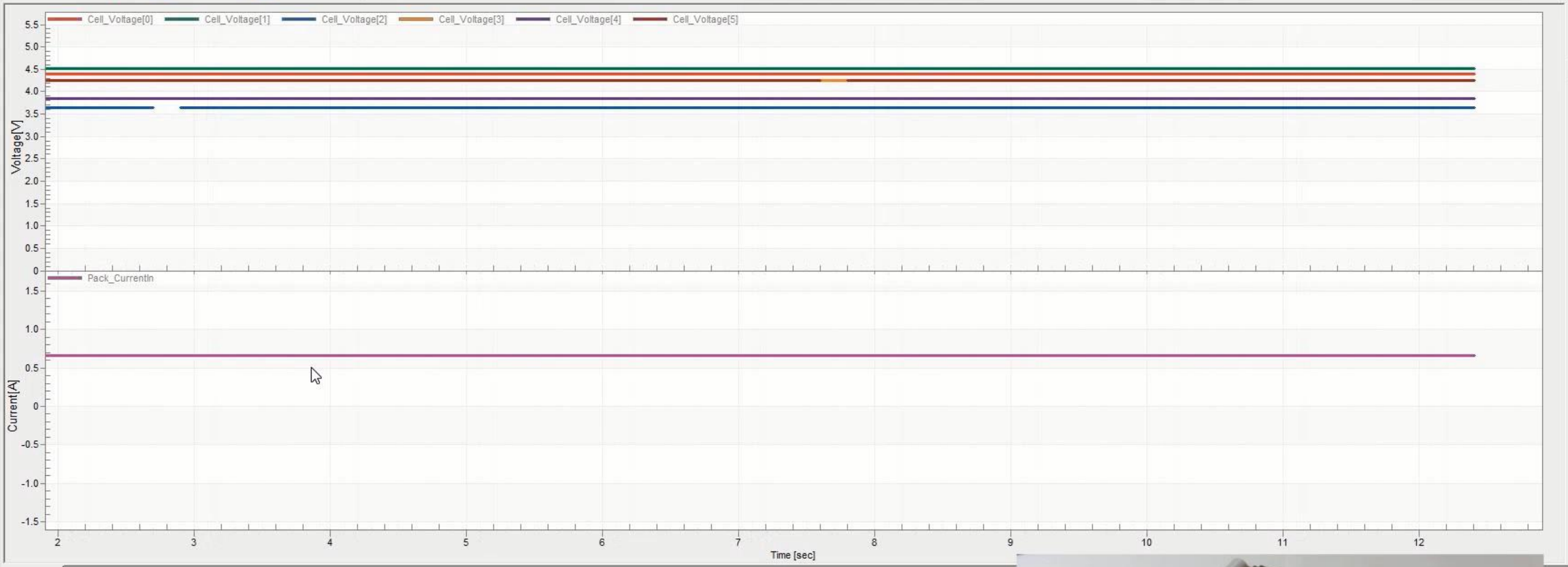
bms.pmpx - FreeMASTER

File Edit View Oscilloscope Project Tools Help

Project Tree

BMS Visualizer Project

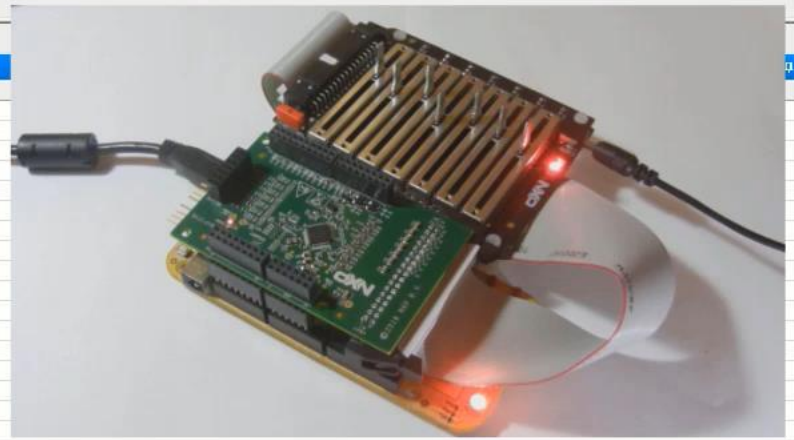
Cell Voltages



Cell Voltages

Variable Watch

Name	Value	Unit
Pack_VoltageIn	24.822	V
Pack_CurrentIn	0.664	A
Cell_Voltage[0]	4.399	V
Cell_Voltage[1]	4.514	V
Cell_Voltage[2]	3.650	V
Cell_Voltage[3]	4.258	V
Cell_Voltage[4]	3.848	V
Cell_Voltage[5]	4.247	V
Pack_TemperatureIn	27.7	°C
BMS_State	Driving [2]	ENUM
BMS_Info_VoltSensor	0	DEC
BMS_Info_OverCurrent	1	DEC
BMS_Info_HighTemp	0	DEC
BMS_Info_LowTemp	0	DEC
BMS_Info_OverVolt	1	DEC
BMS_Info_UnderVolt	0	DEC
BMS_Info_Charger	0	DEC
BMS_Info_Inverter	0	DEC

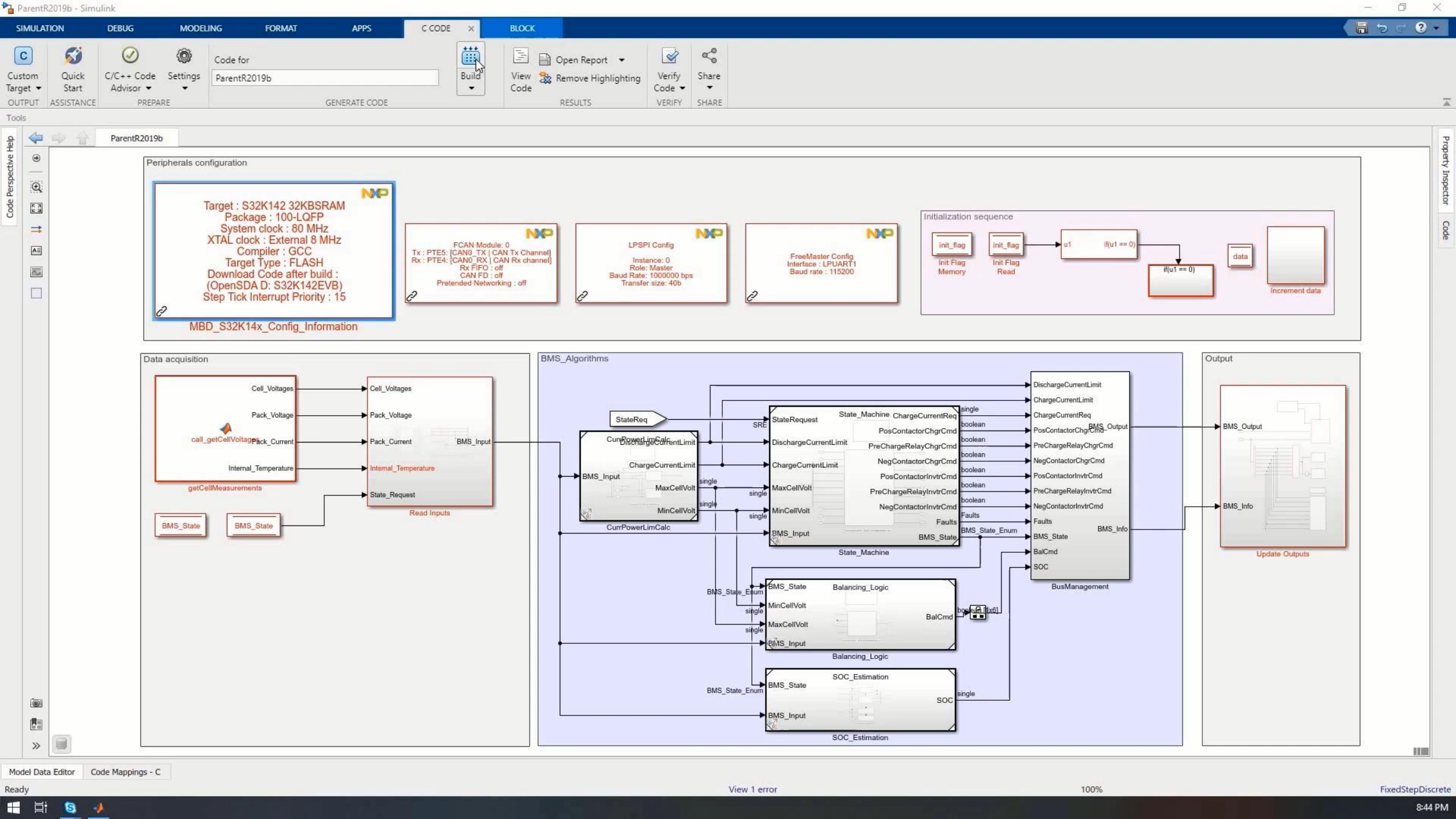


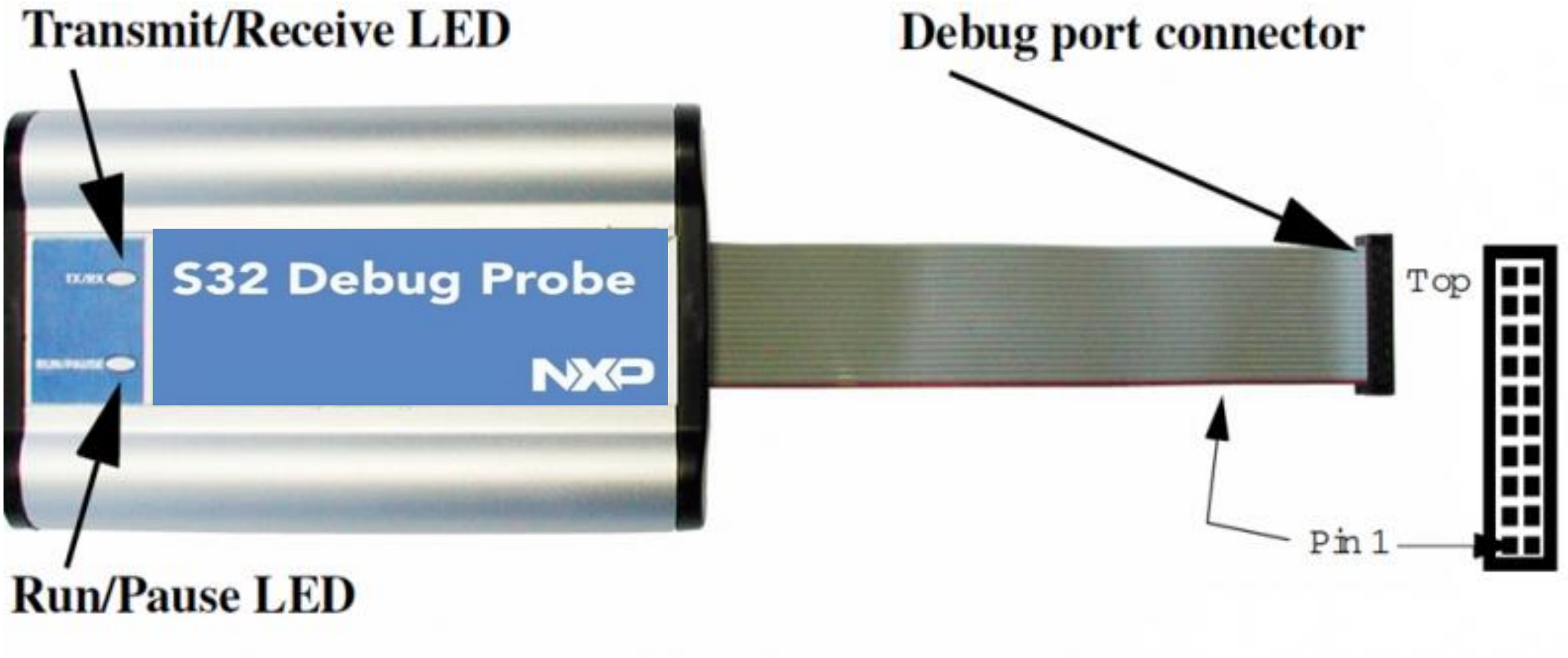
Ready

RS232 UART Communication; COM14; speed=115200

Scope Running

8:48 PM


ParentR2019b - Simulink
SIMULATION
DEBUG
MODELING
FORMAT
APPS
C CODE
BLOCK
Custom Target
Quick Start
C/C++ Code Advisor
Settings
Code for
ParentR2019b
Build
View Code
Open Report
Remove Highlighting
Verify Code
Share
OUTPUT
ASSISTANCE
PREPARE
GENERATE CODE
RESULTS
VERIFY
SHARE
Tools
ParentR2019b
Code Perspective Help
Property Inspector
Code
Peripherals configuration
Target : S32K142 32KBSRAM
Package : 100-LQFP
System clock : 80 MHz
XTAL clock : External 8 MHz
Compiler : GCC
Target Type : FLASH
Download Code after build :
(OpenSDA D: S32K142EVB)
Step Tick Interrupt Priority : 15
MBD_S32K14x_Config_Information
FCAN Module: 0
Tx : PTE5: [CAN0_TX | CAN Tx Channel]
Rx : PTE4: [CAN0_RX | CAN Rx channel]
Rx FIFO : off
CAN FD : off
Pretended Networking : off
LPSPI Config
Instance: 0
Role: Master
Baud Rate: 1000000 bps
Transfer size: 40b
FreeMaster Config
Interface : LPUART1
Baud rate : 115200
Initialization sequence
init_flag
Init Flag Memory
init_flag
Init Flag Read
u1
if(u1 == 0)
if(u1 == 0)
data
Increment data
Data acquisition
Cell_Voltages
Pack_Voltage
Pack_Current
Internal_Temperature
call_getCellVoltages
getCellMeasurements
Cell_Voltages
Pack_Voltage
Pack_Current
Internal_Temperature
State_Request
BMS_Input
Read Inputs
BMS_State
BMS_State
BMS_Algorithms
StateReq
CurrPowerLimCalc
DischargeCurrentLimit
ChargeCurrentLimit
MaxCellVolt
MinCellVolt
BMS_Input
CurrPowerLimCalc
State_Machine
StateRequest
DischargeCurrentLimit
ChargeCurrentLimit
MaxCellVolt
MinCellVolt
BMS_Input
ChargeCurrentReq
PosContactorChgrCmd
PreChargeRelayChgrCmd
NegContactorChgrCmd
PosContactorInvtrCmd
PreChargeRelayInvtrCmd
NegContactorInvtrCmd
Faults
BMS_State
BMS_State_Enum
State_Machine
Balancing_Logic
BMS_State
MinCellVolt
MaxCellVolt
BMS_Input
BalCmd
Balancing_Logic
SOC_Estimation
BMS_State
BMS_Input
SOC
SOC_Estimation
BusManagement
DischargeCurrentLimit
ChargeCurrentLimit
ChargeCurrentReq
PosContactorChgrCmd
PreChargeRelayChgrCmd
NegContactorChgrCmd
PosContactorInvtrCmd
PreChargeRelayInvtrCmd
NegContactorInvtrCmd
Faults
BMS_State
BalCmd
SOC
BMS_Output
BMS_Info
Output
BMS_Output
BMS_Info
Update Outputs
Model Data Editor
Code Mappings - C
Ready
View 1 error
100%
FixedStepDiscrete
8:44 PM


Transmit/Receive LED
Debug port connector
S32 Debug Probe
NXP
Top
Pin 1
Run/Pause LED

workspaceS32DS.3.3_a - C/C++ - S32K1/src/main.c - S32 Design Studio for S32 Platform

File Edit Source Refactor Navigate Search Project ConfigTools Run Window Help

Quick Access

Project Explorer

- S32K1: Debug_FLASH
  - Binaries
  - Includes
  - Project_Settings
  - include
    - devassert.h
    - device_registers.h
    - s32_core_cm4.h
    - S32K144_features.h
    - S32K144.h
    - startup.h
    - system_S32K144.h
  - src
    - main.c
  - Debug_FLASH

Dashboard

- Project Creation
  - S32DS Application Project
  - S32DS Library Project
- Build/Debug
  - Build (All)
  - Clean (All)
  - Debug
- Settings
  - Project settings
  - Build settings
  - Debug settings
- Miscellaneous
  - Getting Started
  - Quick access

main.c

```
 * main implementation: use this 'C' sample to create your own application
#include "S32K144.h"

#if defined (__ghs__)
    #define __INTERRUPT_SVC  __interrupt
    #define __NO_RETURN _Pragma("ghs nowarning 111")
#elif defined (__ICCARM__)
    #define __INTERRUPT_SVC  __svc
    #define __NO_RETURN _Pragma("diag_suppress=Pe111")
#elif defined (__GNUC__)
    #define __INTERRUPT_SVC  __attribute__ ((interrupt ("SVC")))
    #define __NO_RETURN
#else
    #define __INTERRUPT_SVC
    #define __NO_RETURN
#endif

int counter, accumulator = 0, limit_value = 1000000;

int main(void) {
    counter = 0;

    for (;;) {
        counter++;

        if (counter >= limit_value) {
            __asm volatile ("svc 0");
            counter = 0;
        }
    }
    /* to avoid the warning message for GHS and IAR: statement is unreachable*/
    __NO_RETURN
    return 0;
}

__INTERRUPT_SVC void SVC_Handler() {
    accumulator += counter;
}
```

Outline | Build Targets

- S32K144.h
- __INTERRUPT_SVC
- __NO_RETURN
- __INTERRUPT_SVC
- __NO_RETURN
- __INTERRUPT_SVC
- __NO_RETURN
- __INTERRUPT_SVC
- __NO_RETURN
- counter : int
- accumulator : int
- limit_value : int
- main(void) : int
- SVC_Handler() : void

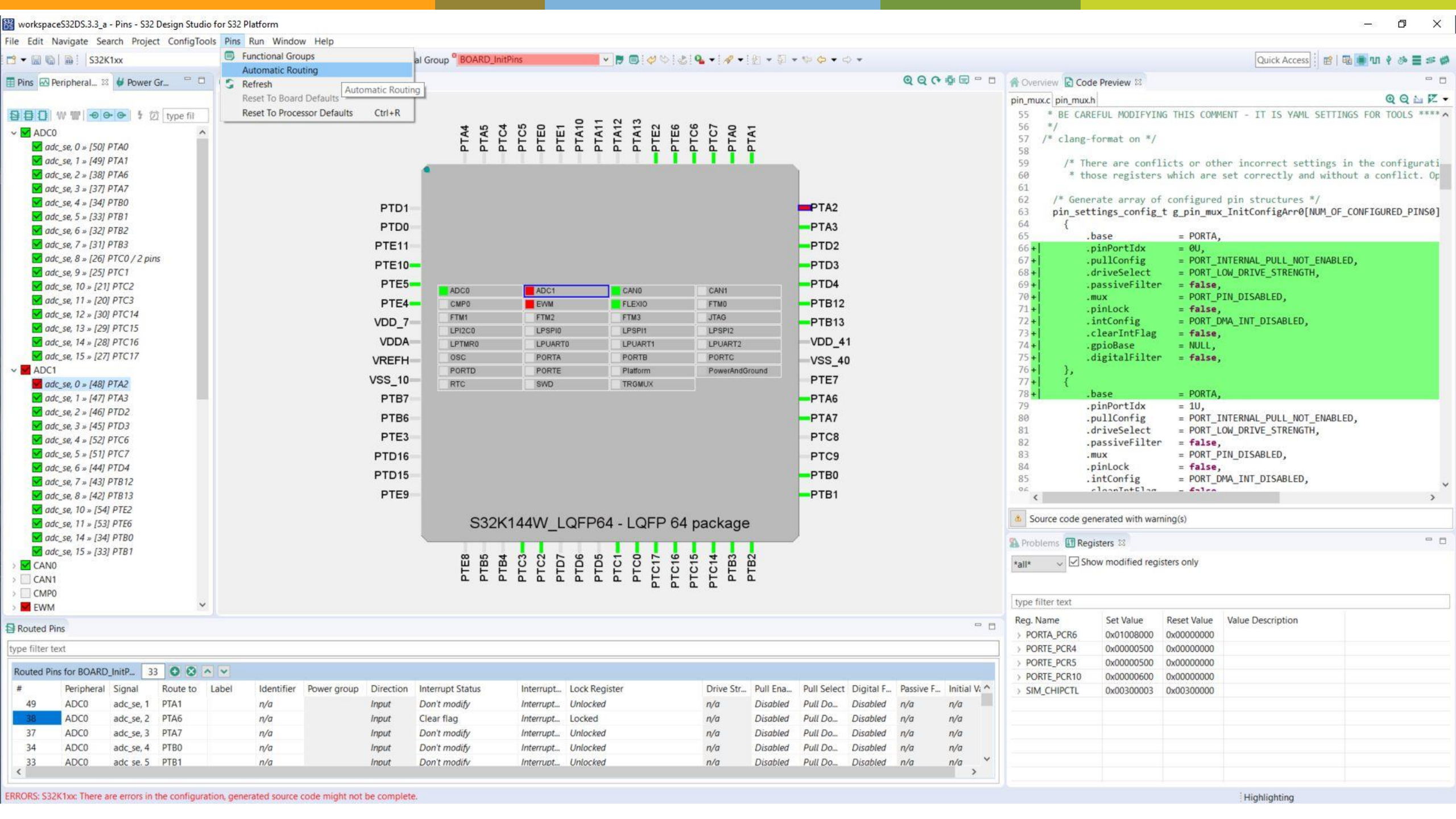
Problems Tasks Console Properties Debug

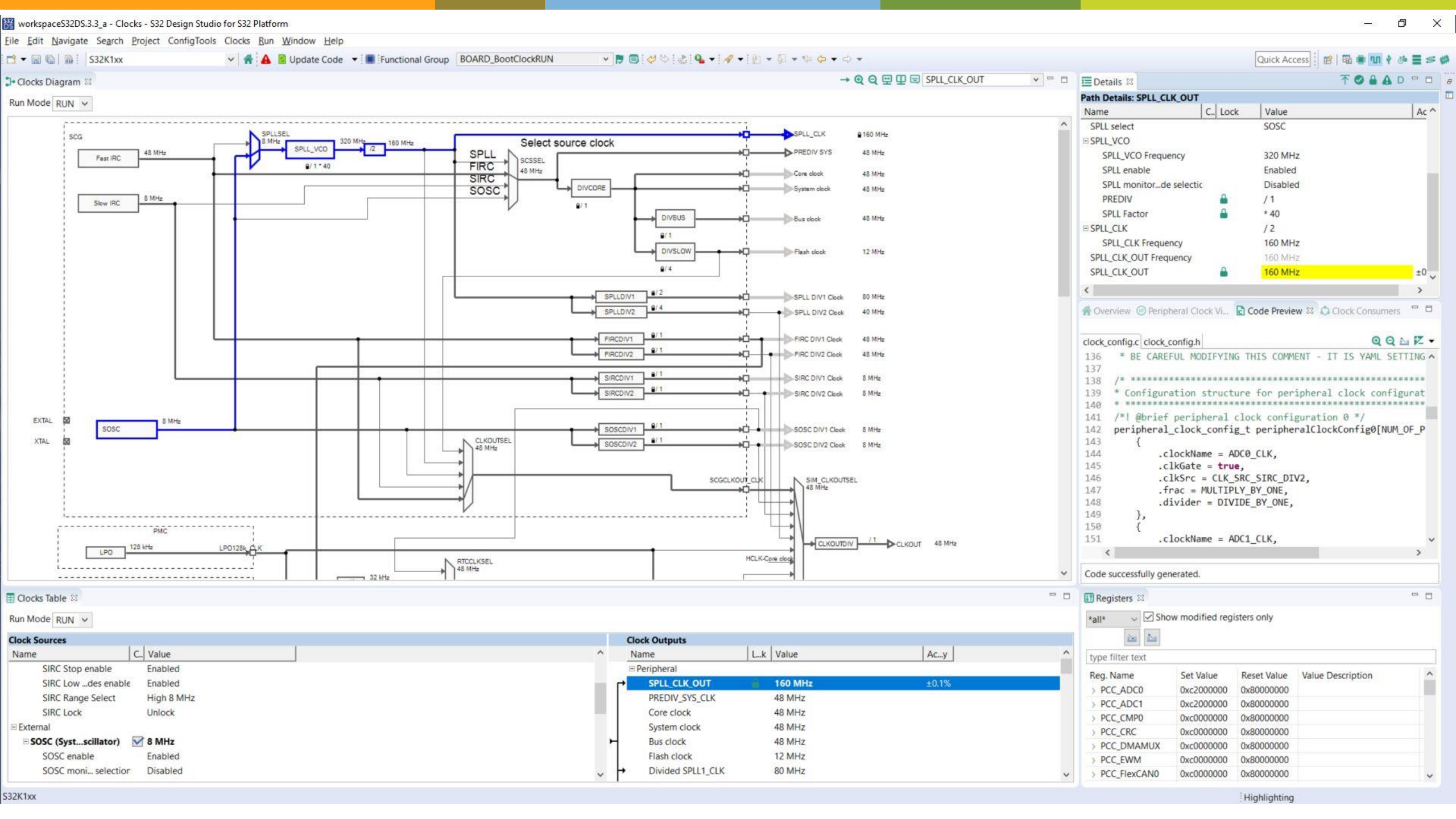
CDT Build Console [S32K1]

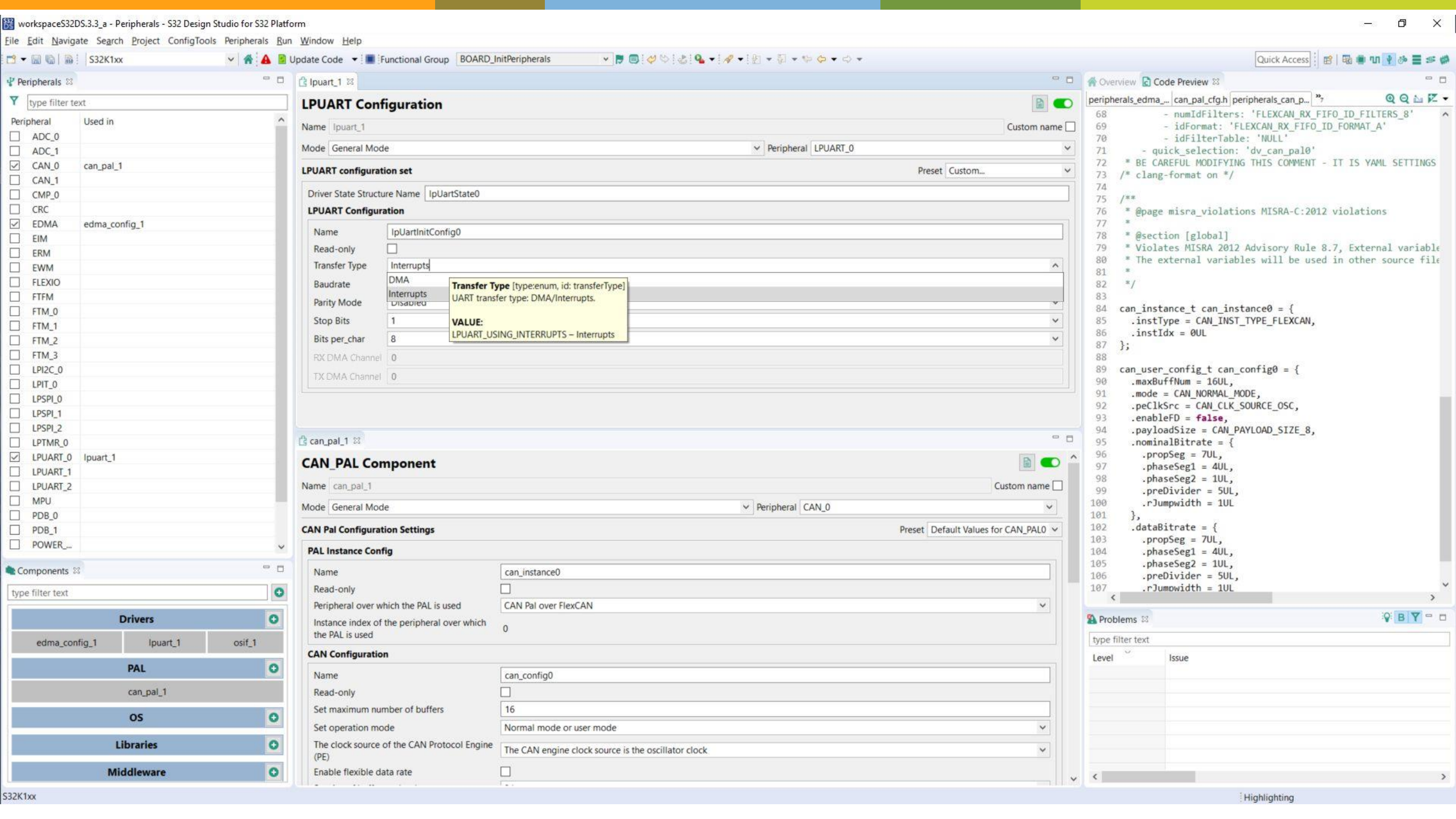
```
Invoking: Standard S32DS Print Size
arm-none-eabi-size --format=berkeley S32K1.elf
   text    data     bss     dec     hex filename
   2340    1068    3112    6520    1978 S32K1.elf
Finished building: S32K1.siz


17:34:50 Build Finished (took 2s.67ms)
```

Highlighting


workspaceS32DS.3.3_a - Pins - S32 Design Studio for S32 Platform
File Edit Navigate Search Project ConfigTools Pins Run Window Help
Functional Groups
Automatic Routing
Refresh
Reset To Board Defaults
Reset To Processor Defaults Ctrl+R
Automatic Routing
BOARD_InitPins
Quick Access
Pins Peripheral... Power Gr...
ADC0
adc_se, 0 » [50] PTA0
adc_se, 1 » [49] PTA1
adc_se, 2 » [38] PTA6
adc_se, 3 » [37] PTA7
adc_se, 4 » [34] PTB0
adc_se, 5 » [33] PTB1
adc_se, 6 » [32] PTB2
adc_se, 7 » [31] PTB3
adc_se, 8 » [26] PTC0 / 2 pins
adc_se, 9 » [25] PTC1
adc_se, 10 » [21] PTC2
adc_se, 11 » [20] PTC3
adc_se, 12 » [30] PTC14
adc_se, 13 » [29] PTC15
adc_se, 14 » [28] PTC16
adc_se, 15 » [27] PTC17
ADC1
adc_se, 0 » [48] PTA2
adc_se, 1 » [47] PTA3
adc_se, 2 » [46] PTD2
adc_se, 3 » [45] PTD3
adc_se, 4 » [52] PTC6
adc_se, 5 » [51] PTC7
adc_se, 6 » [44] PTD4
adc_se, 7 » [43] PTB12
adc_se, 8 » [42] PTB13
adc_se, 10 » [54] PTE2
adc_se, 11 » [53] PTE6
adc_se, 14 » [34] PTB0
adc_se, 15 » [33] PTB1
CAN0
CAN1
CMP0
EWM
PTA4 PTA5 PTC4 PTC5 PTE0 PTE1 PTA10 PTA11 PTA12 PTA13 PTE2 PTE6 PTC6 PTC7 PTA0 PTA1
PTD1 PTD0 PTE11 PTE10 PTE5 PTE4 VDD_7 VDDA VREFH VSS_10 PTB7 PTB6 PTE3 PTD16 PTD15 PTE9
PTA2 PTA3 PTD2 PTD3 PTD4 PTB12 PTB13 VDD_41 VSS_40 PTE7 PTA6 PTA7 PTC8 PTC9 PTB0 PTB1
ADC0 ADC1 CAN0 CAN1
CMP0 EWM FLEXIO FTM0
FTM1 FTM2 FTM3 JTAG
LPI2C0 LPSPI0 LPSPI1 LPSPI2
LPTMR0 LPUART0 LPUART1 LPUART2
OSC PORTA PORTB PORTC
PORTD PORTE Platform PowerAndGround
RTC SWD TRGMUX
S32K144W_LQFP64 - LQFP 64 package
PTE8 PTB5 PTB4 PTC3 PTC2 PTD7 PTD6 PTD5 PTC1 PTC0 PTC17 PTC16 PTC15 PTC14 PTB3 PTB2
Overview Code Preview
pin_mux.c pin_mux.h
* BE CAREFUL MODIFYING THIS COMMENT - IT IS YAML SETTINGS FOR TOOLS ****
*/
/* clang-format on */
/* There are conflicts or other incorrect settings in the configurati
* those registers which are set correctly and without a conflict. Op
/* Generate array of configured pin structures */
pin_settings_config_t g_pin_mux_InitConfigArr0[NUM_OF_CONFIGURED_PINS0]
{
.base = PORTA,
.pinPortIdx = 0U,
.pullConfig = PORT_INTERNAL_PULL_NOT_ENABLED,
.driveSelect = PORT_LOW_DRIVE_STRENGTH,
.passiveFilter = false,
.mux = PORT_PIN_DISABLED,
.pinLock = false,
.intConfig = PORT_DMA_INT_DISABLED,
.clearIntFlag = false,
.gpioBase = NULL,
.digitalFilter = false,
},
{
.base = PORTA,
.pinPortIdx = 1U,
.pullConfig = PORT_INTERNAL_PULL_NOT_ENABLED,
.driveSelect = PORT_LOW_DRIVE_STRENGTH,
.passiveFilter = false,
.mux = PORT_PIN_DISABLED,
.pinLock = false,
.intConfig = PORT_DMA_INT_DISABLED,
Source code generated with warning(s)
Problems Registers
all Show modified registers only
type filter text
Reg. Name Set Value Reset Value Value Description
PORTA_PCR6 0x01008000 0x00000000
PORTE_PCR4 0x00000500 0x00000000
PORTE_PCR5 0x00000500 0x00000000
PORTE_PCR10 0x00000600 0x00000000
SIM_CHIPCTL 0x00300003 0x00300000
Routed Pins
type filter text
Routed Pins for BOARD_InitP... 33
Peripheral Signal Route to Label Identifier Power group Direction Interrupt Status Interrupt... Lock Register Drive Str... Pull Ena... Pull Select Digital F... Passive F... Initial V...
49 ADC0 adc_se, 1 PTA1 n/a Input Don't modify Interrupt... Unlocked n/a Disabled Pull Do... Disabled n/a n/a
38 ADC0 adc_se, 2 PTA6 n/a Input Clear flag Interrupt... Locked n/a Disabled Pull Do... Disabled n/a n/a
37 ADC0 adc_se, 3 PTA7 n/a Input Don't modify Interrupt... Unlocked n/a Disabled Pull Do... Disabled n/a n/a
34 ADC0 adc_se, 4 PTB0 n/a Input Don't modify Interrupt... Unlocked n/a Disabled Pull Do... Disabled n/a n/a
33 ADC0 adc_se, 5 PTB1 n/a Input Don't modify Interrupt... Unlocked n/a Disabled Pull Do... Disabled n/a n/a
ERRORS: S32K1xx: There are errors in the configuration, generated source code might not be complete.
Highlighting


workspaceS32DS.3.3_a - Clocks - S32 Design Studio for S32 Platform
File Edit Navigate Search Project ConfigTools Clocks Run Window Help
S32K1xx
Update Code
Functional Group
BOARD_BootClockRUN
Quick Access
Clocks Diagram
Run Mode RUN
SPLL_CLK_OUT
Select source clock
SPLL
FIRC
SIRC
SOSC
SCG
Fast IRC
48 MHz
Slow IRC
8 MHz
SPLLSEL
8 MHz
SPLL_VCO
320 MHz
/2
160 MHz
/ 1 * 40
SCSSEL
48 MHz
DIVCORE
/ 1
DIVBUS
/ 1
DIVSLOW
/ 4
SPLL_CLK
160 MHz
PREDIV SYS
48 MHz
Core clock
48 MHz
System clock
48 MHz
Bus clock
48 MHz
Flash clock
12 MHz
SPLLDIV1
/ 2
SPLLDIV2
/ 4
SPLL DIV1 Clock
80 MHz
SPLL DIV2 Clock
40 MHz
FIRCDIV1
FIRCDIV2
FIRC DIV1 Clock
48 MHz
FIRC DIV2 Clock
48 MHz
SIRCDIV1
SIRCDIV2
SIRC DIV1 Clock
8 MHz
SIRC DIV2 Clock
8 MHz
EXTAL
XTAL
SOSC
8 MHz
SOSCDIV1
SOSCDIV2
SOSC DIV1 Clock
8 MHz
SOSC DIV2 Clock
8 MHz
CLKOUTSEL
48 MHz
SCGCLKOUT_CLK
SIM_CLKOUTSEL
48 MHz
CLKOUTDIV
/ 1
CLKOUT
48 MHz
PMC
LPO
128 kHz
LPO128k_CLK
RTCCLKSEL
48 MHz
HCLK-Core clock
32 kHz
Details
Path Details: SPLL_CLK_OUT
Name
C..
Lock
Value
SPLL select
SOSC
SPLL_VCO
SPLL_VCO Frequency
320 MHz
SPLL enable
Enabled
SPLL monitor...de selectic
Disabled
PREDIV
/ 1
SPLL Factor
* 40
SPLL_CLK
/ 2
SPLL_CLK Frequency
160 MHz
SPLL_CLK_OUT Frequency
160 MHz
SPLL_CLK_OUT
160 MHz
Overview
Peripheral Clock Vi...
Code Preview
Clock Consumers
clock_config.c
clock_config.h
136 * BE CAREFUL MODIFYING THIS COMMENT - IT IS YAML SETTING
137
138 /* ***
139 * Configuration structure for peripheral clock configurat
140 * ***
141 /*! @brief peripheral clock configuration 0 */
142 peripheral_clock_config_t peripheralClockConfig0[NUM_OF_P
143 {
144 .clockName = ADC0_CLK,
145 .clkGate = true,
146 .clkSrc = CLK_SRC_SIRC_DIV2,
147 .frac = MULTIPLY_BY_ONE,
148 .divider = DIVIDE_BY_ONE,
149 },
150 {
151 .clockName = ADC1_CLK,
Code successfully generated.
Clocks Table
Run Mode RUN
Clock Sources
Name
C..
Value
SIRC Stop enable
Enabled
SIRC Low ...des enable
Enabled
SIRC Range Select
High 8 MHz
SIRC Lock
Unlock
External
SOSC (Syst...scillator)
8 MHz
SOSC enable
Enabled
SOSC moni... selectior
Disabled
Clock Outputs
Name
L...k
Value
Ac...y
Peripheral
SPLL_CLK_OUT
160 MHz
±0.1%
PREDIV_SYS_CLK
48 MHz
Core clock
48 MHz
System clock
48 MHz
Bus clock
48 MHz
Flash clock
12 MHz
Divided SPLL1_CLK
80 MHz
Registers
all
Show modified registers only
type filter text
Reg. Name
Set Value
Reset Value
Value Description
PCC_ADC0
0xc2000000
0x80000000
PCC_ADC1
0xc2000000
0x80000000
PCC_CMP0
0xc0000000
0x80000000
PCC_CRC
0xc0000000
0x80000000
PCC_DMAMUX
0xc0000000
0x80000000
PCC_EWM
0xc0000000
0x80000000
PCC_FlexCAN0
0xc0000000
0x80000000
S32K1xx
Highlighting


workspaceS32DS.3.3_a - Peripherals - S32 Design Studio for S32 Platform
File Edit Navigate Search Project ConfigTools Peripherals Run Window Help
S32K1xx
Update Code
Functional Group
BOARD_InitPeripherals
Quick Access
Peripherals
type filter text
Peripheral
Used in
ADC_0
ADC_1
CAN_0
can_pal_1
CAN_1
CMP_0
CRC
EDMA
edma_config_1
EIM
ERM
EWM
FLEXIO
FTFM
FTM_0
FTM_1
FTM_2
FTM_3
LPI2C_0
LPIT_0
LPSPI_0
LPSPI_1
LPSPI_2
LPTMR_0
LPUART_0
lpuart_1
LPUART_1
LPUART_2
MPU
PDB_0
PDB_1
POWER_...
Components
type filter text
Drivers
edma_config_1
lpuart_1
osif_1
PAL
can_pal_1
OS
Libraries
Middleware
lpuart_1
LPUART Configuration
Name lpuart_1
Custom name
Mode General Mode
Peripheral LPUART_0
LPUART configuration set
Preset Custom...
Driver State Structure Name lpUartState0
LPUART Configuration
Name lpUartInitConfig0
Read-only
Transfer Type Interrupts
Baudrate
DMA
Interrupts
Transfer Type [type:enum, id: transferType]
UART transfer type: DMA/Interrupts.
VALUE:
LPUART_USING_INTERRUPTS – Interrupts
Parity Mode
Stop Bits 1
Bits per_char 8
RX DMA Channel 0
TX DMA Channel 0
can_pal_1
CAN_PAL Component
Name can_pal_1
Custom name
Mode General Mode
Peripheral CAN_0
CAN Pal Configuration Settings
Preset Default Values for CAN_PAL0
PAL Instance Config
Name can_instance0
Read-only
Peripheral over which the PAL is used
CAN Pal over FlexCAN
Instance index of the peripheral over which the PAL is used
0
CAN Configuration
Name can_config0
Read-only
Set maximum number of buffers
16
Set operation mode
Normal mode or user mode
The clock source of the CAN Protocol Engine (PE)
The CAN engine clock source is the oscillator clock
Enable flexible data rate
Overview
Code Preview
peripherals_edma_...
can_pal_cfg.h
peripherals_can_p...
- numIdFilters: 'FLEXCAN_RX_FIFO_ID_FILTERS_8'
- idFormat: 'FLEXCAN_RX_FIFO_ID_FORMAT_A'
- idFilterTable: 'NULL'
- quick_selection: 'dv_can_pal0'
* BE CAREFUL MODIFYING THIS COMMENT - IT IS YAML SETTINGS
/* clang-format on */
/**
* @page misra_violations MISRA-C:2012 violations
*
* @section [global]
* Violates MISRA 2012 Advisory Rule 8.7, External variable
* The external variables will be used in other source file
*
*/
can_instance_t can_instance0 = {
.instType = CAN_INST_TYPE_FLEXCAN,
.instIdx = 0UL
};
can_user_config_t can_config0 = {
.maxBuffNum = 16UL,
.mode = CAN_NORMAL_MODE,
.peClkSrc = CAN_CLK_SOURCE_OSC,
.enableFD = false,
.payloadSize = CAN_PAYLOAD_SIZE_8,
.nominalBitrate = {
.propSeg = 7UL,
.phaseSeg1 = 4UL,
.phaseSeg2 = 1UL,
.preDivider = 5UL,
.rJumpwidth = 1UL
},
.dataBitrate = {
.propSeg = 7UL,
.phaseSeg1 = 4UL,
.phaseSeg2 = 1UL,
.preDivider = 5UL,
.rJumpwidth = 1UL
Problems
type filter text
Level
Issue
S32K1xx
Highlighting