

# MATLAB EXPO

## 2021

**Low Cost 5G Test Bed for the Futuristic 6G  
Research**



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# Agenda

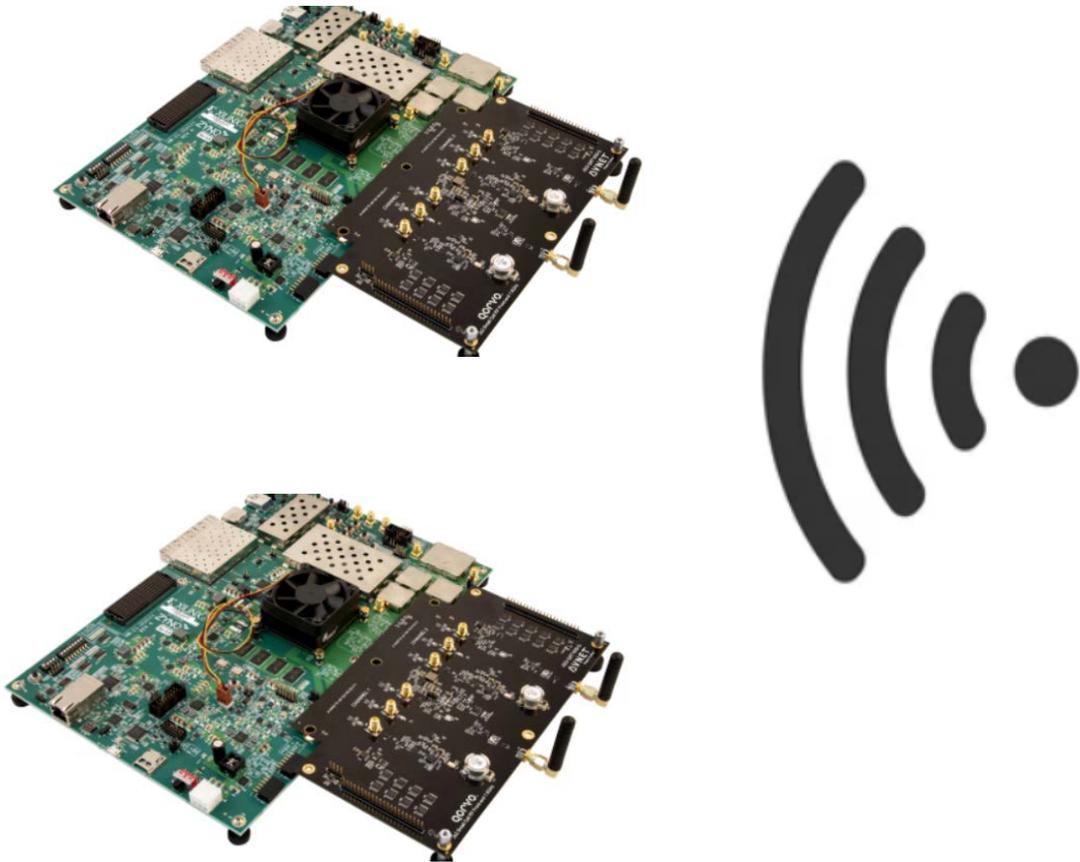
- **Introduction**
- **Overview of 5G Testbed System**
- **Challenges and Approach to implement 5G Testbed System**
- **MATLAB Simulation Results and Analysis**
- **Future scope of Work**
- **Summary and Conclusion**

# IIT Kharagpur

- Indian Institute of Technology, Kharagpur is the first IIT established in India in May 1950 by an act of Indian Parliament.
- This is the one of the most premier educational institute of science and technology in India and the world.
- Currently, it houses more than 40 Departments, Schools, Centers and offers B.Tech, M.Tech, M.S, PhD degrees.
- With more than 750 faculties and 15,000 students at present in a sprawling green campus on ~2200 acres of land, this is also one of most prestigious institute of research in the world.

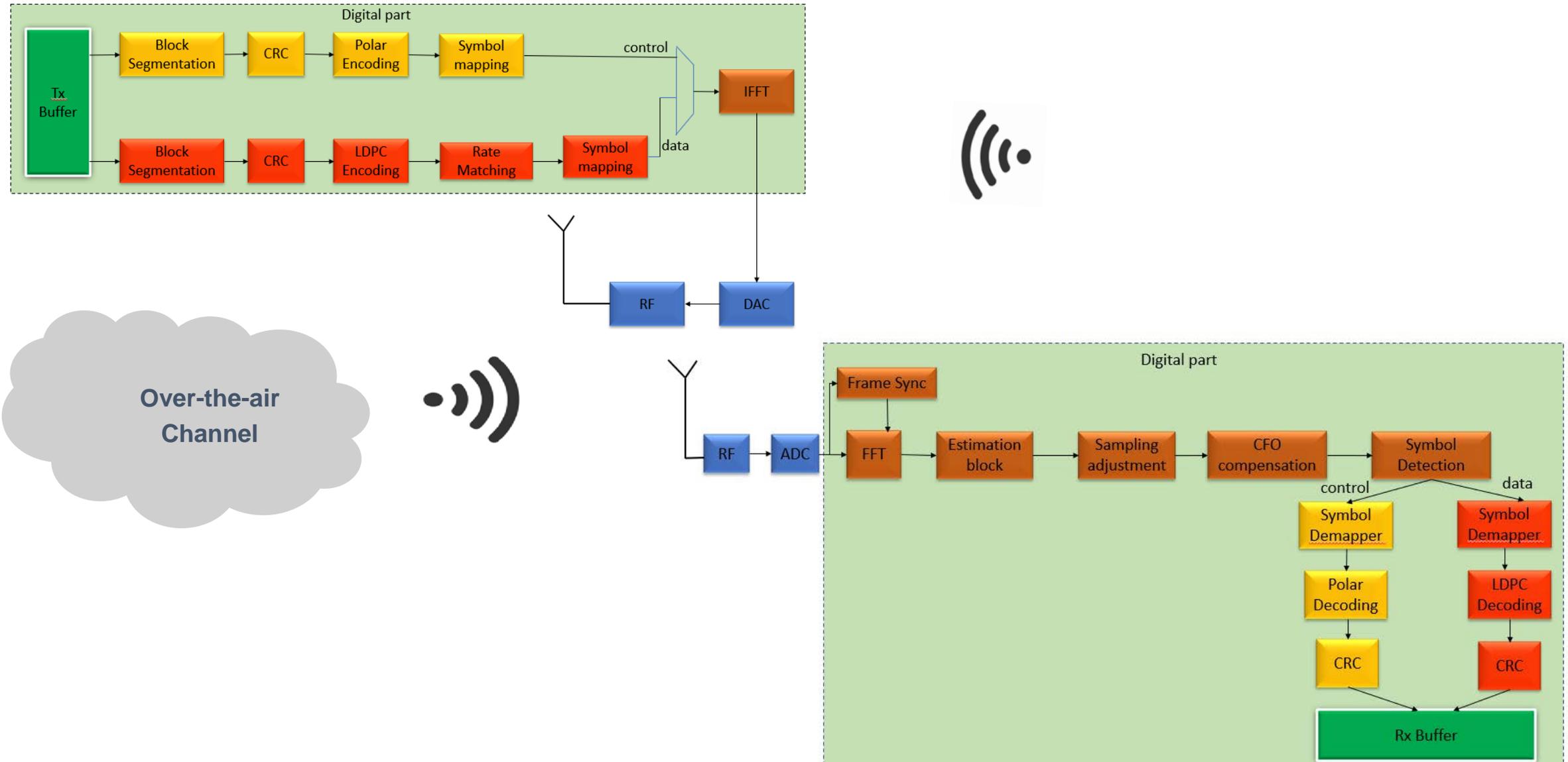


# Overview of 5G Testbed System



- This is an end-to-end 5G cellular standard testbed development project on FPGA platforms compliant to 3GPP Rel-16.
- Contains one base station (gNB) and one user equipment (UE) with complete RF support in sub-6Ghz range.
- It contains PHY with 6G research.
- A low-cost testbed with single antenna at Phase I and MIMO in Phase-II
- Funded through IIT Kharagpur by Govt. of India under ISIRD scheme and SERB.
- The modem is being co-developed as part of an IIT KGP incubated Start-up “VORAI SEMICONDUCTOR Pvt. Ltd.”

# Details of Transceiver Requirement



# Challenges



Change in technology  
requires change on  
methodology

- Requires a flexible development environment
- Change in architecture involves reprogramming

Programming and  
Verification Expertise

- Proficiency in HDL programming
- Dedicated team to write verification Test benches
- Late detection of errors

Reuse the IP

- Can I create reusable IPs for other projects?

Verification of the  
Design

- How to do functional verification with Hardware?

Fast Prototype

- Can I create a working prototype with small team?

# Proposed Approach



Change in technology  
requires change on  
methodology

- Use 5G toolbox for standard compliant waveform generation & PHY Layer signal chains

Programming and  
Verification Expertise

- Autogenerate synthesizable VHDL code and testbench for verification using HDL Coder and HDL Verifier

Reuse the IP

- Leverage existing HDL IP in Wireless HDL Toolbox
- Customize IPs for further reuse

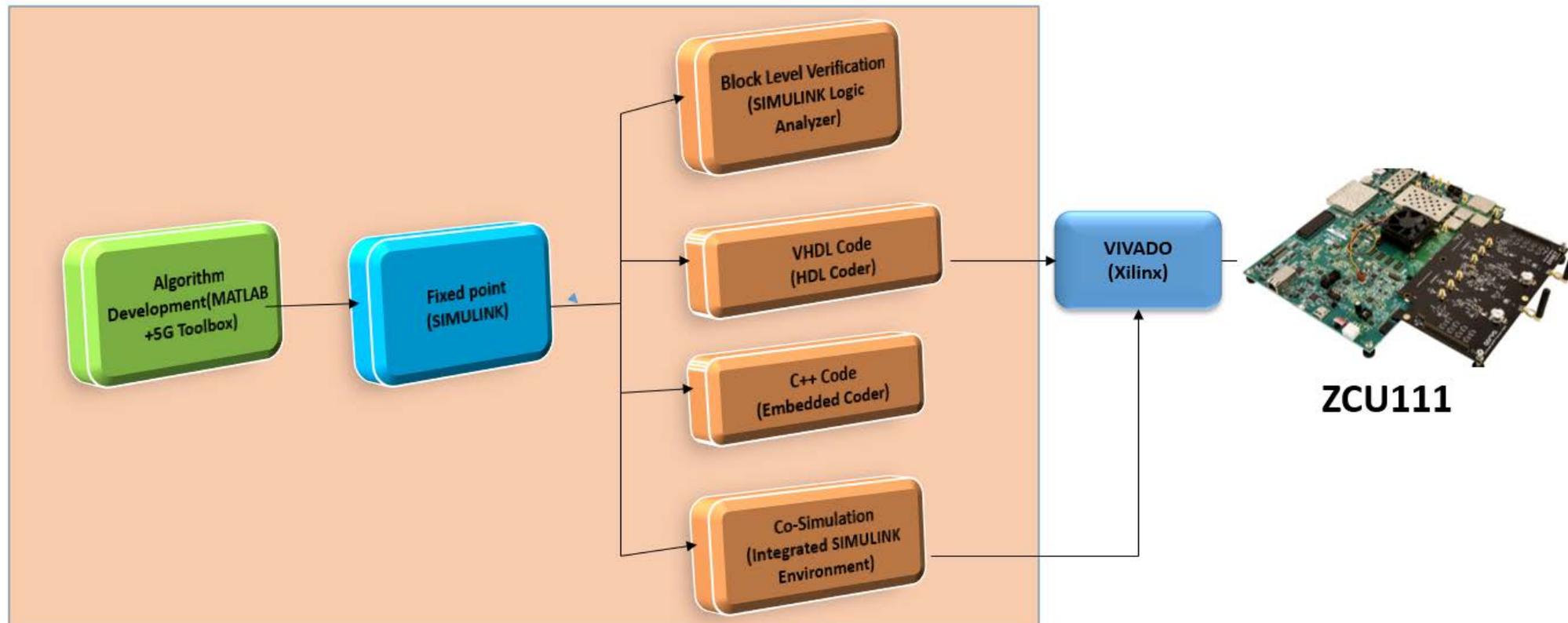
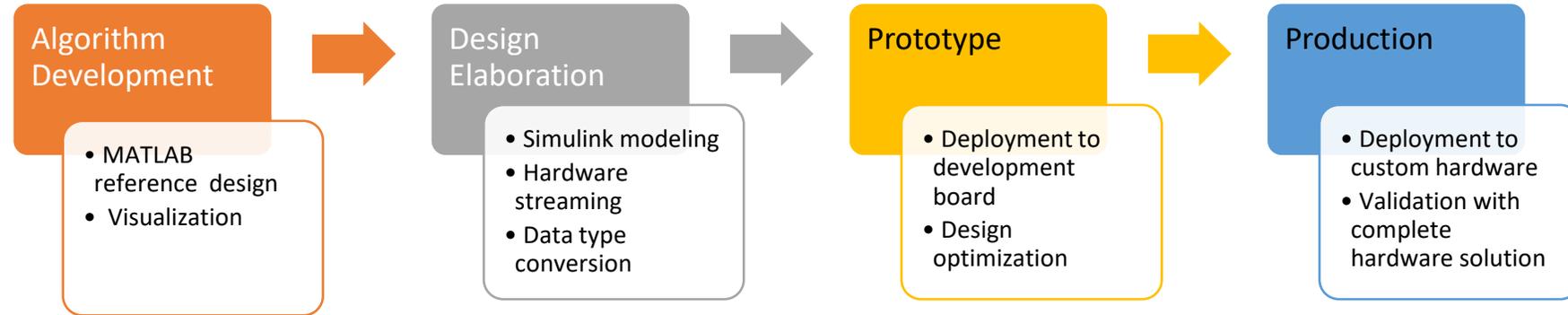
Verification of the  
Design

- Validating the subsystems at system level
- Over the air testing with Qorvo RF frontend.
- RTL Co-simulation and FPGA in the loop verification

Fast Prototype

- Rapid prototyping & hardware deployment

# Design & Verification Approach



# MATLAB Demo: Block Level Simulation with Simulink Logic Analyzer (IFFT with Test bench)

The image displays the MATLAB R2020a environment with a Simulink test bench script open in the Editor. The script, named 'Top\_Tx\_Rx.m', is located at 'D:\Projects\Samsung\_TV\5G\_TX\_RX\TB\Data\_generation\TB\_TOP\Top\_Tx\_Rx.m'. The script contains the following code:

```
1 % This is the TOP TB
2 % Amit Dutta
3 % Date : 25-2-2021
4
5 % Parameters %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
6 clear all;
7
8 sigma_h = 0.1; % PSD for channel coefficient
9 SNR = (0:2:20); % SNR in dB
10 plot_control = 4;
11 Data_length = 5000; % # of ADC samples
12 Fs = 44100;%2e+6;% Sampling frequency at the ADC
13 Fc = 0.2; % Normalized frequency Fc in Hz = Fc*Fs/2;
14 ADC_len = 16; % This is the ADC length
15 Resolution = 10000;
16 pilot_bin_len = 200000; % length of pilot data in binary form
```

The Command Window shows the execution of the script:

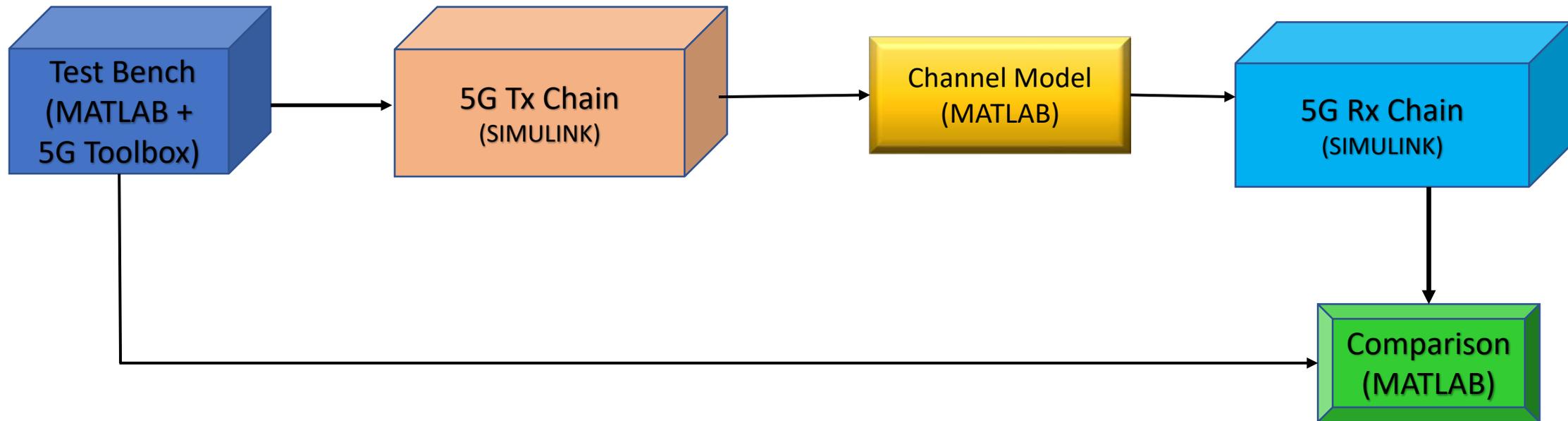
```
>> Top_Tx_Rx
fx >>
```

The Workspace window on the right lists various variables and parameters, including:

- Fs
- h
- h\_est
- i
- ITR\_LIMIT
- l
- L
- M
- mu
- n
- N
- out
- pilot\_bin\_len
- pilot\_interv
- plot\_control
- power\_control
- r
- Resolution
- rx
- rx\_comp
- S
- S\_cons
- sample\_rate
- sigma\_h
- sigma\_noise
- sigma\_x
- sn
- SNR
- TERM\_LIMIT
- vec\_CFO
- vec\_CFO\_correction
- w
- x\_cor\_sym
- x\_dec\_bin
- x\_dec\_bin
- x\_dec\_bin
- xbin
- xbin\_pilot
- xbin\_reshape
- xbin\_reshape
- xsym
- xsym\_data
- xsym\_data
- xsym\_pilot
- xsym\_tx

# End-to-End System validation

- ✓ The overall system validation diagram



# MATLAB Demo

The screenshot displays the MATLAB R2020a interface. The main window shows a script editor with the following code:

```
1 % This is the TOP TB
2 % Amit Dutta
3 % Date : 25-2-2021
4
5 % Parameters %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
6 clear all;
7
8 sigma_h = 0.1; % PSD for channel coefficient
9 SNR = (0:2:20); % SNR in dB
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11 Data_length = 5000; % # of ADC samples
12 Fs = 44100;%2e+6;% Sampling frequency at the ADC
13 Fc = 0.2; % Normalized frequency Fc in Hz = Fc*Fs/2;
14 ADC_len = 16; % This is the ADC length
15 Resolution = 10000;
16 pilot_bin_len = 200000; % length of pilot data in binary form
17 pilot_interval = 10;
```

The Command Window shows the following commands and their outputs:

```
% Define the general CDL/TDL propagation channel parameters
simParameters.DelayProfile = 'CDL-C'; % Use CDL-C model (Urban macrocell model)
simParameters.DelaySpread = 300e-9;
simParameters.MaximumDopplerShift = 5;

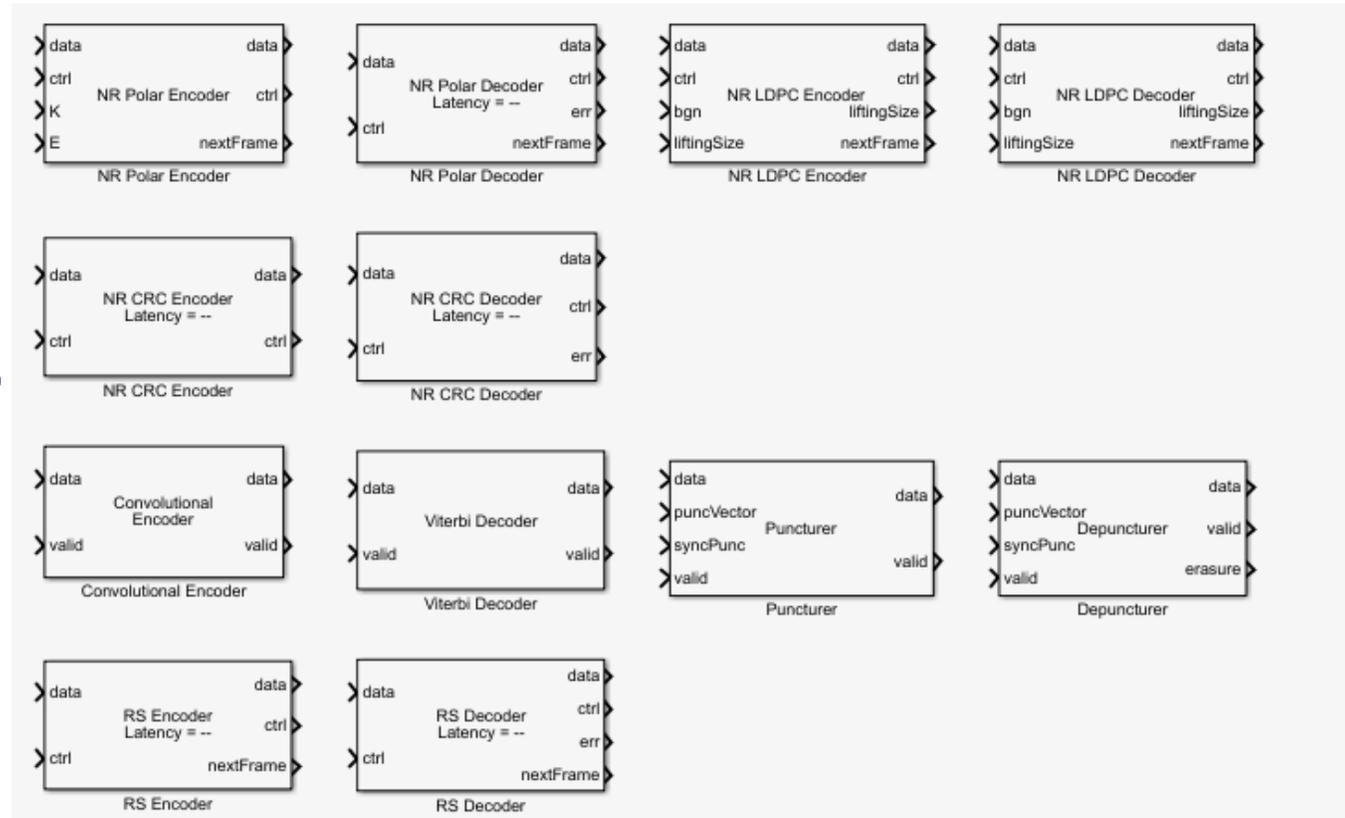
% Cross-check the PDSCH layering against the channel geometry
>>
>> Top_Tx_Rx
>> Top_Tx_Rx
fx >>
```

The Workspace window on the right shows the following variables and their values:

Name	Value
adc_data	1x5000 double
ADC_len	16
Audio_clip_len	2
BER	1x17 double
best_index	12
CFO	-2.2830e-09
CFO_est	3.8363e-09
Data_length	5000
data_segment	2000
error_count	1x17 double
Fc	0.2000
Fs	44100
h	0.0547 - 0.2476i
h_est	0.0384 - 0.1541i
i	2000
ITR_LIMIT	20
l	2000
L	80000
M	16
mu	0.0100
n	10
N	128
pilot_bin_len	200000
pilot_interval	10
plot_control	4
power_cons	10
r	1.6093 - 1.4699i
REF	0
Resolution	10000
rx	1x17 complex double
rx_compensated	1x17 complex double
S	1x16 complex double
S_cons	1x16 complex double
sample_dec	1x5000 double
sigma_h	0.1000
sigma_noise	1x17 double
sigma_x	1
sn	11
SNR	1x17 double
TERM_LIMIT	1.0000e-03
vec_CFO	1x17 complex double
vec_CFO_com	1x17 complex double
w	1x17 complex double
x_cor_sym	0.9487 - 0.9487i
x_dec_bin	'1011'

# Wireless HDL Toolbox- Hardware Optimized HDL IPs

- **FFT**
- **IFFT**
- **Memory**
- **Symbol Mapper/Demapper**
- **Polar Encoder/Decoder**
- **LDPC Encoder/Decoder**
- **CRC blocks**

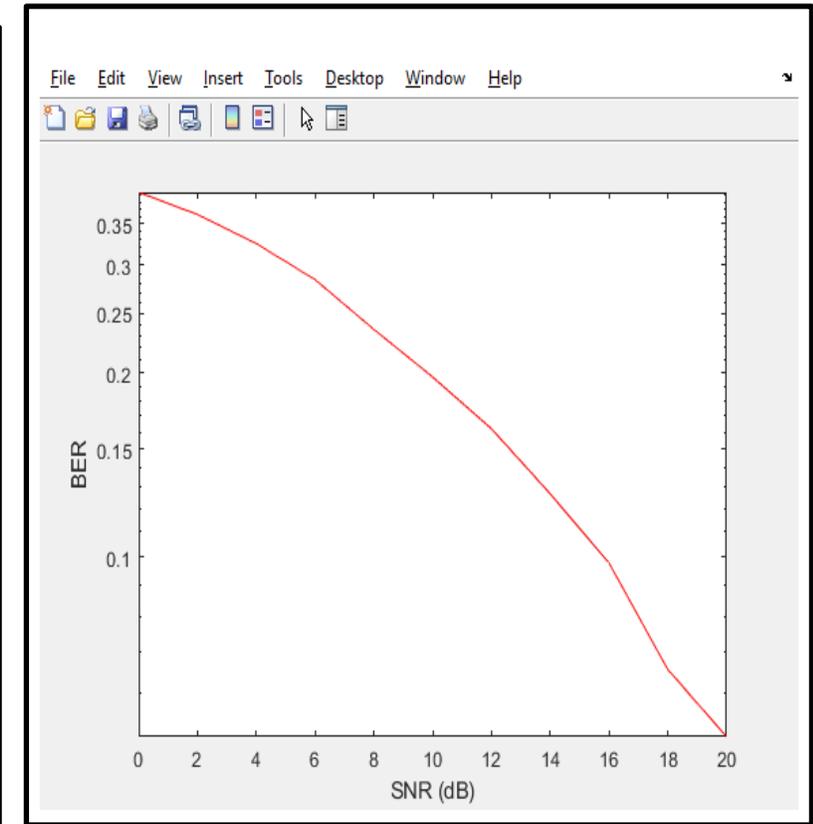
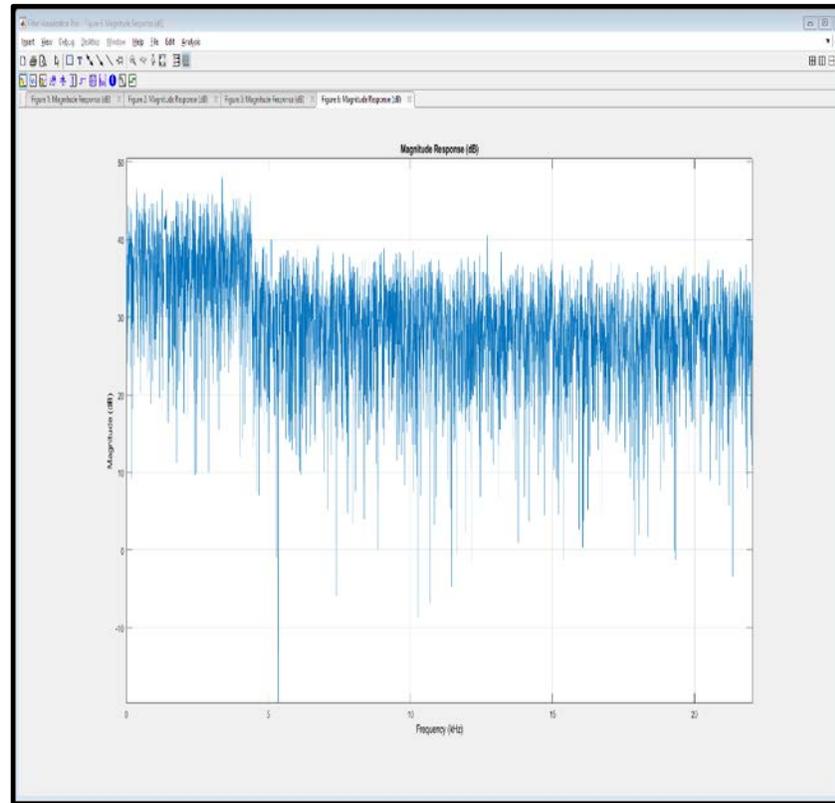
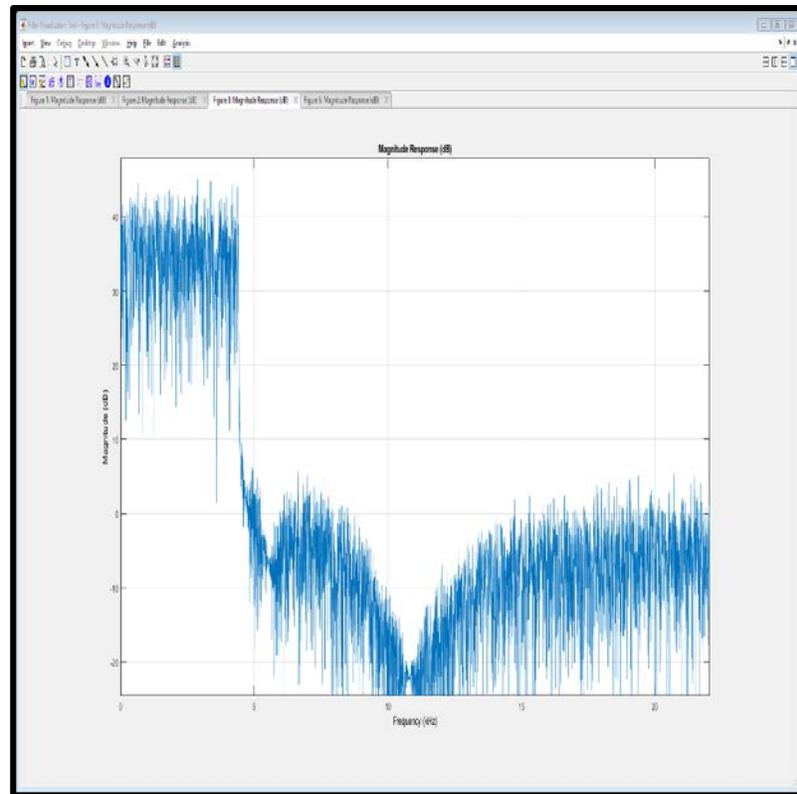


# Achieved Results with 5G Tx-Rx Chain

## Tx Spectrum

## Rx Spectrum

## BER generated curve



# RTL and Synthesis Results- Component Level

The screenshot displays the Design Timing Summary tool interface. The main window is titled "Design Timing Summary" and contains several panels:

- Objects:** A table listing various signals and their properties.
- Processes (Active):** A table listing active processes.
- Wave - Default:** A timing diagram showing signal transitions over time.

**Objects Table:**

Name	Value	KI	Now	In/Out
clk	1'h0			Net In
reset	1'h0			Net In
clk_enable	1'h1			Net In
EN	1'h0			Net In
WE_in	1'h0			Net In
Symbol_data_in_re	16'h0...			Net In
Symbol_data_in_im	16'h0...			Net In
Symbol_write_addr...	18'h0...			Net In
RESET_1	1'h0			Net In
ce_out	1'h1			Net Out
IFFT_data_out_re	16'hff94			Net Out
IFFT_data_out_im	16'hffd3			Net Out
IFFT_other_valid...	1'h1			Net Out
IFFT_PSS_valid_ou...	1'h0			Net Out
IFFT other end	1'h0			Net Out

**Processes (Active) Table:**

Name	Type (filtered)	State
[Empty list]		

**Wave - Default Table:**

Signal	Value
/TOP_IFFT/clk	1'h0
/TOP_IFFT/reset	1'h0
/TOP_IFFT/clk_enable	1'h1
/TOP_IFFT/EN	1'h0
/TOP_IFFT/WE_in	1'h1
/TOP_IFFT/Symbol_data_in_re	16'h...
/TOP_IFFT/Symbol_data_in_im	16'h...
/TOP_IFFT/Symbol_write_address	18'h...
/TOP_IFFT/RESET_1	1'h0
/TOP_IFFT/ce_out	1'h1
/TOP_IFFT/IFFT_data_out_re	16'h...
/TOP_IFFT/IFFT_data_out_im	16'h...
/TOP_IFFT/IFFT_other_valid_out	1'h0
/TOP_IFFT/IFFT_PSS_valid_out	1'h0
/TOP_IFFT/IFFT_other_end	1'h0
/TOP_IFFT/IFFT_PSS_end	1'h0
/TOP_IFFT/IFFT_other_start	1'h0
/TOP_IFFT/IFFT_PSS_start	1'h0
/TOP_IFFT/IFFT_data_WE_out	1'h0
/TOP_IFFT/End_of_iftt	1'h0

**Timing Diagram:** The diagram shows a series of signal transitions over time. The x-axis represents time in nanoseconds (ns), ranging from 232500 ns to 236000 ns. The y-axis represents the signal values. The diagram shows a sequence of signals, including /TOP\_IFFT/clk, /TOP\_IFFT/reset, /TOP\_IFFT/clk\_enable, /TOP\_IFFT/EN, /TOP\_IFFT/WE\_in, /TOP\_IFFT/Symbol\_data\_in\_re, /TOP\_IFFT/Symbol\_data\_in\_im, /TOP\_IFFT/Symbol\_write\_address, /TOP\_IFFT/RESET\_1, /TOP\_IFFT/ce\_out, /TOP\_IFFT/IFFT\_data\_out\_re, /TOP\_IFFT/IFFT\_data\_out\_im, /TOP\_IFFT/IFFT\_other\_valid\_out, /TOP\_IFFT/IFFT\_PSS\_valid\_out, /TOP\_IFFT/IFFT\_other\_end, /TOP\_IFFT/IFFT\_PSS\_end, /TOP\_IFFT/IFFT\_other\_start, /TOP\_IFFT/IFFT\_PSS\_start, /TOP\_IFFT/IFFT\_data\_WE\_out, and /TOP\_IFFT/End\_of\_iftt.

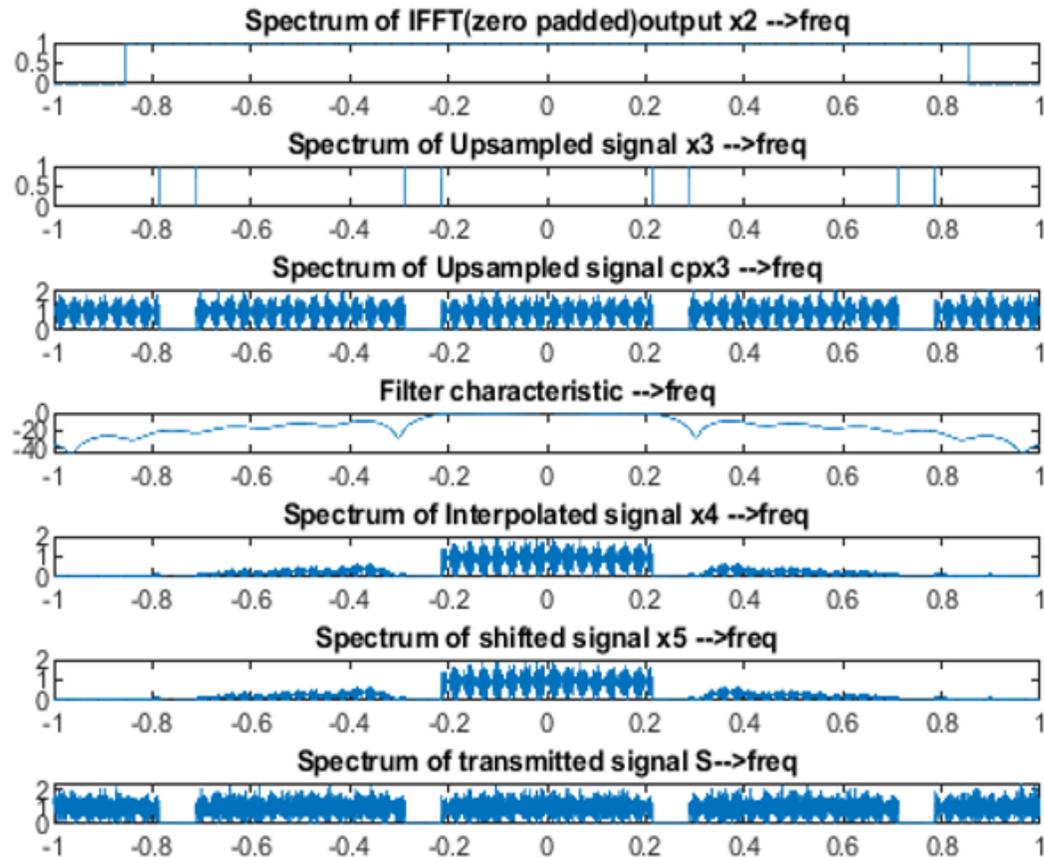
**Bottom Panel:** The bottom panel shows the status of the design, including "Ready", "Sample based", and "T=27362.000".

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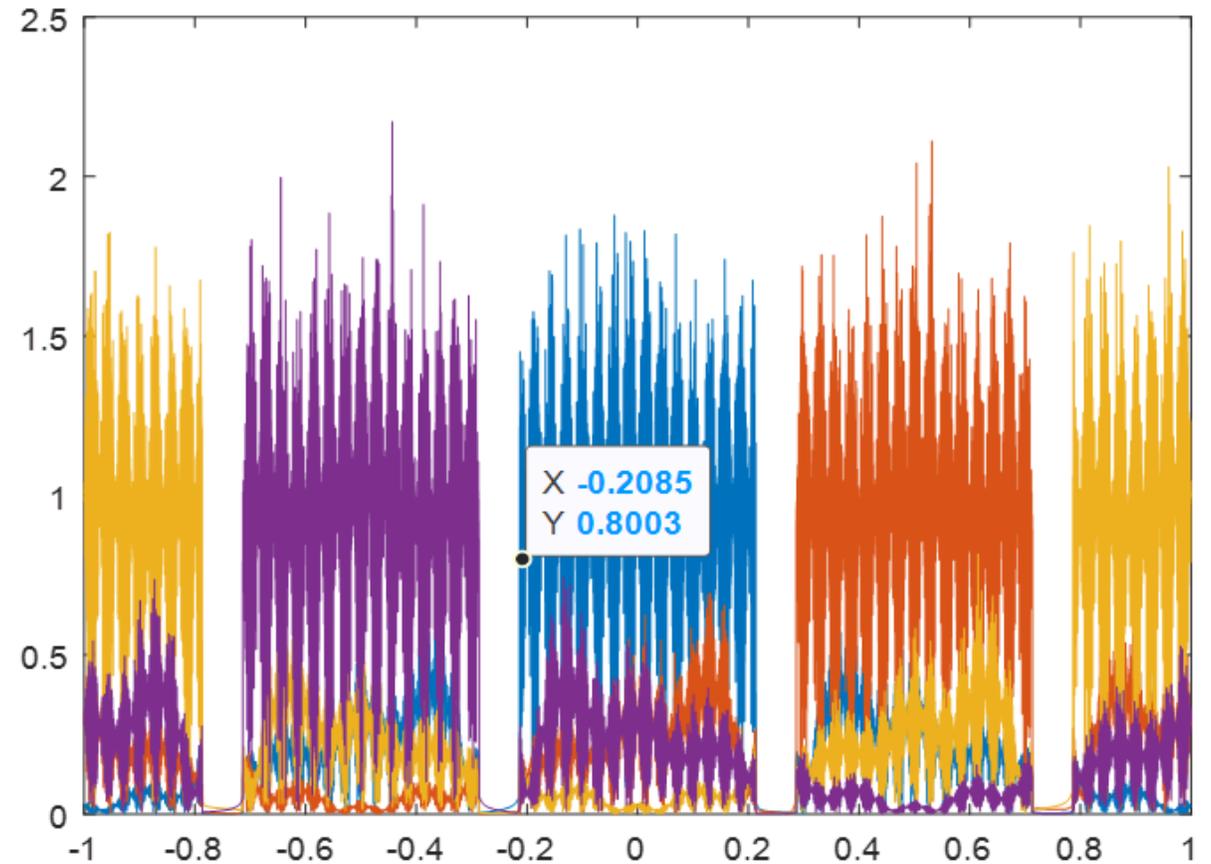
# Future Scope of Work (6G components)

- ✓ Apart from the standard 3GPP Rel-16 components, we also plan to add few futuristic modules planned for 6G.
- ✓ **THz beamforming:** There will be a special module for pencil beamforming targeted for THz signal.
- ✓ **New waveform:** There will a waveform module based on the Filter bank to counter the THz **large bandwidth** effect.

# THz Channel Modeling and Results



Tx spectrum



Rx spectrum

Source: THz related current work from Dr. Amit Kumar Dutta, Ankam Madhusree, IIT KGP

# Summary and Conclusion

- ✓ **5G Toolbox standard compliant built-in functions and Wireless HDL Toolbox hardware optimized IPs helped us in quick validation of 3GPP 5G NR physical layer signal chains.**
- ✓ **Using complete Model-Based Design approach with MATLAB and Simulink helped us to bridge the gap between system engineers and hardware designers.**
- ✓ **The indigenous developed 5G testbed system is scalable and 6G algorithms can be easily plugged into it for testing**
- ✓ **The Tx-Rx system can be used as any commercial Modem.**
- ✓ **The developed test bed can be used for validating various subsystems by different institutions and startups.**

# MATLAB EXPO

## 2021

Thank you

