MATLAB EXPO 2019

Wired Communications Systems Modeling and Analysis

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What’s Covered

- Introduction to SerDes Design and Signal Integrity Analysis
- Using SerDes Toolbox for System-Level Design and Analysis
- Automatic Generation of Standard Compliant IBIS-AMI Models
- SerDes Verification Using Channel Simulators
Introduction to SerDes Design and Signal Integrity Analysis
What is Signal Integrity?

Digital (ideal) signal

Real Signal
Typical SerDes Design Workflow

1. Time-domain characterization of the channel
2. Design of analog and digital equalizers
3. Simulation of the system performance in the time domain
4. Hardware implementation and IP verification
5. IBIS-AMI model generation and SerDes system verification
A Typical SerDes System: TX, RX, and Channel
SerDes Design and Verification Challenges

- Difficult architectural trade-offs
- Slow design iterations
- Disconnected teams

Accurate channel model
Time consuming model creation
Limited correlation
Large data analysis
System-Level Design and Analysis Leads to Continuous Verification

Rapid system analysis

Multi-domain simulation

Rapid design iterations

Easier analog modeling

Integrated specification

Improved team communication

ANALOG & DIGITAL DESIGN

SPECIFICATION / CHANNEL MODEL

IMPLEMENTATION

PROTOTYPE / INTEGRATION

VHDL, Verilog

Spice-like

IBIS-AMI MODEL GENERATION / TEST & VERIFICATION

Improved team communication

Rapid system analysis

Multi-domain simulation

Rapid design iterations

Easier analog modeling

Integrated specification

Improved team communication
Shifting-Left

Where Errors are Introduced… and Detected

Shift-left Verification

- Specification: 60%
- Design: 21%
- Implement: 15%
- Test: 7%

Increased Modelling & Simulation

Traditional Verification

Clive Maxfield and Kuhoo Goyal
“EDA: Where Electronics Begins”
Save 30% of Overall Development Time (and improve quality, reduce re-spins, etc.)

EE Times - Top-down verification guides mixed-signal designs


“In order to address these challenges, many design teams are either looking to, or else have already implemented, a top-down design methodology. In a top-down approach, the architecture of the chip is defined as a block diagram and simulated and optimized using a system simulator such as MATLAB or Simulink. From the high-level simulation, requirements for the individual circuit blocks are derived.”
What’s New

R2019a

SerDes Toolbox

Integration with IC design tools and channel simulators

SPECIFICATION

ANALOG & DIGITAL DESIGN

IMPLEMENTATION

VHDL, Verilog

IMPLEMENTATION

Spice-like

PROTOTYPE / INTEGRATION
SerDes Toolbox

Design SerDes systems and generate IBIS-AMI models for high-speed digital interconnects

- Design and analyze transmitters and receivers with the SerDes Designer app
- Develop equalization algorithms with MATLAB System objects and Simulink blocks
  - FFE, DFE, AGC, CDR, CTLE, etc...
- Perform SerDes statistical analysis and time-domain simulation
- Generate dual IBIS-AMI models for 3rd party channel simulators
- Use reference designs for high-speed links such as Ethernet CEI-56G, DDR5, PCI-Gen4, USB3.1
SerDes Designer app: No Need to be a SerDes Expert

- Design and analyze SerDes systems including transmitters and receivers with arbitrary configuration
- Use parameterized building blocks
- Perform statistical analysis: eye diagram, BER, bathtub, pulse response....
SerDes Design: Where to Start?

- Modulation
- Sample rate
- Signaling

Add SerDes components

Export to:
- MATLAB
- Simulink
- IBIS-AMI

Component specifications

Plot analysis results

High-speed link
SerDes Top Down Design

- Create a MATLAB script for automation and design space exploration
- Export to Simulink models for time-domain simulation
- Create dual IBIS-AMI models
SerDes Toolbox: Simulink Models

- Develop adaptive equalizers using white-box models such as DFE, CTLE, AGC, and CDR
- Use parametrized blocks and algorithms for single-ended and differential signals
- Generate PRBS and custom stimulus patterns supporting PAM4 and NRZ modulation
SerDes Simulation and Architecture Exploration

Channel modeling

White-box (customizable) models

Simulate and customize adaptive equalizers

Global Parameters
Automatic Generation of Standard Compliant IBIS-AMI Models
Statistical vs. Time Domain

Analog Channel Pulse Response → Transmit Equalization → Receive Equalization → Statistical Analysis → RX AMI File Parameters

Statistical Eye

Clock PDF

Analog Channel Impulse Response → Transmit Equalization → Convolve → Receive Equalization → Accumulate

Persistent Eye

Clock PDF

Stimulus → TX GetWave → RX GetWave

TX Init → RX Init
SerDes Toolbox: IBIS-AMI Dual Model Generation

- Generate standard-compliant Init and GetWave IBIS-AMI models
- Generate associated analog IBIS model
- Customize the model interface by managing the IBIS-AMI-parameters
SerDes Verification Using Channel Simulators
Channel Simulation Using IBIS-AMI Models

- Integrate standard-compliant IBIS-AMI models in 3rd party channel simulators
  - Correlation & regression testing
  - Identification of corner cases over large families of channel models and configurations
Integration with QCD/QSI (SiSoft Link)

- Bidirectional link between SerDes Toolbox and SiSoft QCD/QSI
- Automatically create a QCD/QSI project from SerDes Toolbox
- Back-annotate the channel model, stimuli, and AMI parameter settings into SerDes Toolbox
- Rapidly iterate between system design and channel simulation
Use Simulink and SerDes Toolbox

- Algorithmic design, analysis, and system-level simulation of SerDes systems with many trusted functions

- Integrate with 3rd party channel simulators for SerDes verification
  - Generate standard-compliant IBIS-AMI models

- Link with IC design tools to model implementation impairments and reuse testbenches
  - Co-simulation, HDL/SV code generation, and data post-processing
Thank You!

Q&A