

# MATLAB EXPO 2018

## Developing Battery Management System using Simulink

Chirag Patel  
MathWorks



# Motivation

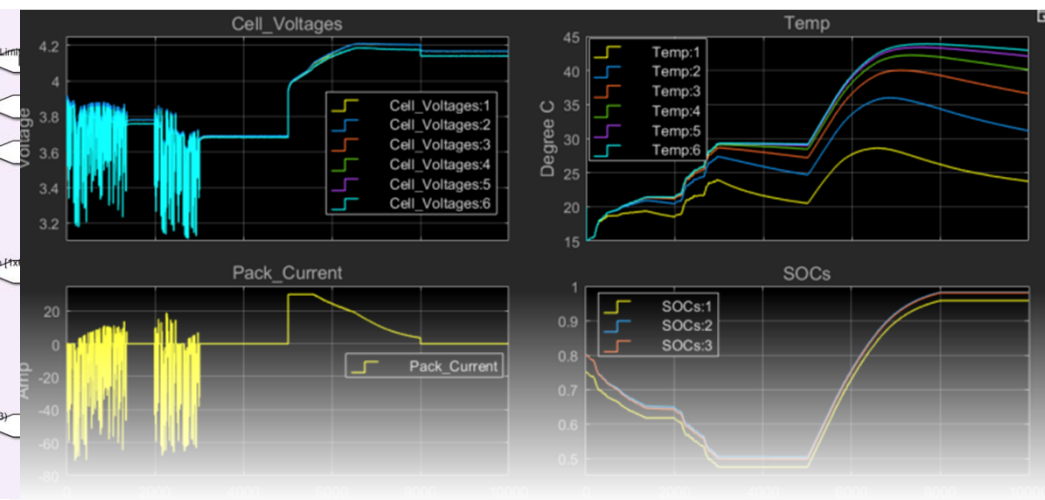
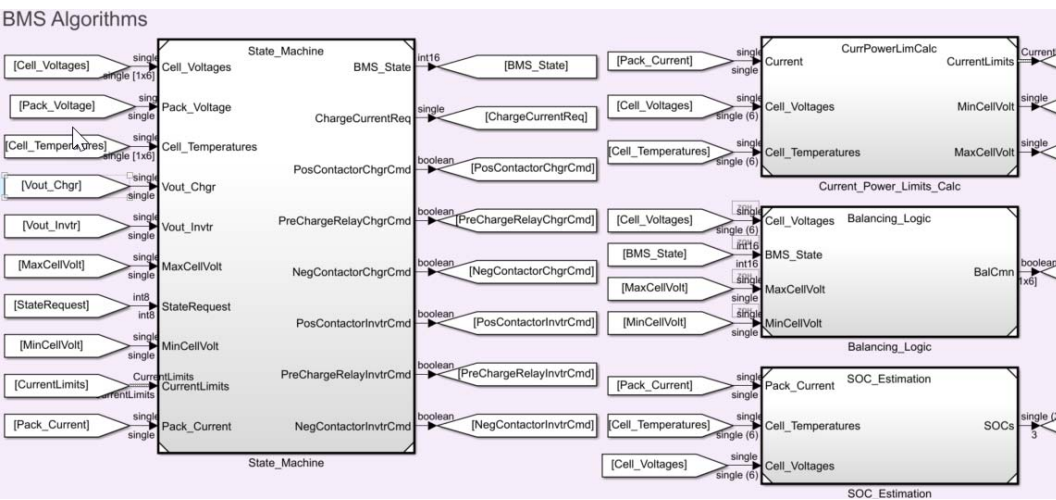
## Collaboration



## Short Iteration Cycles



## Safety Critical System



# What is BMS?



## Battery Pack

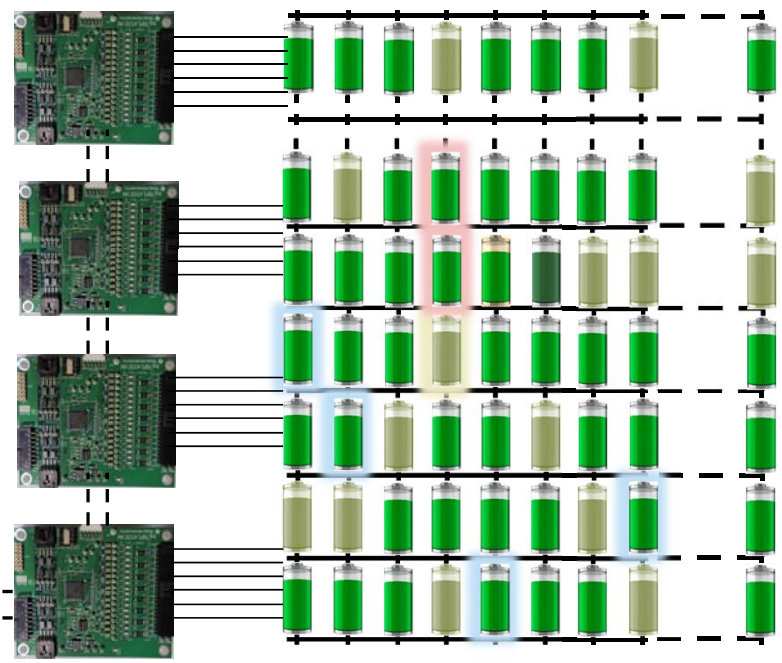


```

if (((uint32_T)State_Machine_DW.temporalCounter_i3) < 15U) {
    State_Machine_DW.temporalCounter_i3 = (uint8_T)((int32_T)((int32_T)
        State_Machine_DW.temporalCounter_i3) + 1));
}

if (((uint32_T)State_Machine_DW.is_active_c2_State_Machine) == 0U) {
    State_Machine_DW.is_active_c2_State_Machine = 1U;
    State_Machine_DW.is_MainStateMachine = State_Machine_IN_Standby;
    *rtu_BMS_State = 0;
    State_Machine_DW.MonitorCurrLimMode = MonitorCurrLimModeType_NoCurrLimFaul
    State_Machine_DW.MonitorCellVoltageMode =
        MonitorCellVoltageModeType_NoCellVoltFault;
    State_Machine_DW.Delta = (real32_T)fabs((real_T)((real32_T)
        ((*rtu_Pack_Voltage) - sum_gyOCKAG3(rtu_Cell_Voltages))));
    State_Machine_DW.FaultPresent = false;
}
    
```

- Supervisory tasks
- SOC estimation
- Contactor management
- Isolation monitoring
- Fault detection and recovery
- Thermal Management
- Current & Power Limits



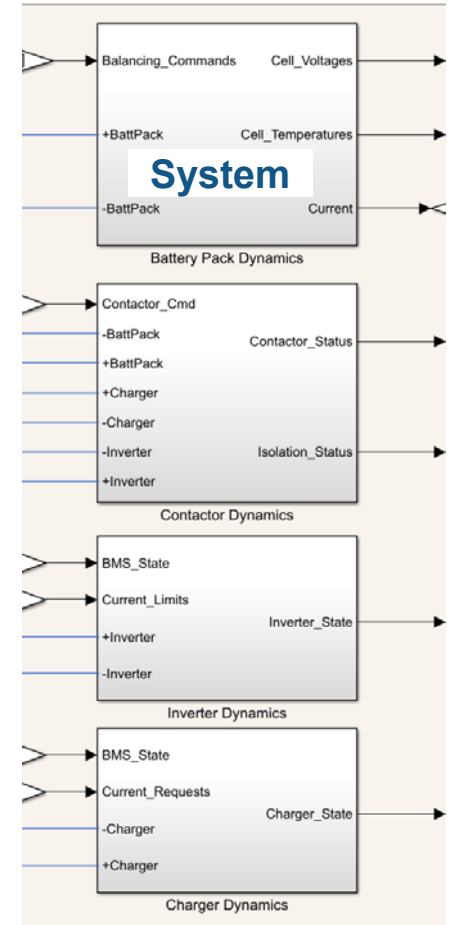
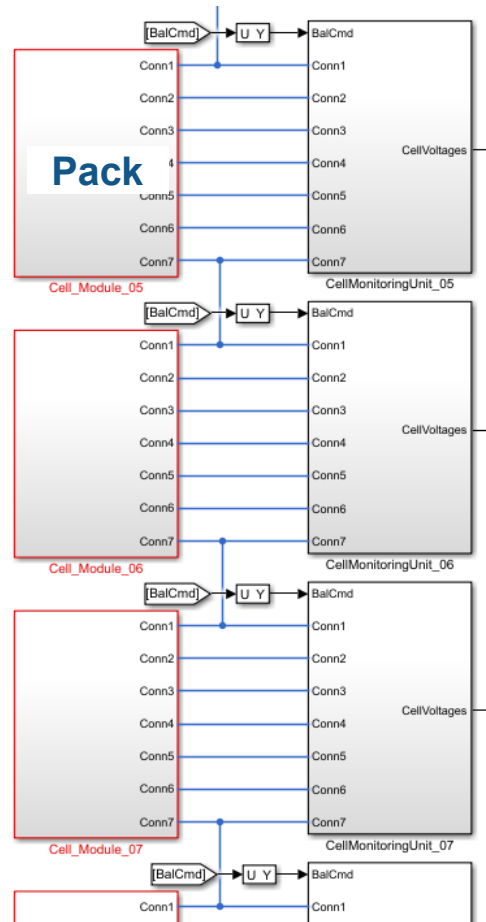
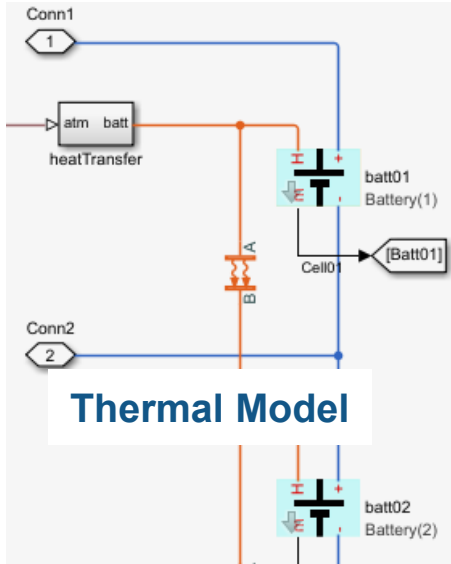
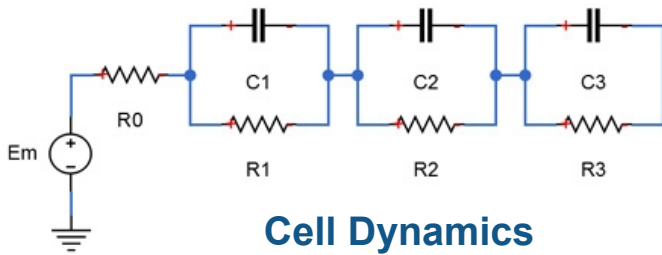
Block Voltage,  
Temperature Measurement  
Cell Diagnostic  
Cell Balancing

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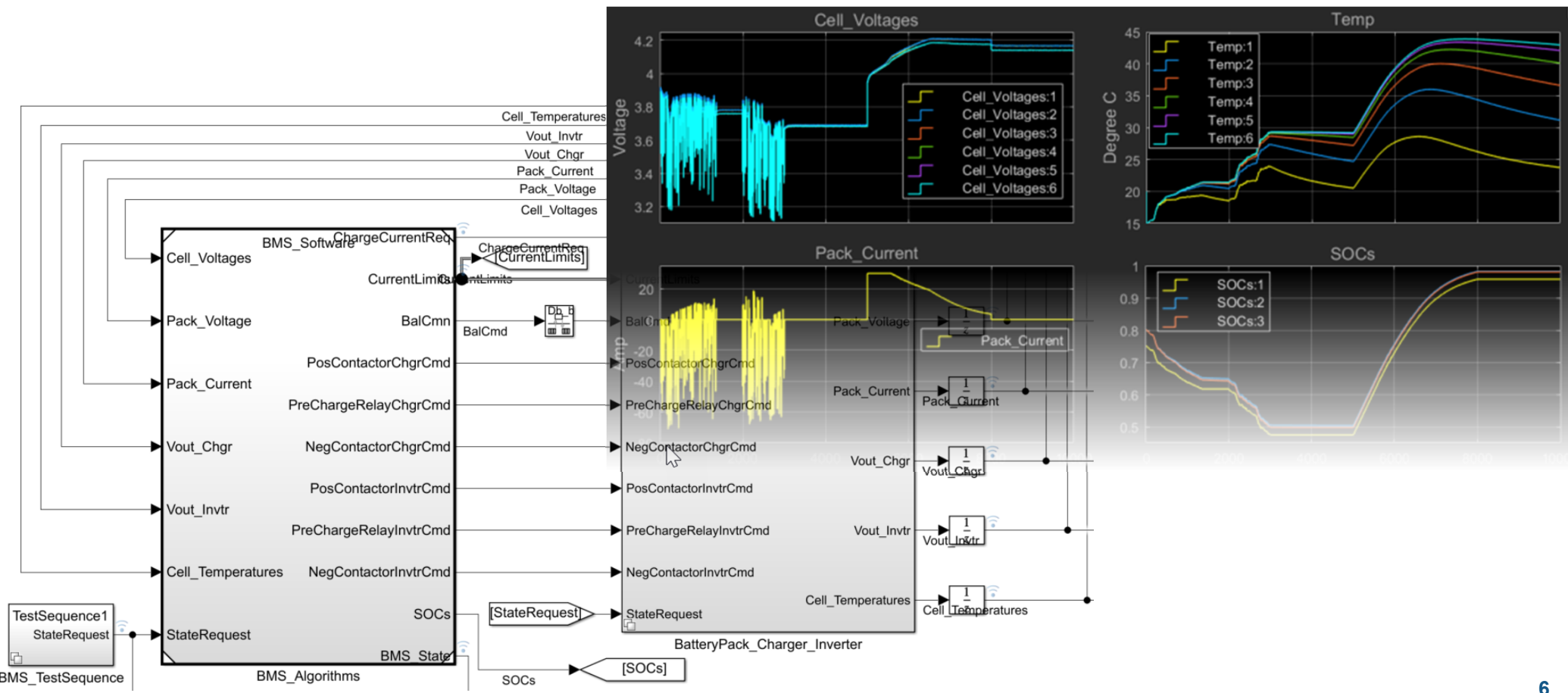


# Start with Simulation

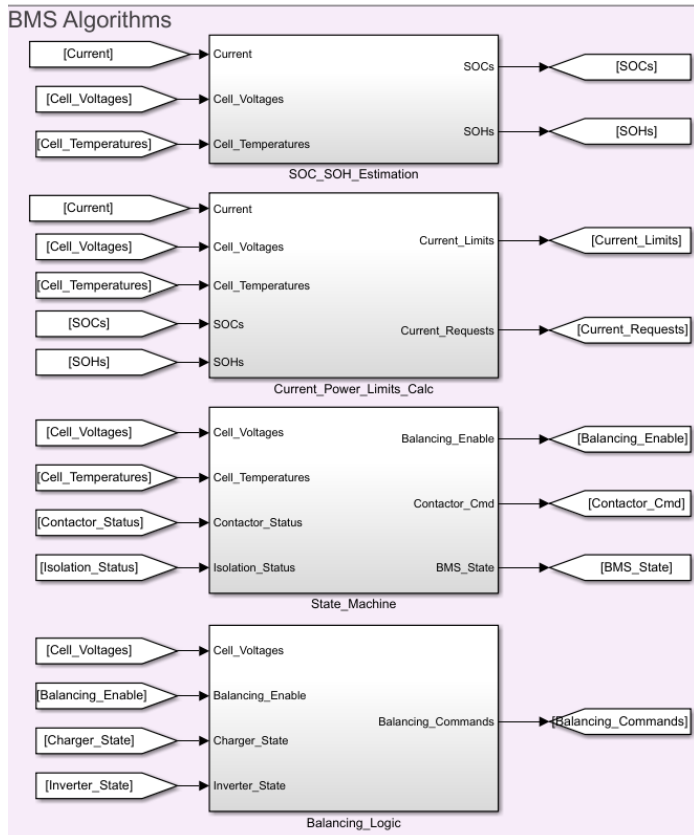
## Capture Dynamics of Battery Cell → Large Battery Pack



# Develop Battery Management Algorithms in Simulink



# Generate C/C++ Code From BMS Algorithm Models



Find:
Match Case

**Contents**

Summary

[Subsystem Report](#)

[Traceability Report](#)

[Static Code Metrics Report](#)

[Code Replacements Report](#)

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**Generated Code**

[ - ] **Model files**

- State\_Machine.c (16)
- [State\\_Machine.h](#)
- [State\\_Machine\\_private.h](#)
- [State\\_Machine\\_types.h](#)

[ + ] **Shared files (3)**

387

388 `if (((uint32_T)State_Machine_DW.temporalCounter_i3) < 15U) {`

389 `State_Machine_DW.temporalCounter_i3 = (uint8_T)((int32_T)((int32_T)`

390 `State_Machine_DW.temporalCounter_i3) + 1));`

391 `}`

392

393 `if (((uint32_T)State_Machine_DW.is_active_c2_State_Machine) == 0U) {`

394 `State_Machine_DW.is_active_c2_State_Machine = 1U;`

395 `State_Machine_DW.is_MainStateMachine = State_Machine_IN_Standby;`

396 `*rtx_BMS_State = 0;`

397 `State_Machine_DW.MonitorCurrLimMode = MonitorCurrLimModeType_NoCurrLimFault;`

398 `State_Machine_DW.MonitorCellVoltageMode =`

399 `MonitorCellVoltageModeType_NoCellVoltFault;`

400 `State_Machine_DW.Delta = (real32_T)fabs((real_T)((real32_T)`

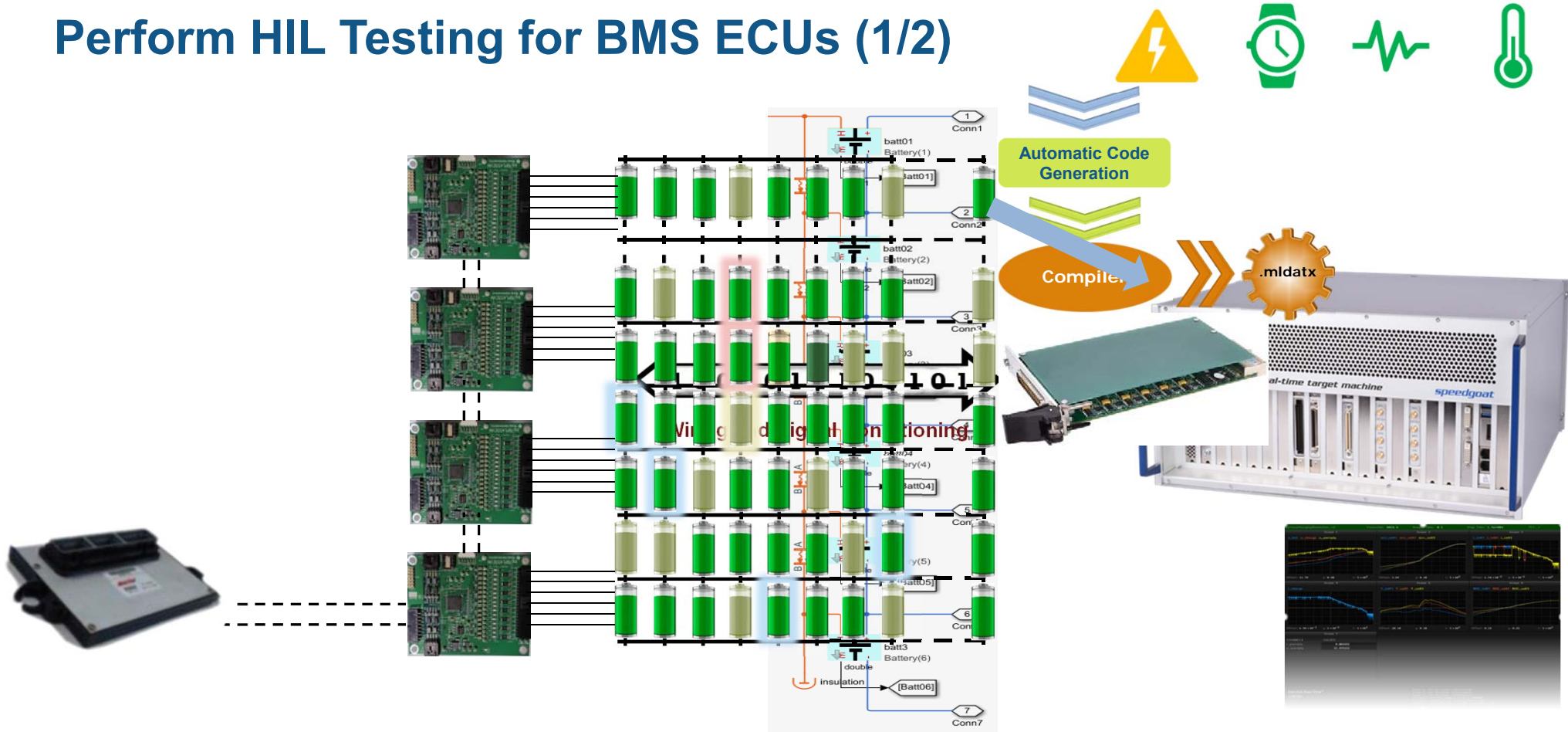
401 `(((*rtu_Pack_Voltage) - sum_gyOCKAG3(rtu_Cell_Voltages))));`

402 `State_Machine_DW.FaultPresent = false;`

**State\_Machine** View All

State\_Machine State\_Machine

# Perform HIL Testing for BMS ECUs (1/2)



## Perform HIL Testing for BMS ECUs (2/2)

### IO991: Battery Emulation I/O Module

#### Key Features

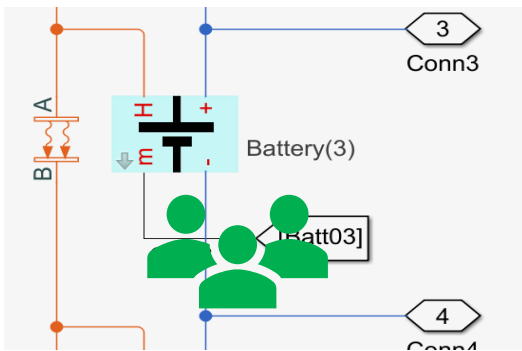
- 6 independent isolated channels
- Architecture allows series and parallel battery stack combinations
- Independent power and sense lines
- Voltage range of 0-7 V with 14-bit resolution
- 300 mA source to load
- 100 mA sink adjustable in 16 steps





# Summary

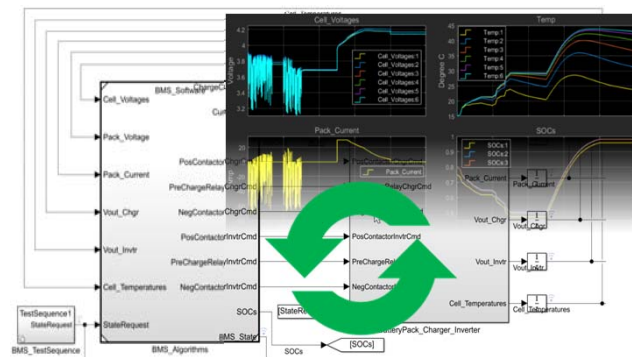
## Multi-Domain



## Collaborate Across Domains

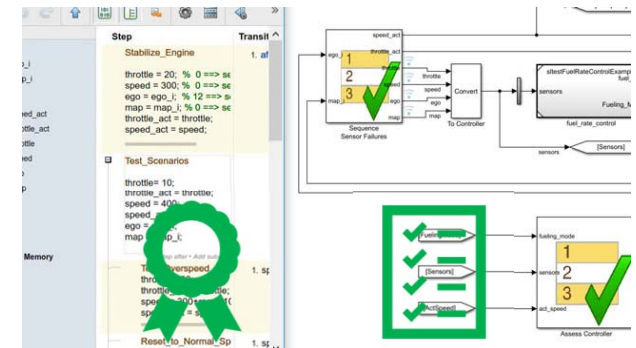
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## Long Iteration Cycles



## Reduce Iteration Time

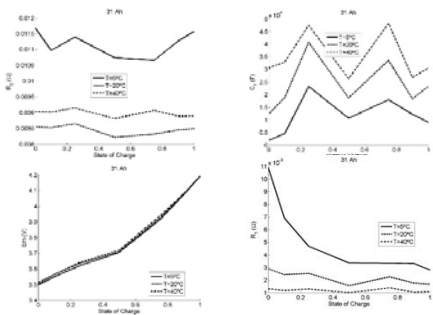
## Safety Critical System



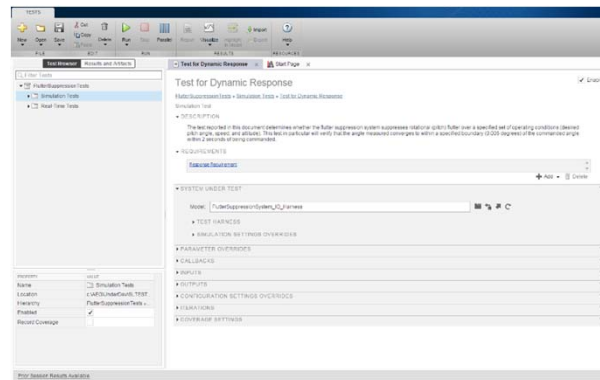
## Functional Safety Certification

# Taking It Further

## Parameter Estimation



## Test Automation



## HDL Code Generation

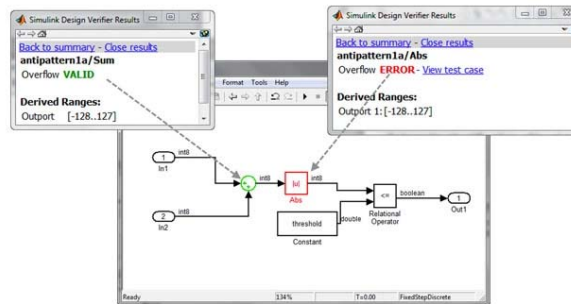


## Model Checks

- Modeling Standards for Secure Coding (CERT C, CWE, ISO/IEC TS 17961)
- Check configuration parameters for secure coding standards
- Check for blocks not recommended for C/C++ production code deployment
- Check for blocks not recommended for secure coding standards
- Check usage of Assignment blocks
- Check for switch case expressions without a default case
- Check for bitwise operations on signed integers
- Check for equality and inequality operations on floating-point values
- Check integer word lengths
- Detect Dead Logic
- Detect Integer Overflow
- Detect Division By Zero
- Detect Out Of Bound Array Access
- Detect Violation of Specified Intermediate Minimum and Maximum Values

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## Design Error Detection

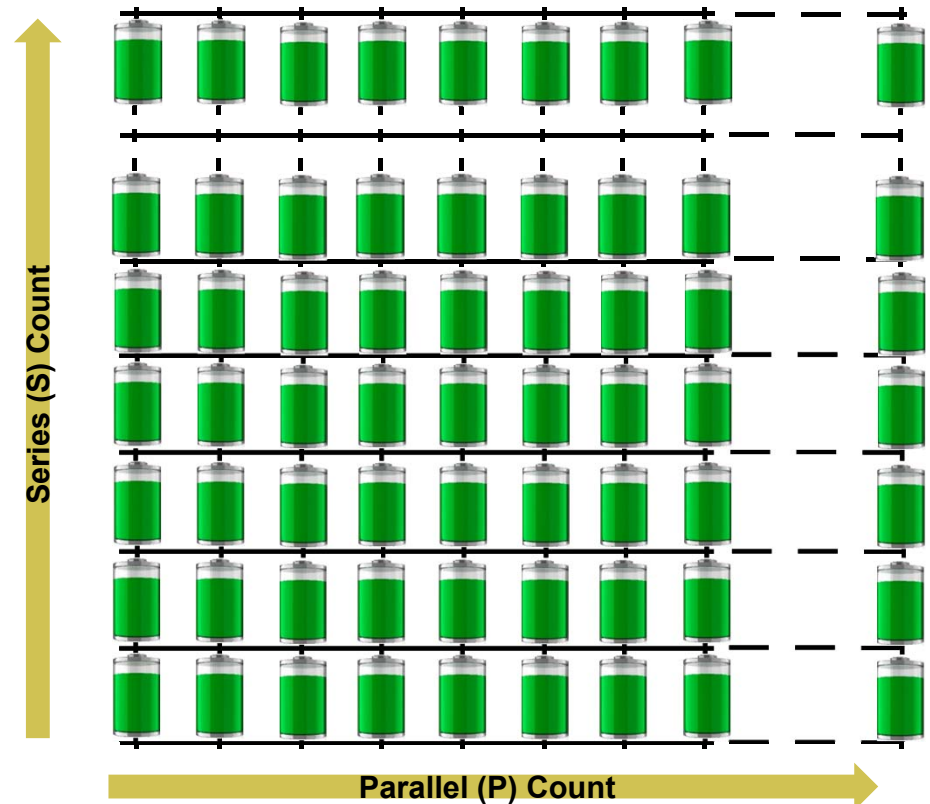


## Model Coverage

Model Hierarchy/Complexity	Current Run			Delta			Cumulative		
	D1	C1	MCDC	D1	C1	MCDC	D1	C1	MCDC
1. <a href="#">Blockset_AutoGen_Test_Trace</a>	31 39%	41%	17%	0%	0%	0%	21%	41%	17%
2. <a href="#">Logic</a>	25 34%	38%	17%	0%	0%	0%	47%	38%	17%
3. <a href="#">SP_Active</a>	24 34%	38%	17%	0%	0%	0%	47%	38%	17%
4. <a href="#">antipattern1a/Abs</a>	11 84%	67%	33%	21%	17%	0%	83%	67%	33%
5. <a href="#">antipattern1a/Sum</a>	4 38%	NA	NA	12%	NA	NA	88%	NA	NA
6. <a href="#">antipattern1a/Sum</a>	13 11%	0%	0%	0%	0%	0%	11%	0%	0%
7. <a href="#">antipattern1a/Sum</a>	8 0%	NA	NA	0%	NA	NA	0%	NA	NA
8. <a href="#">antipattern1a/Sum</a>	3 0%	NA	NA	0%	NA	NA	0%	NA	NA
9. <a href="#">antipattern1a/Sum</a>	8 65%	50%	NA	0%	0%	NA	85%	50%	NA
10. <a href="#">Subsystem1</a>	1 0%	NA	NA	0%	NA	NA	100%	NA	NA
11. <a href="#">Subsystem2</a>	1 0%	NA	NA	0%	NA	NA	100%	NA	NA
12. <a href="#">Subsystem3</a>	1 100%	NA	NA	0%	NA	NA	100%	NA	NA
13. <a href="#">Subsystem4</a>	1 100%	NA	NA	0%	NA	NA	100%	NA	NA
14. <a href="#">Subsystem5</a>	1 0%	NA	NA	0%	NA	NA	0%	NA	NA
15. <a href="#">Subsystem6</a>	1 0%	NA	NA	0%	NA	NA	0%	NA	NA
16. <a href="#">Validation</a>	2 100%	50%	NA	0%	0%	NA	100%	50%	NA

## An Example BMS Architecture (1/2)

- Cells connected in parallel to match Ah capacity requirement
  - a **Block** is one row of P number of cells in parallel
- Blocks are connected in series to match DC Bus voltage
- Cells are assembled, soldered and packaged in smaller Modules
  - A **Module** is typically 6 to 16 **Blocks** in series
- An Example 54kWh Pack Configuration
  - Cell: Nominal 3.6v with Capacity 3.4Ah
  - 46Cells in Parallel; Block of 156.4Ah Capacity
  - 98Cells in Series; 6-S Module; Total 16 Modules
  - Pack of 4416 cells with ~54kWh Capacity



# An Example BMS Architecture (2/2)

