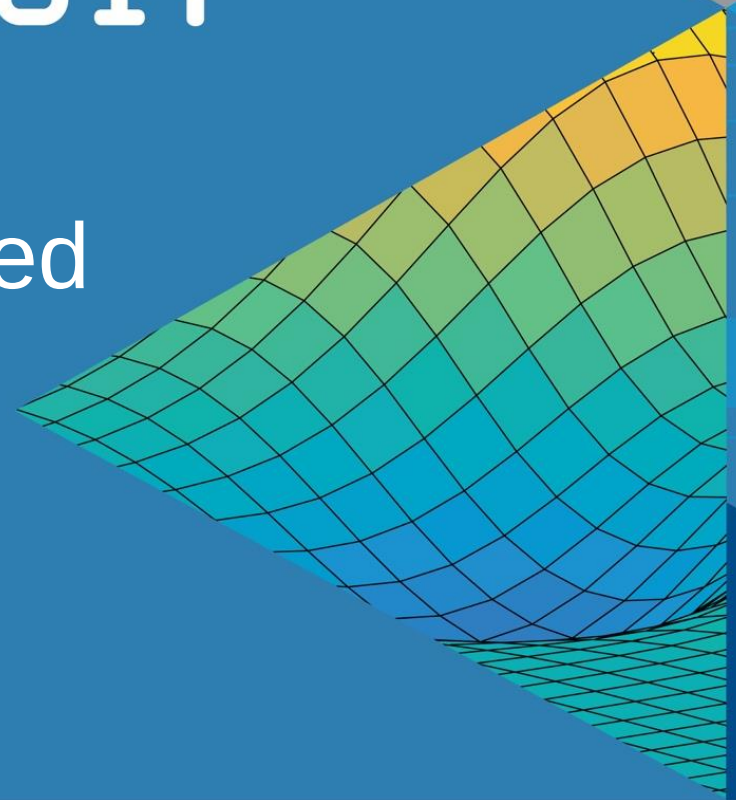
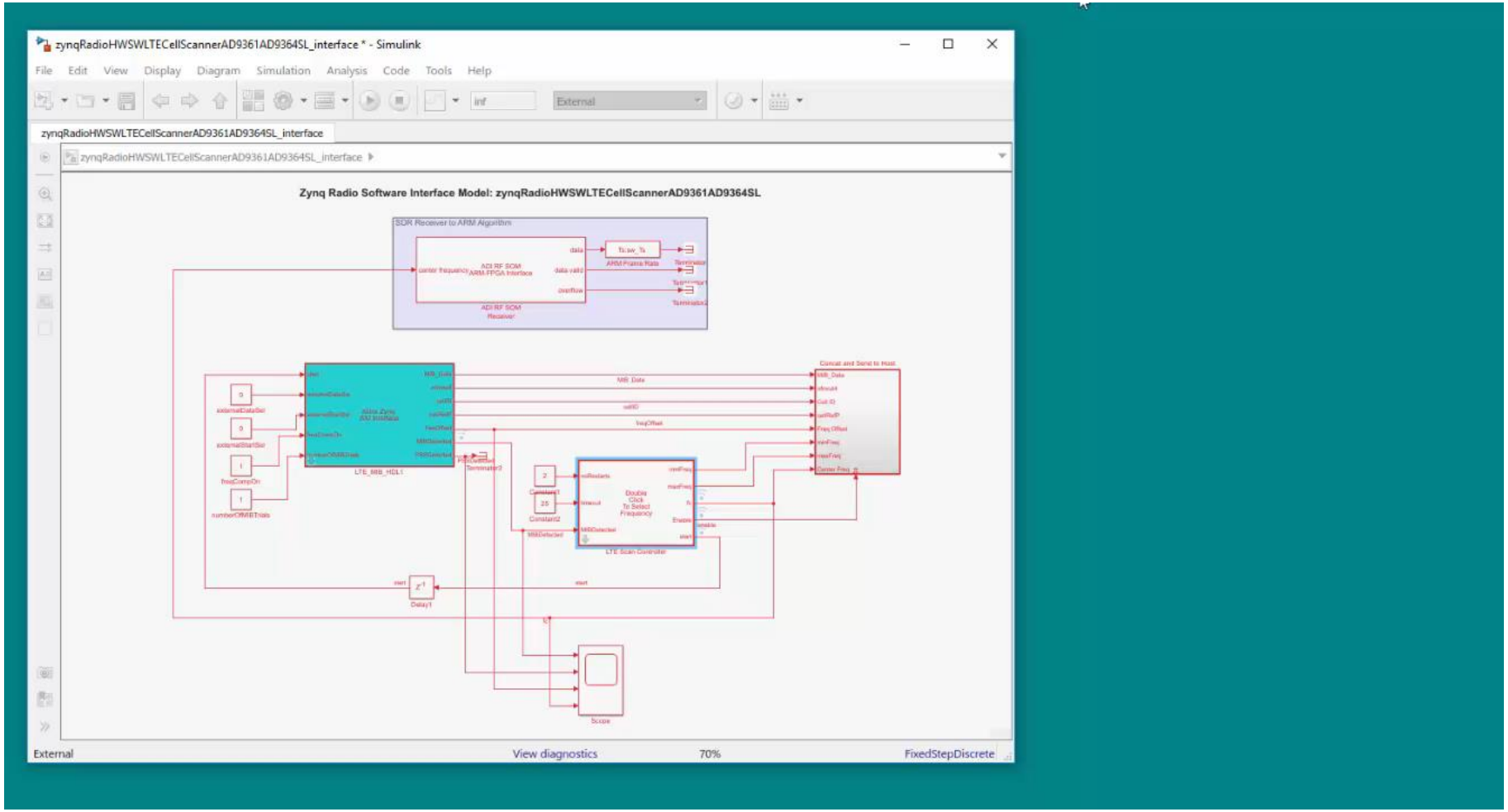
MATLAB EXPO 2017

Simulation, prototyping and verification of standards-based wireless communications

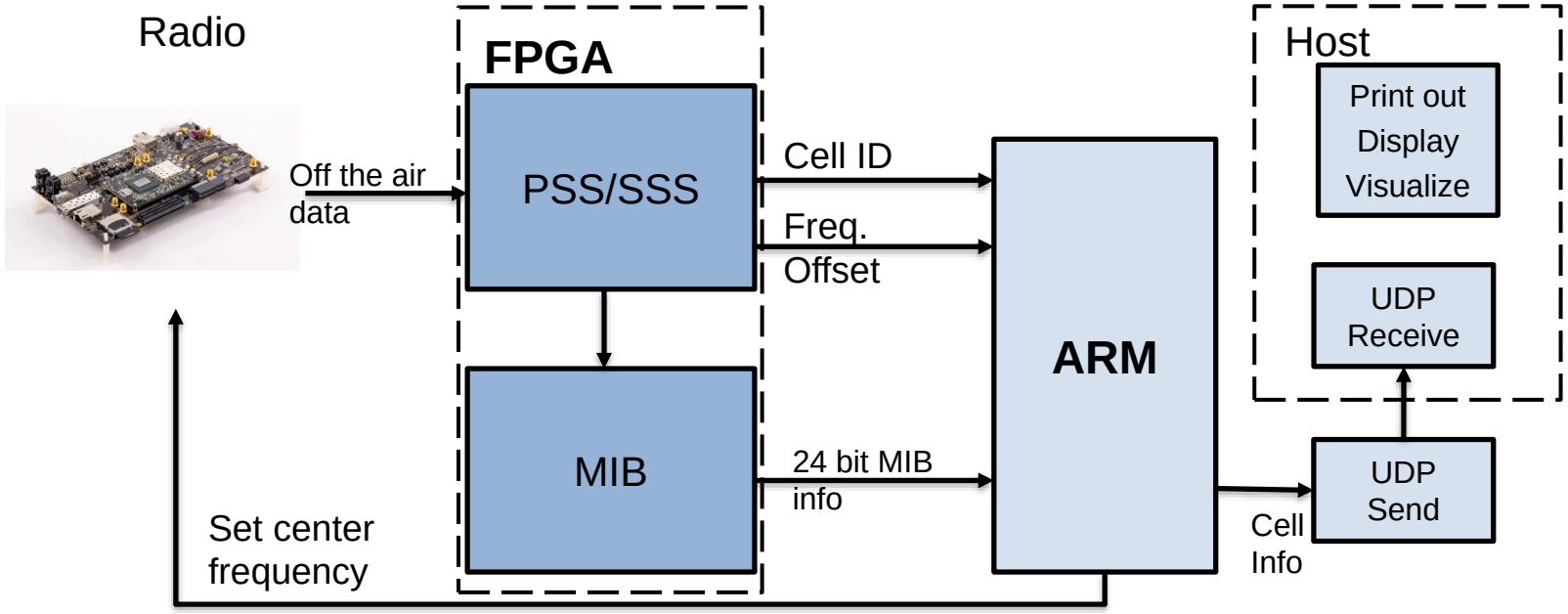
Colin McGuire, Neil MacEwen



Real Time LTE Cell Scanner with MATLAB and Simulink



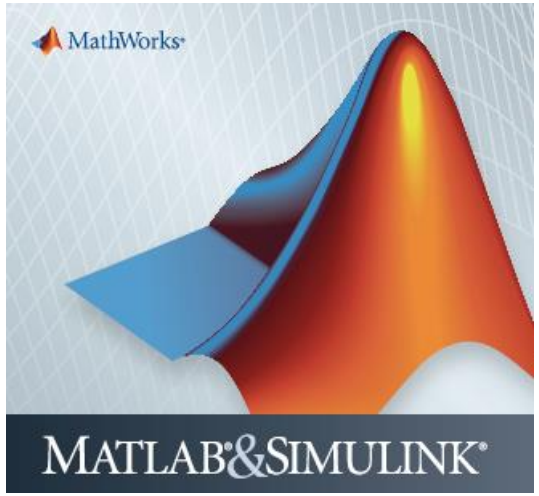
Real time LTE Frequency Scanner

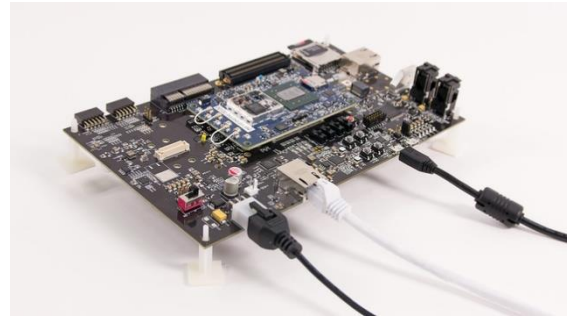


From Design to Prototype

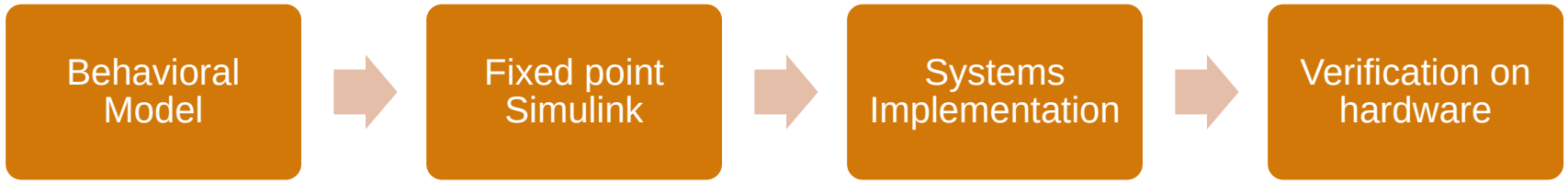
- A common design environment across multiple teams
  - Systems Engineers, RF Engineers, Algorithm Developers, HDL Engineers

- Target off-the-shelf hardware for prototype development





From Design to Prototype

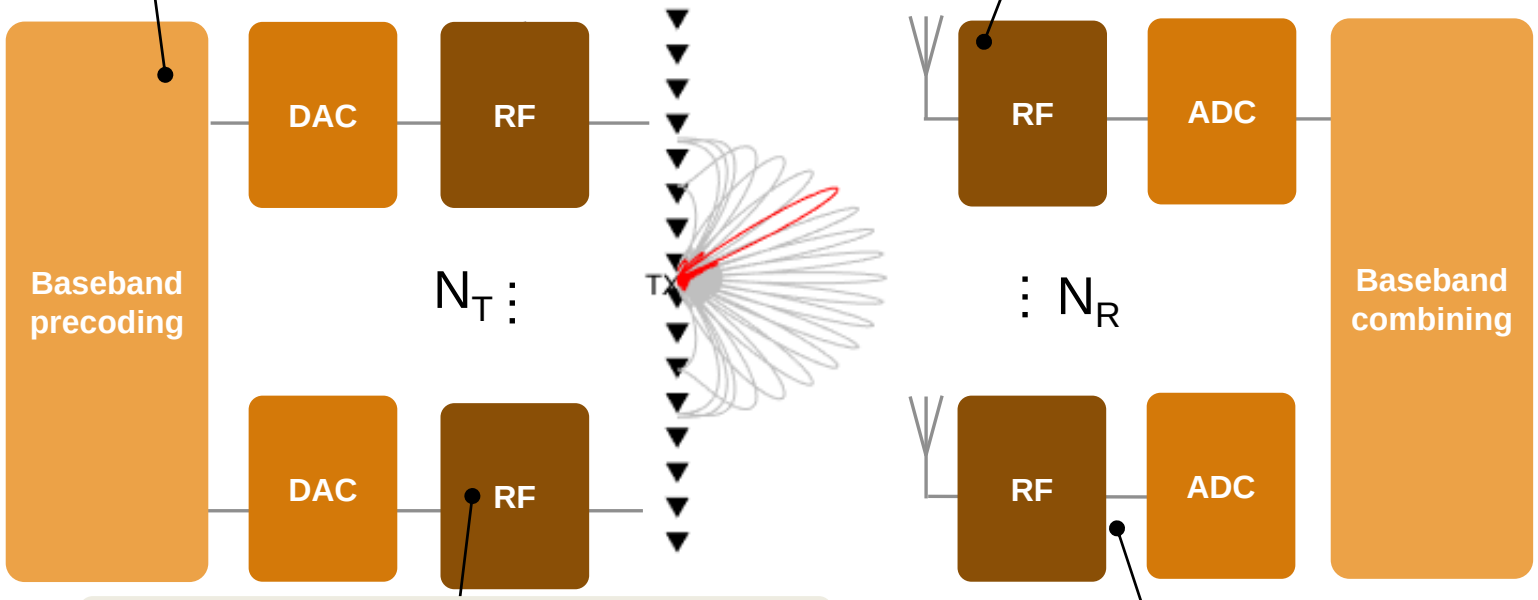


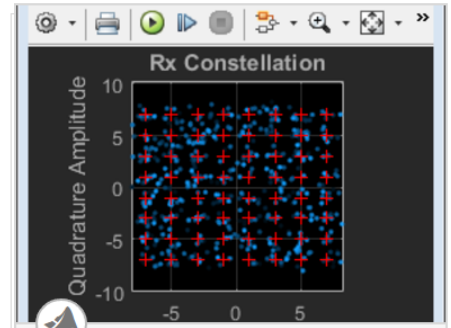
Modeling Wireless Standards with MATLAB & SIMULINK

Wireless Modeling Challenges

Baseband DSP development
- Is my implementation correct?
- How can I evaluate link performance with my algorithm?
- 5G challenges, e.g. out of band emission..

Antenna array design and evaluation
- Element coupling
- Edge effects
- Imperfections





Wireless Digital Video Broadcasting with RF Beamforming

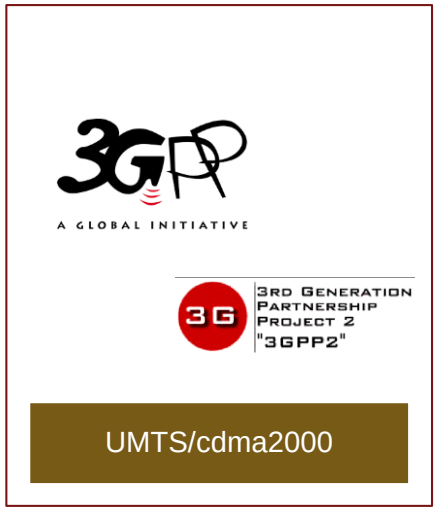
Model a digital video broadcasting system which includes phased array antennas. The baseband transmitter, receiver and channel are realized

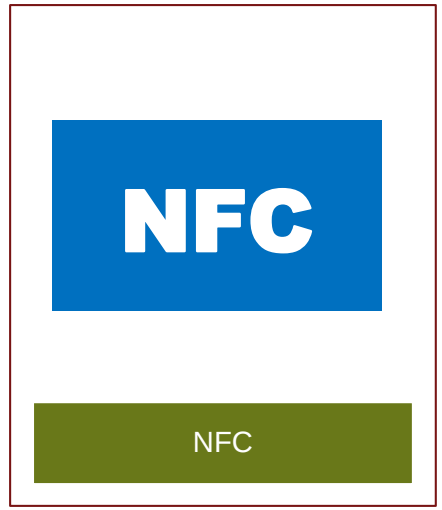
Open Script

Explore beamforming trade-offs
- Baseband, analogue or hybrid beamforming?
- Simulate capabilities and limitations
- Trade-off ADCs vs RF components

Investigate the impact of RF impairments
- Frequency dependency
- Non-linearities
- Mismatches and coupling

Modeling Wireless Standards with MATLAB & SIMULINK





From Design to Prototype

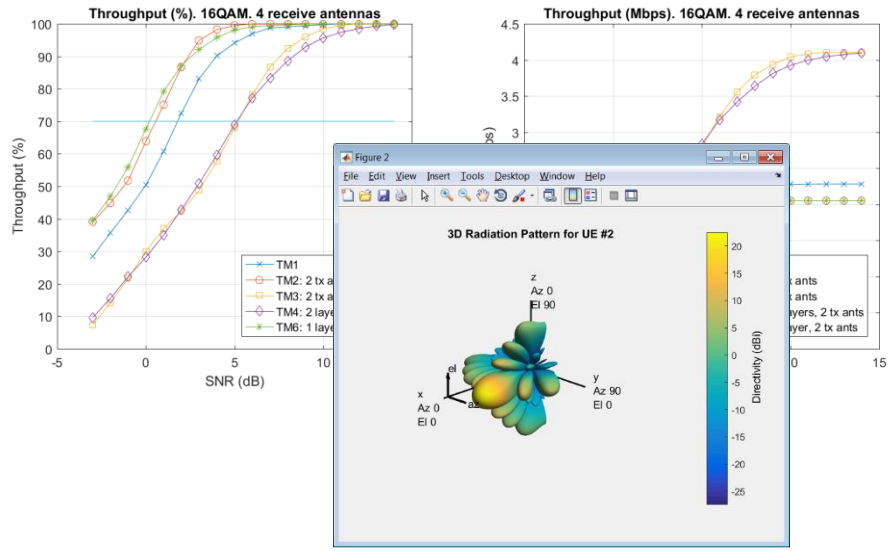
How can I evaluate the performance of my algorithm?

Behavioral Model

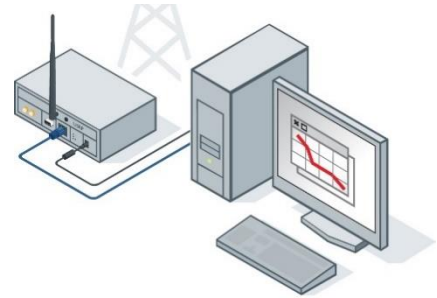
Fixed point Simulink

Is my implementation correct?

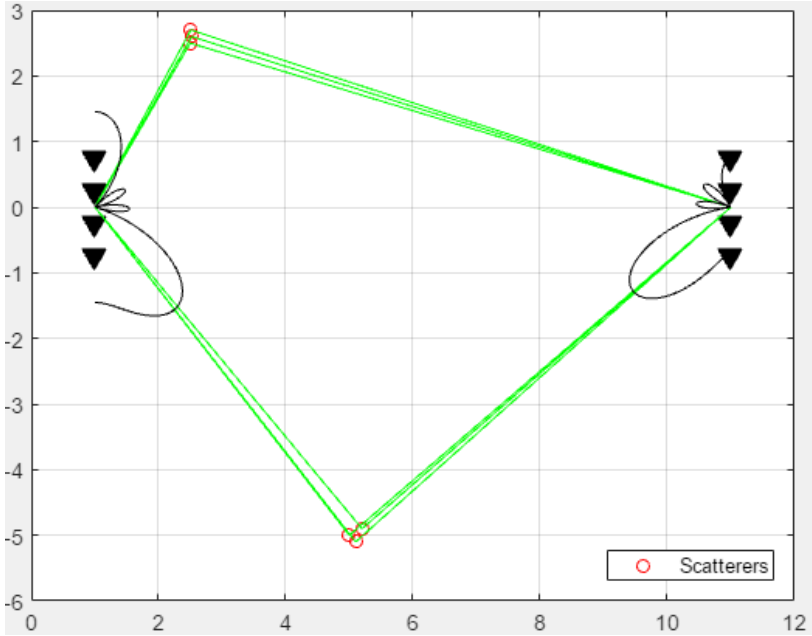
System simulation



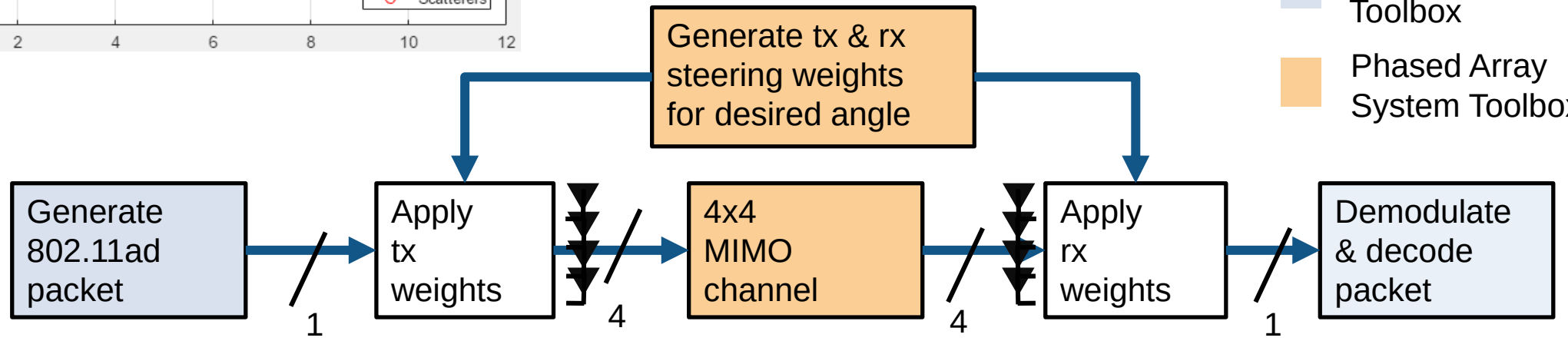
Working with real signals



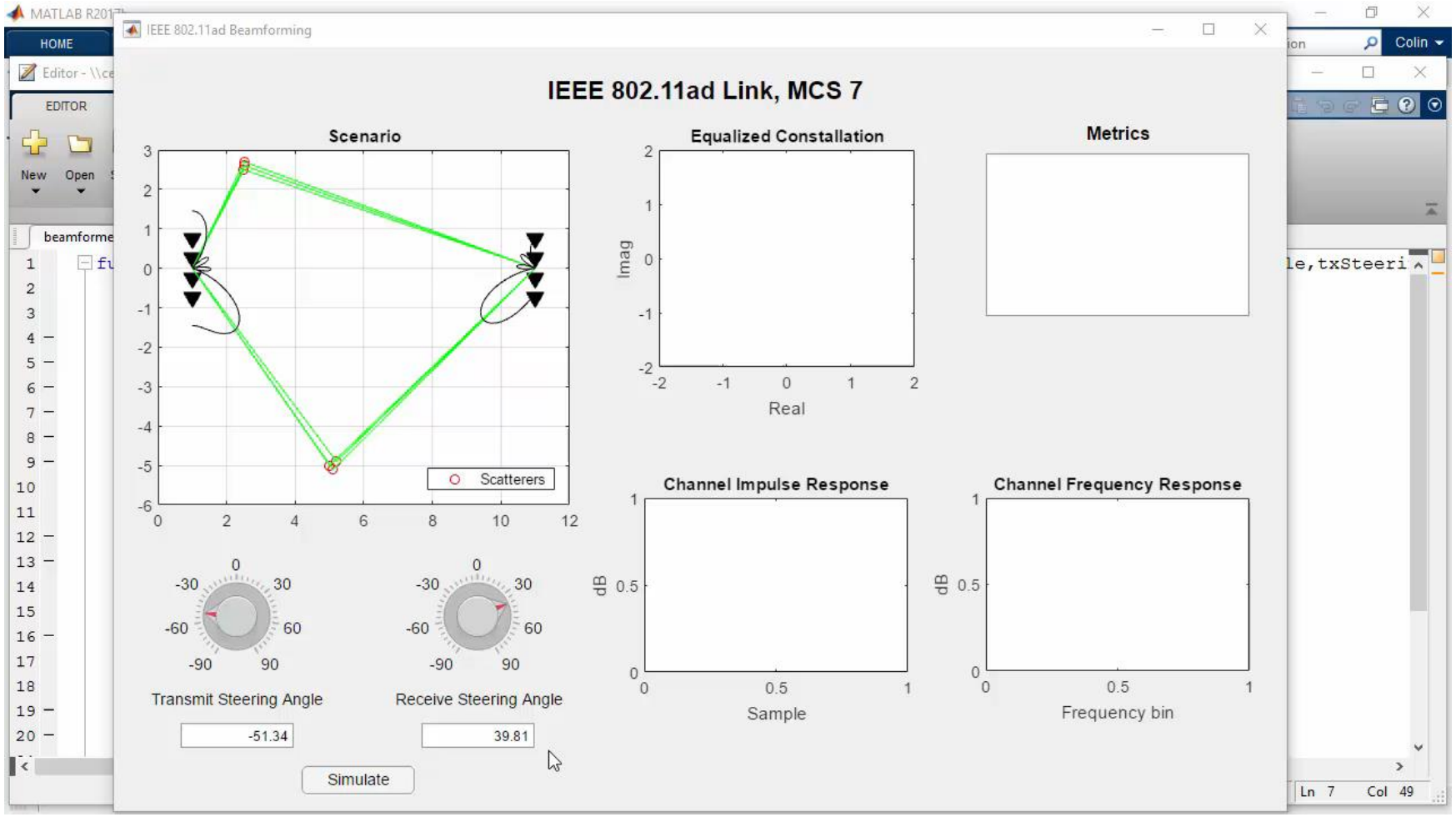
Demo: Modeling 802.11ad Beamforming



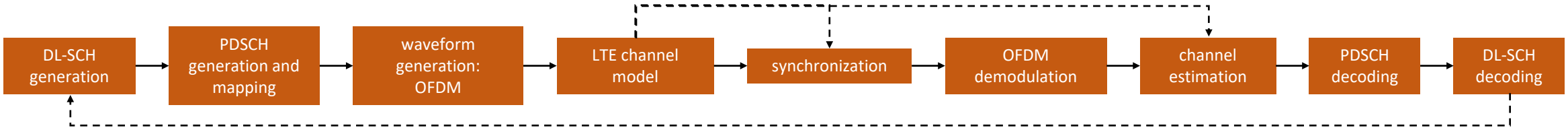
- Uniform linear array of 4 elements at transmitter and receiver
- MIMO channel with 6 scatterers
- PER and EVM for 802.11ad link

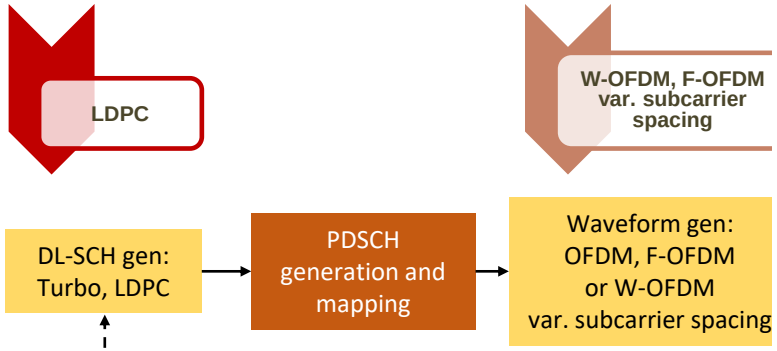


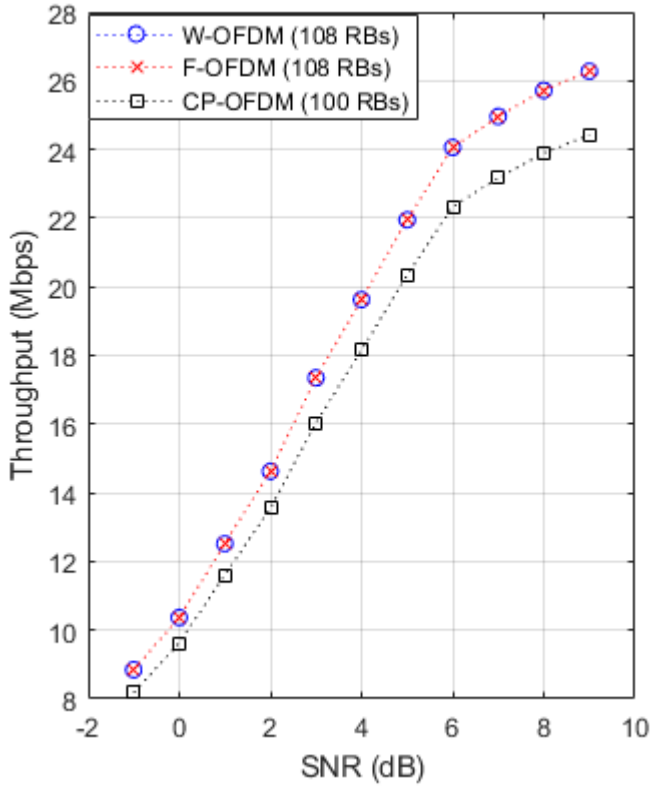
Demo: Modeling 802.11ad Beamforming

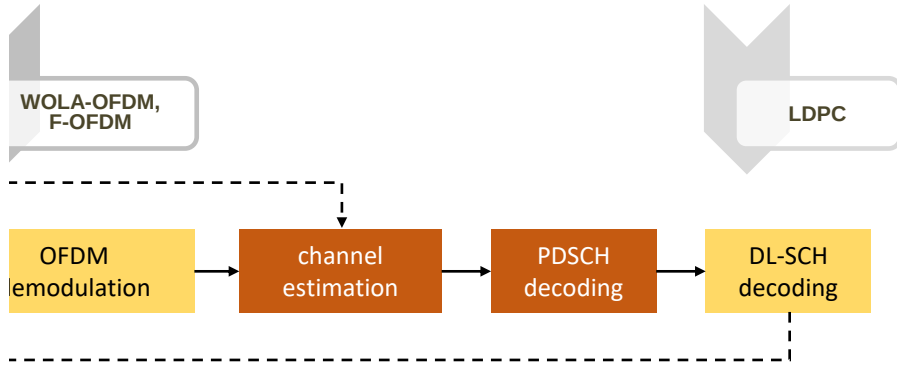


Extending standards… LTE to 5G

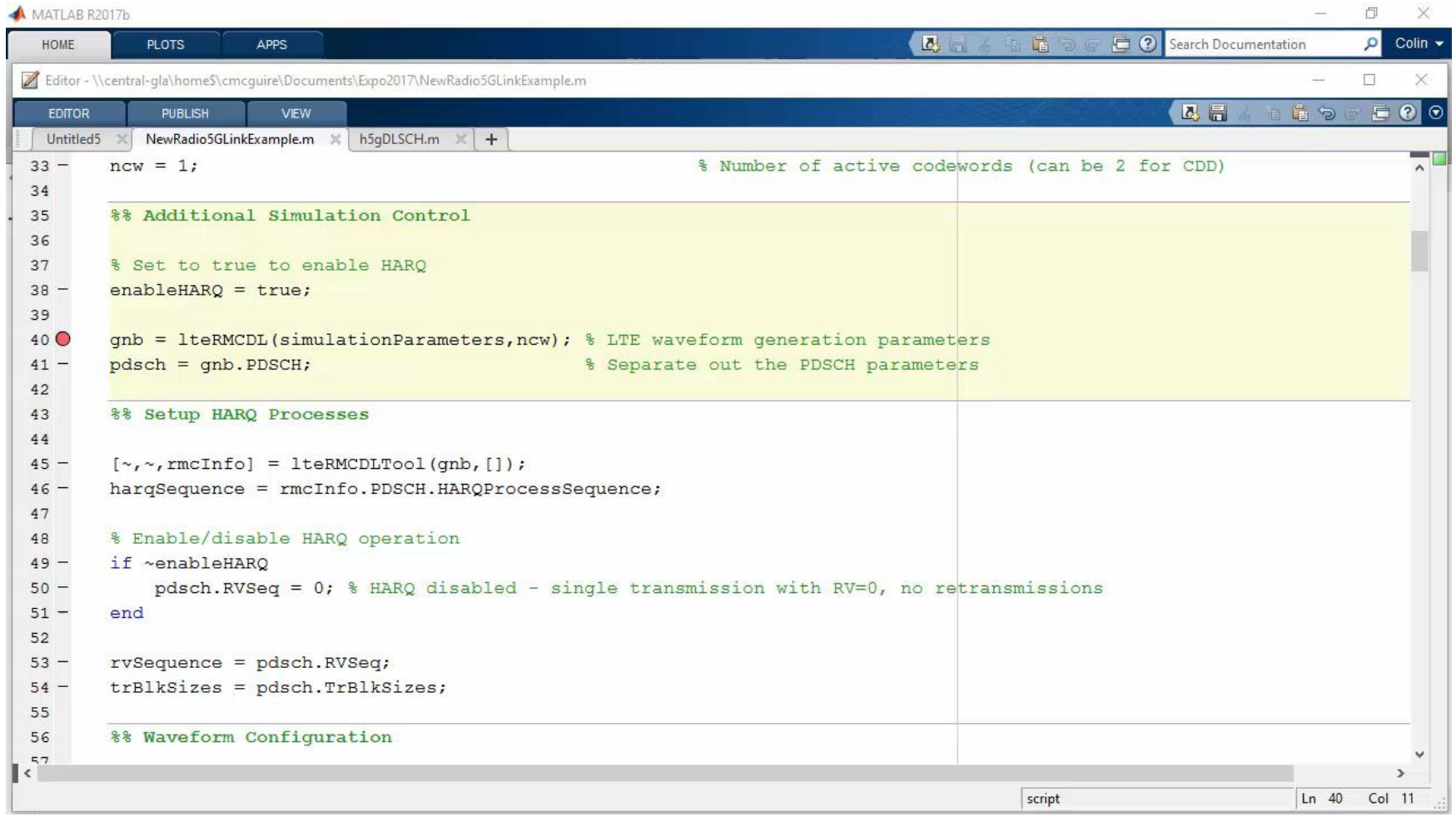








Demo – Extending LTE for 5G link level simulation



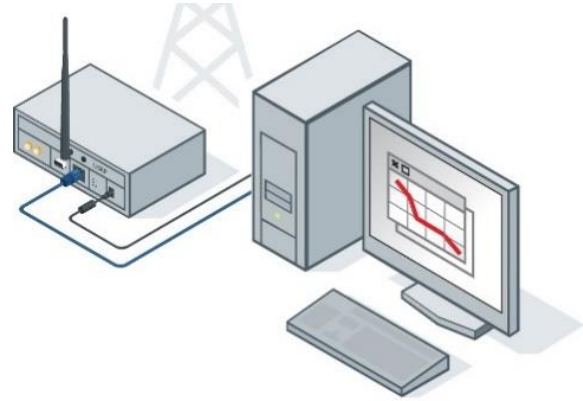
From Design to Prototype

How can I evaluate the performance of my algorithm?

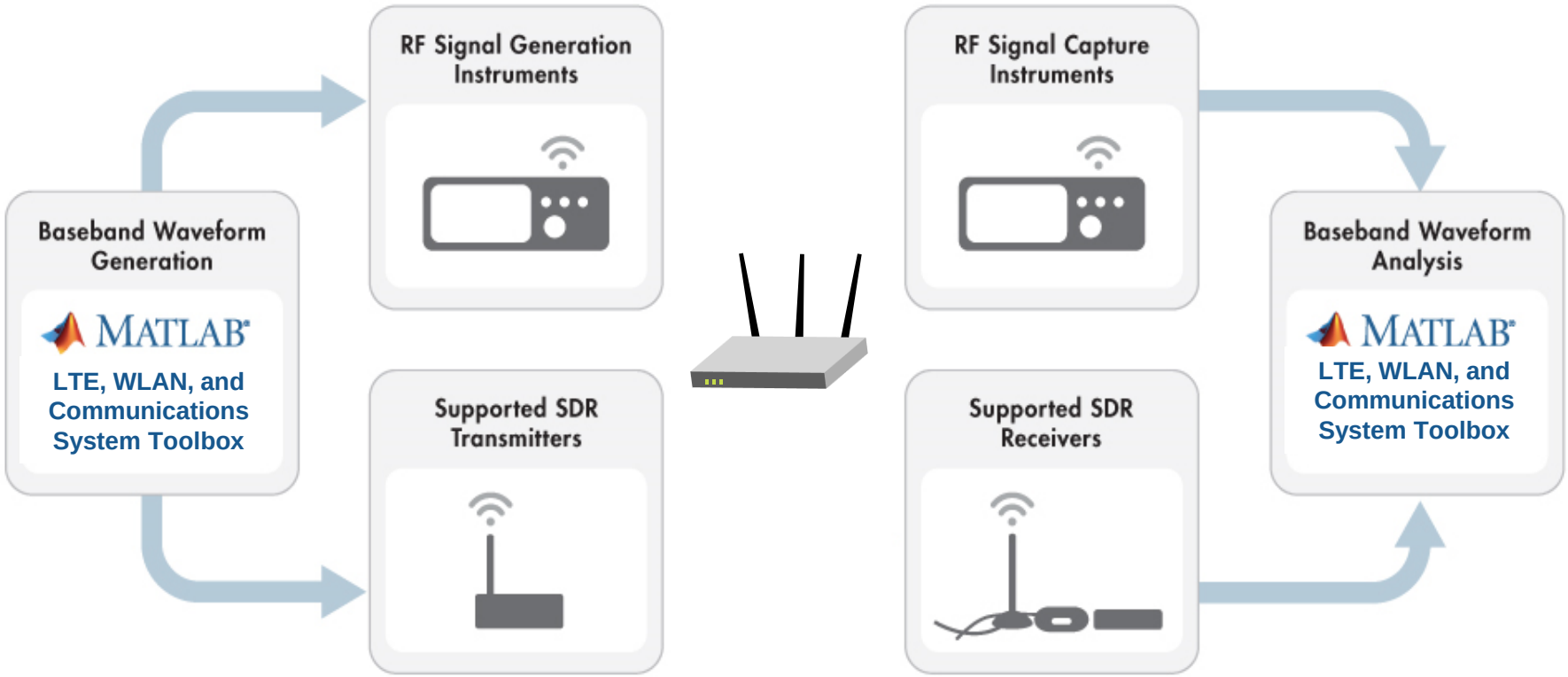
Behavioral Model → Fixed point Simulink

Is my implementation correct?

Working with real signals



Working with Real Signals… Beyond Simulation



Supported Hardware for Radio Connectivity

Decreasing Cost

Signal Generator and Analyser

Keysight, R&S, NI, Tektronix, …
High quality RF front end
Wide frequency range, high bandwidth

SDR

USRP, PLUTO, Zynq, …
Customizable RF front end
Sizable FPGA for targeting designs

Ultra low-cost SDR

RTL-SDR, …
Low bandwidth
Receive only

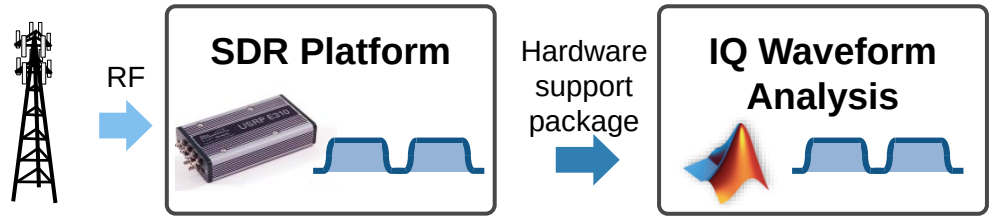
Instrument Control Toolbox

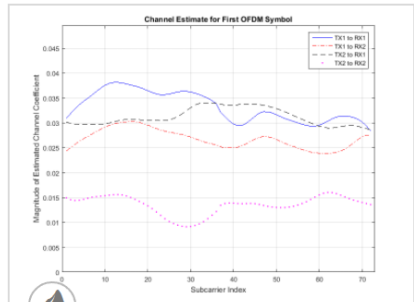
SDR Hardware Support Package

Prototype with Real Signals

- SDR platforms can be used as low-cost RF interface
- Transmit repeat capability allows USRP E310 or Zynq to be used as an RF signal generator

- Capture a burst of IQ and process in MATLAB





LTE Cell Search, MIB and SIB1 Recovery with Two Antennas

Uses both channels of USRP® B210, X300 or X310 to receive an LTE downlink signal. The LTE System Toolbox™ is used to

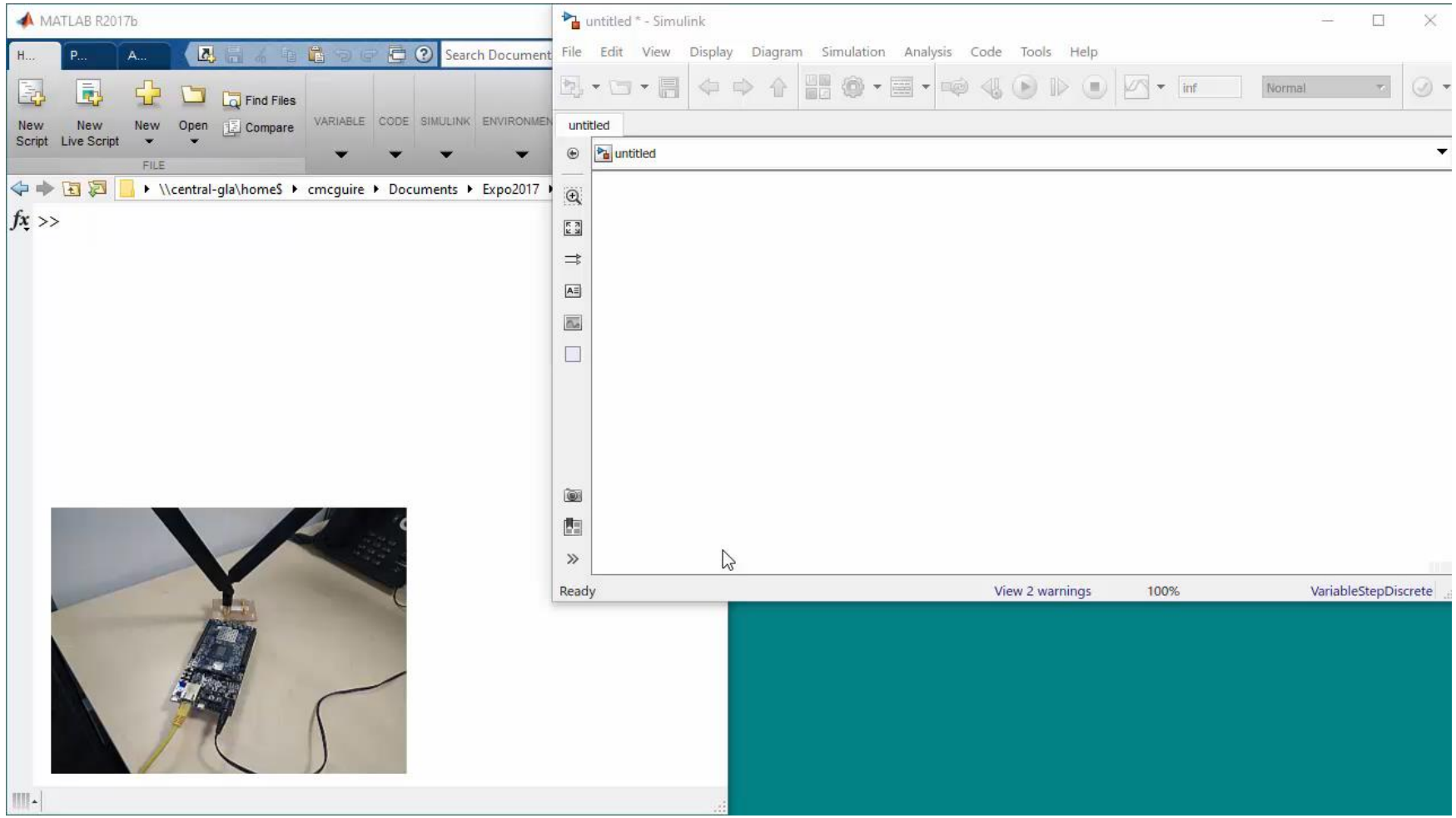
Open Script

802.11a Transmission and Reception Using Analog Devices AD9361/AD9364

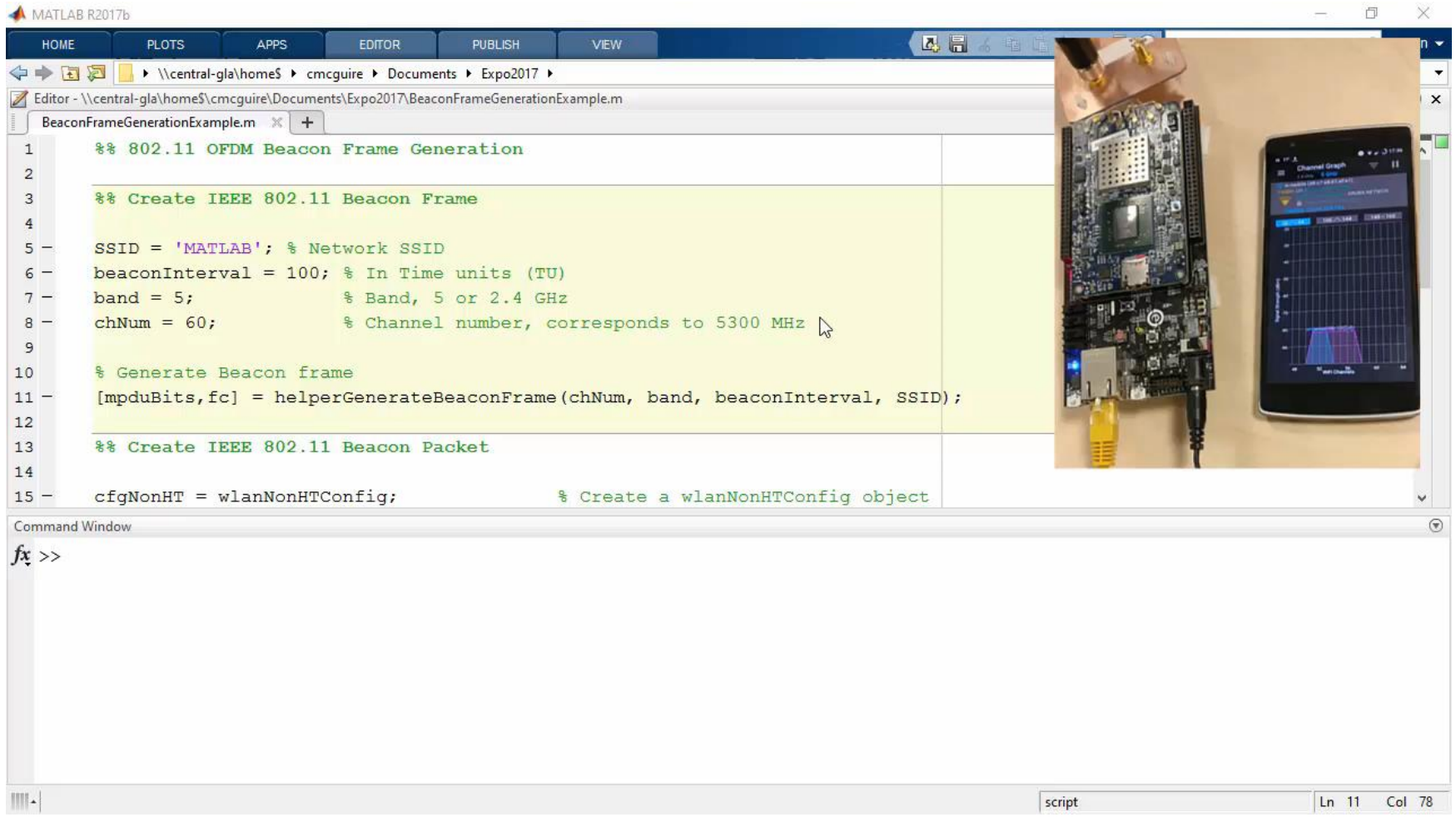
Transmit and receive WLAN packets on a single SDR platform, using Xilinx® Zynq-Based Radio Support Package with MATLAB® and WLAN

Open Script

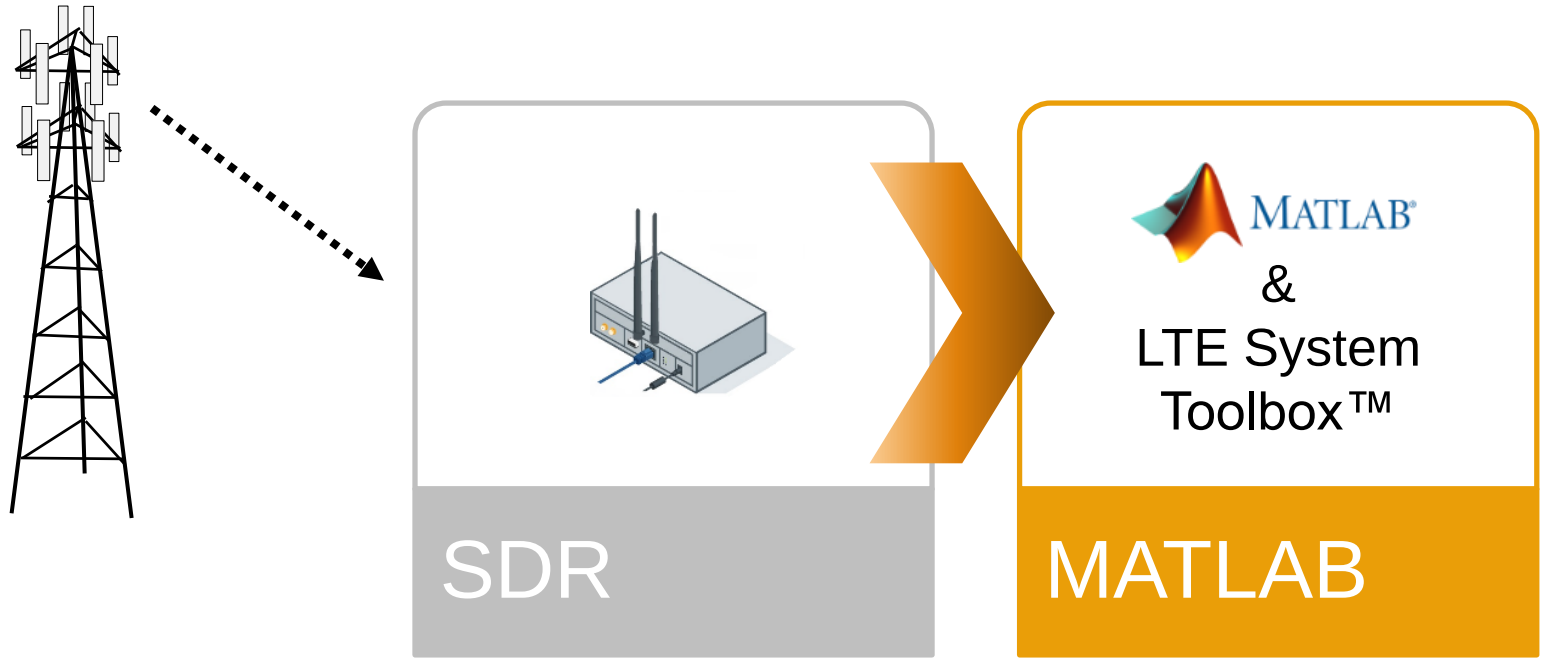
Demo: SDR as a low-cost RF interface



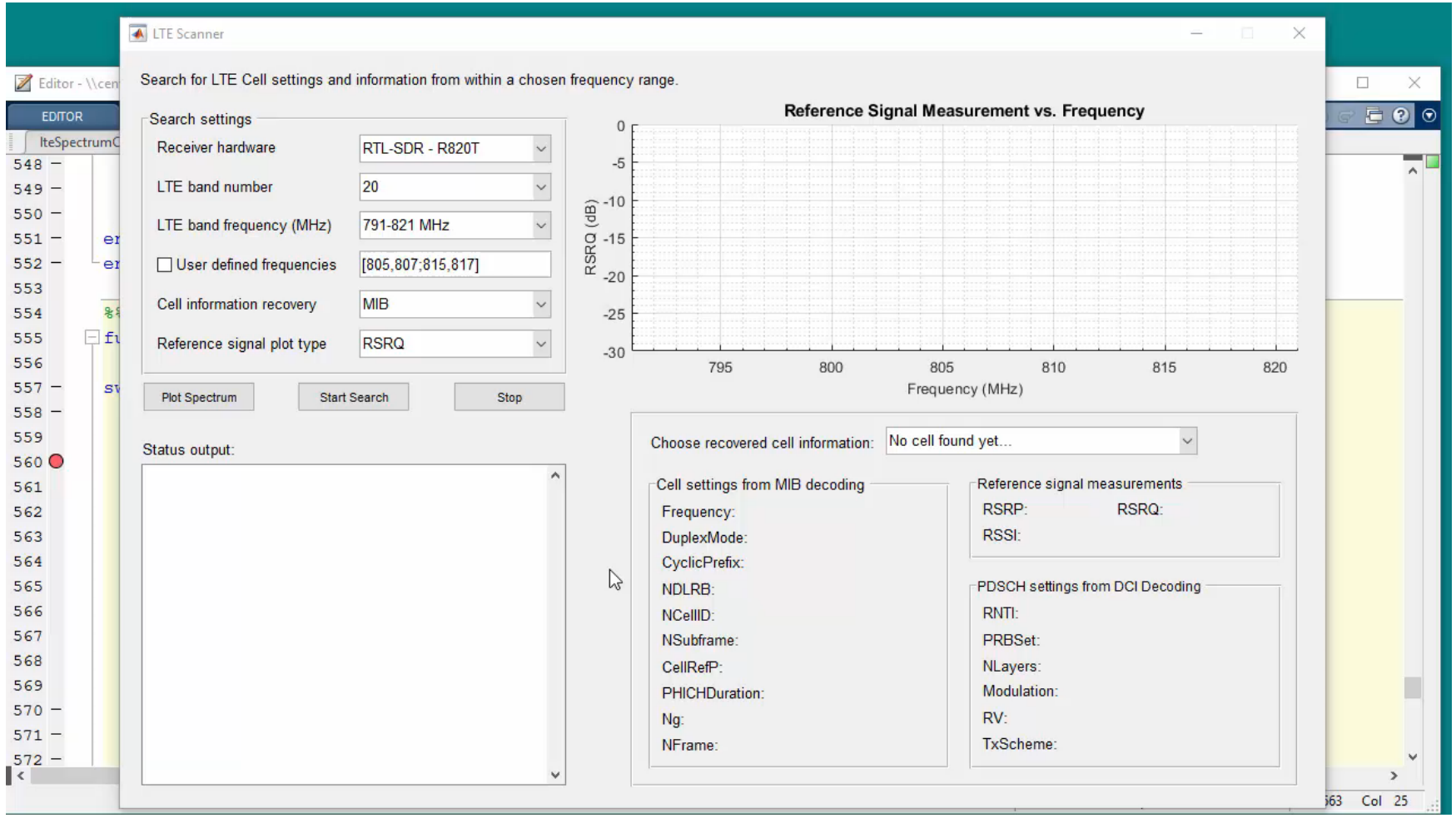
Demo: Generating WLAN Beacons



Demo: LTE Scanner

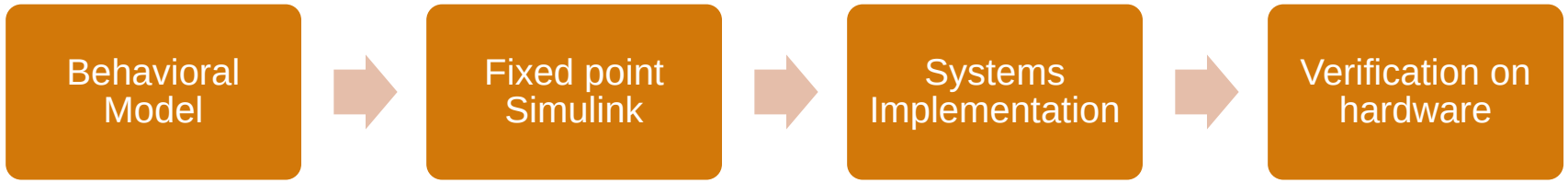


Demo: LTE Cell Scanner



Simulink for Wireless System Design

From Design to Prototype



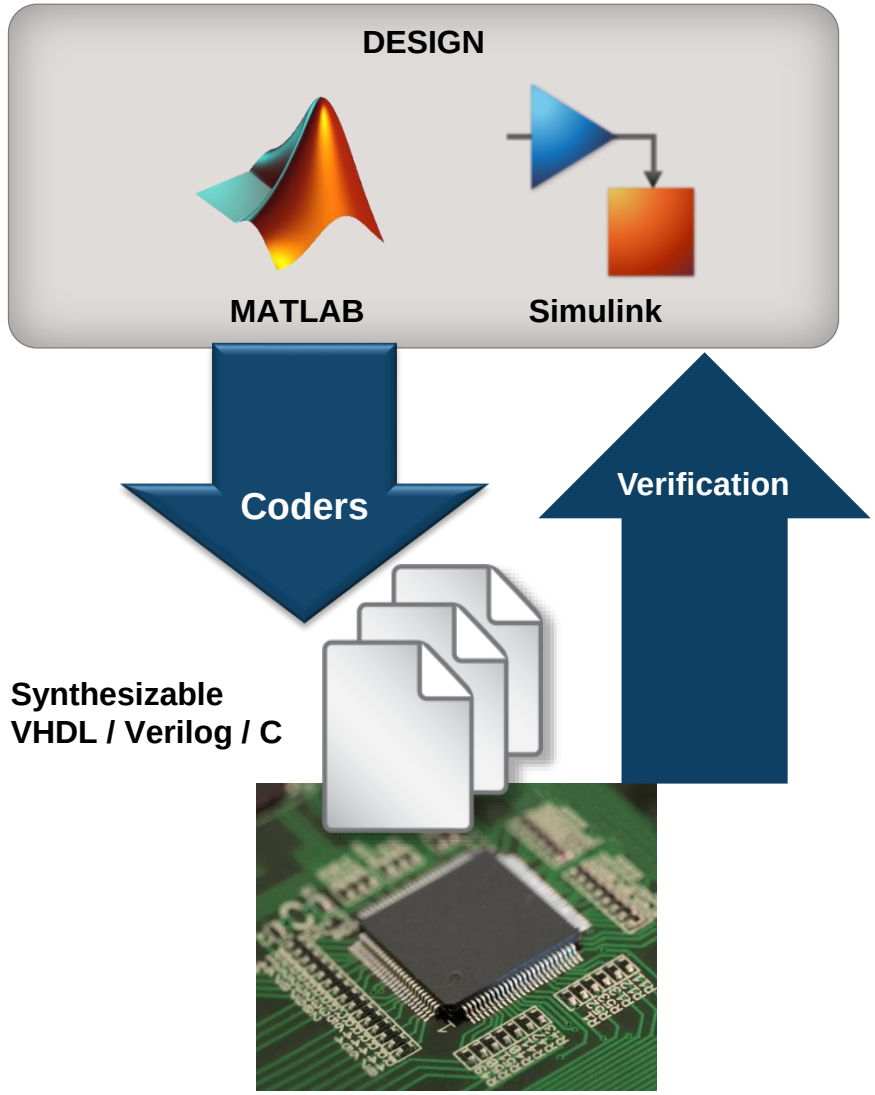
From Design To Hardware

MATLAB
- ✓ Large data sets
- ✓ Explore mathematics
- ✓ Data visualization

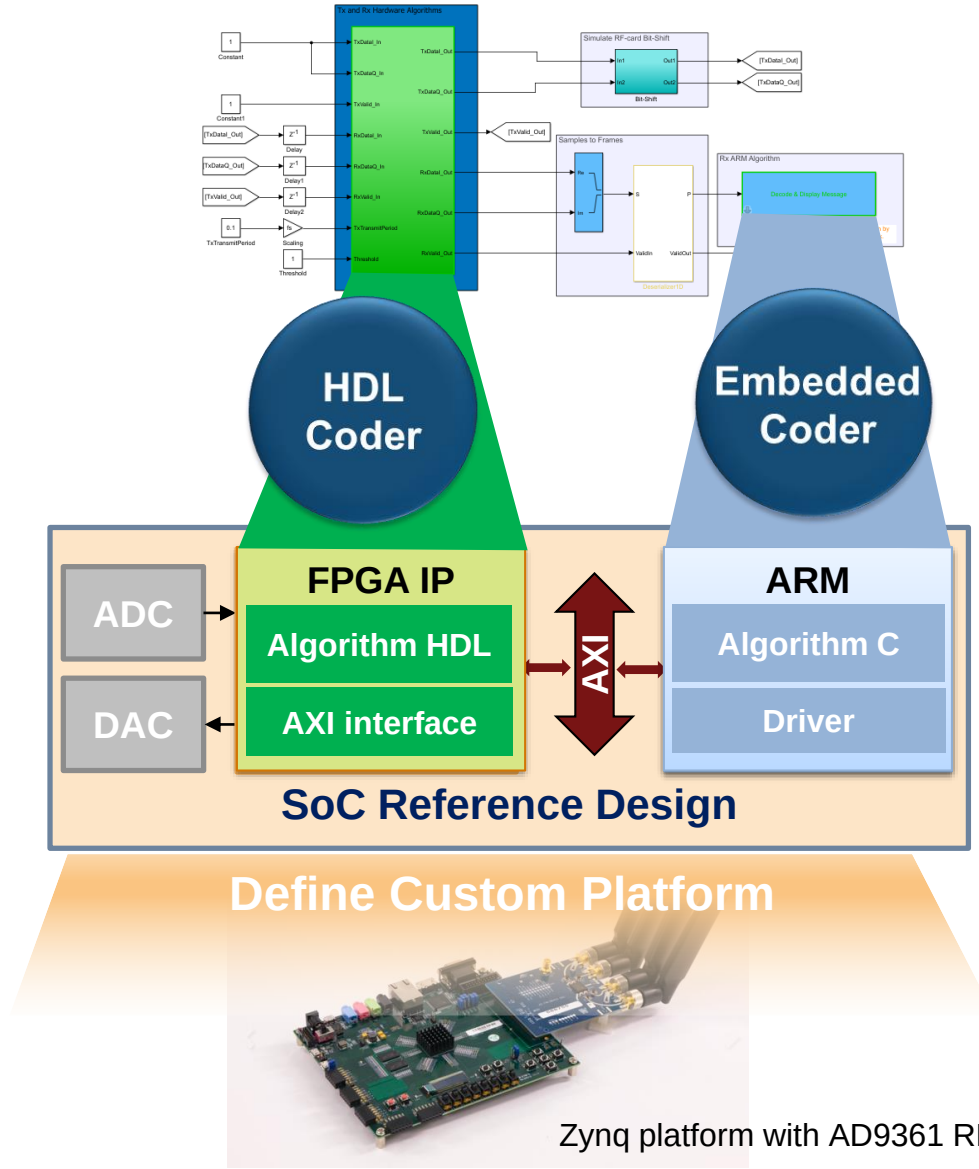
Simulink
- ✓ Parall chitectures
- ✓ Timing
- ✓ Data opagation

?

Targeting FPGA and ASIC
- ❑ Streaming design
- ❑ Implementation detail
- ❑ Architectural specification
- ❑ Verification



Generate C and HDL Code and Implement On Hardware

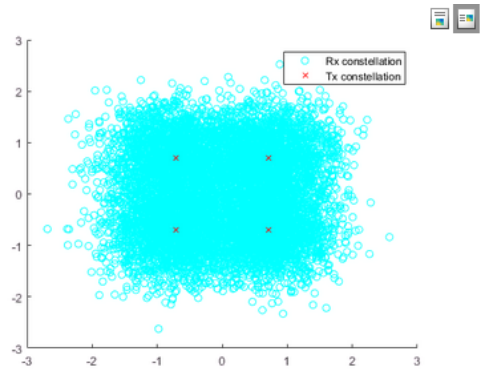


Zynq platform with AD9361 RF card

Verification: MATLAB reference model to FPGA implementation

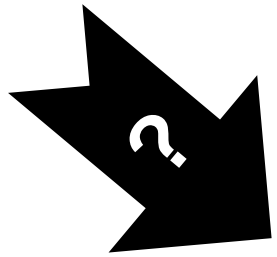
```
% generate bits for transmission
txBits = randi([0 1],6144,1);
% encode and modulate bits
codedData = lteTurboEncode(txBits);
txSymbols = lteSymbolModulate(codedData,'QPSK');

% add noise
noise = 0.5*complex(randn(size(txSymbols)),randn(size(txSymbols)));
rxSymbols = txSymbols + noise;
```

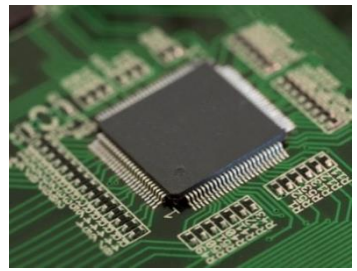
```
% plot transmitted and received symbols
scatter(real(rxSymbols),imag(rxSymbols),'co'); hold on;
scatter(real(txSymbols),imag(txSymbols),'rx')
legend('Rx constellation','Tx constellation')
```



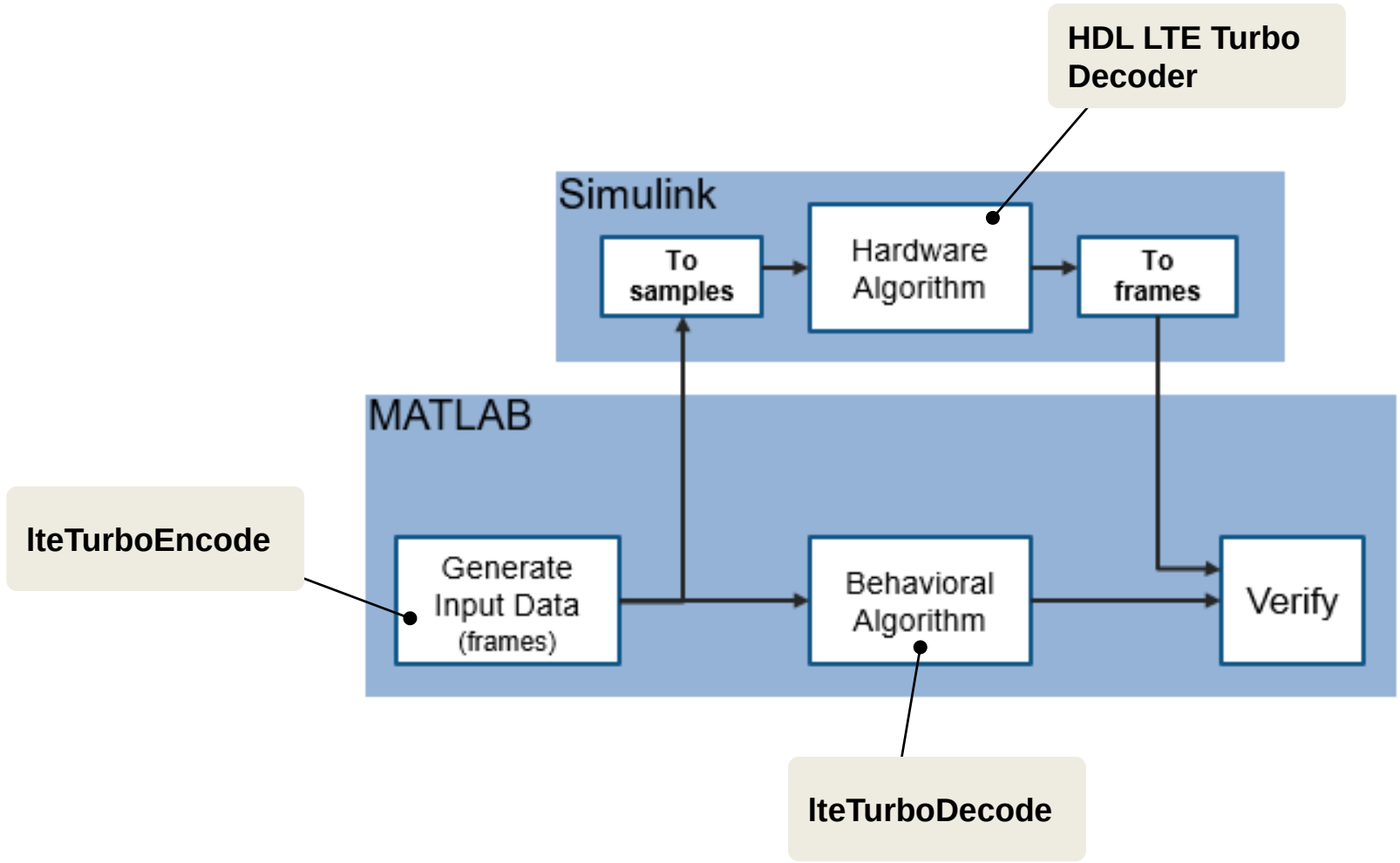

```
% demodulate data
softBits = lteSymbolDemodulate(rxSymbols,'QPSK','Soft');

% decode
rxBits = lteTurboDecode(softBits);

% check number of errors
numberErrors = sum(rxBits ~= int8(txBits))
```

```
numberErrors = 0
```



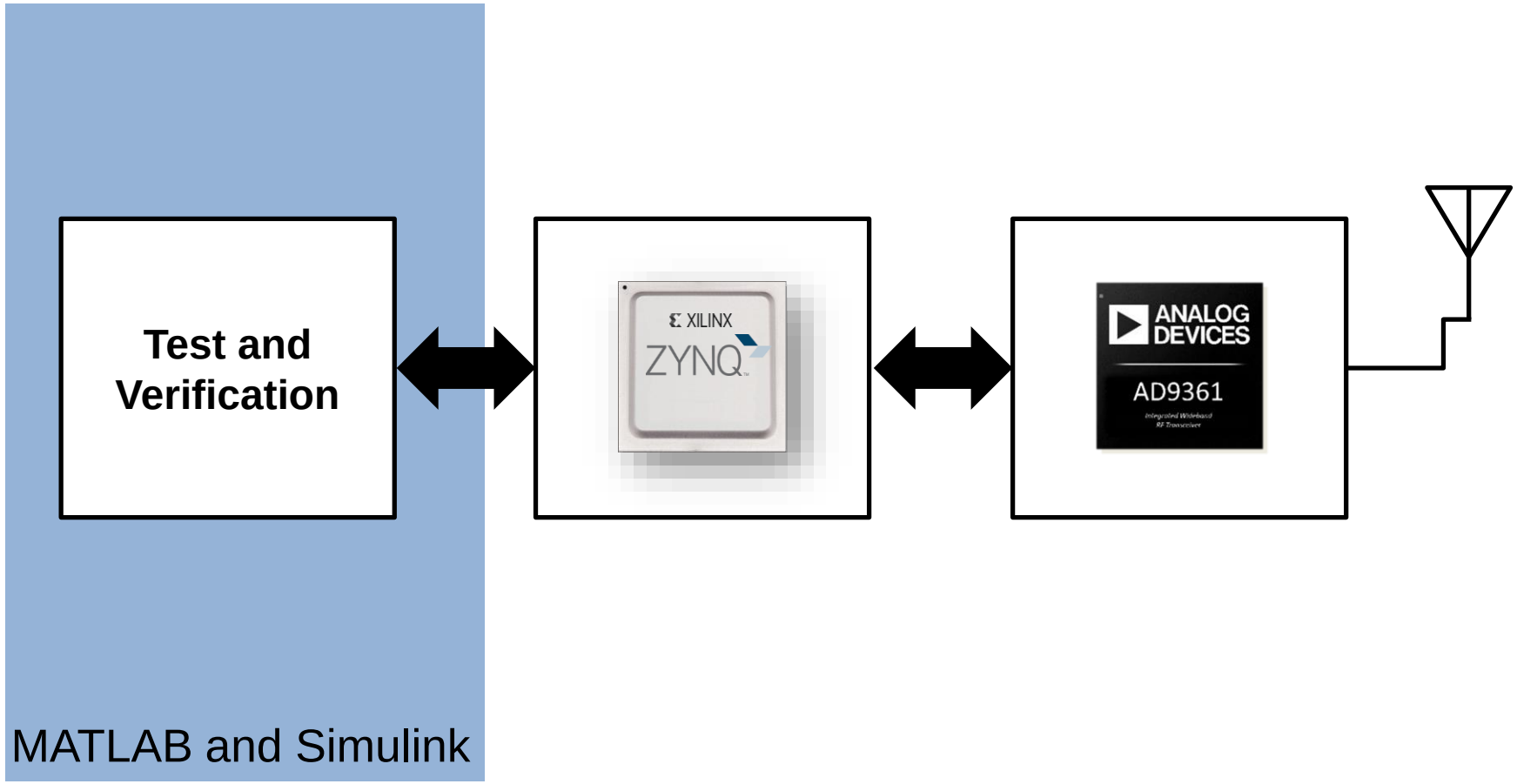


Demo - Verify Turbo Decoder with LTE System Toolbox

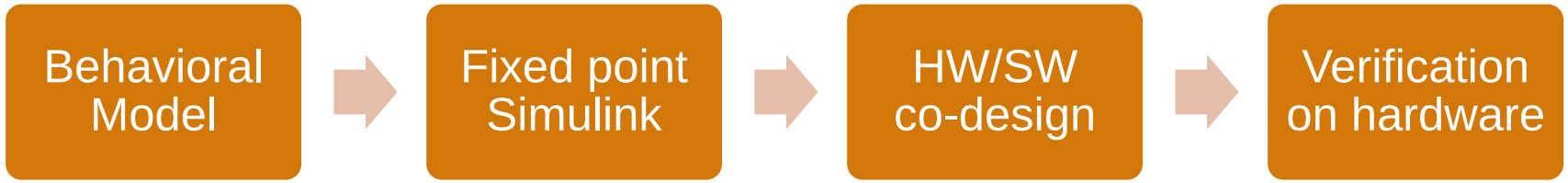


Demo: LTE Turbo Decoder

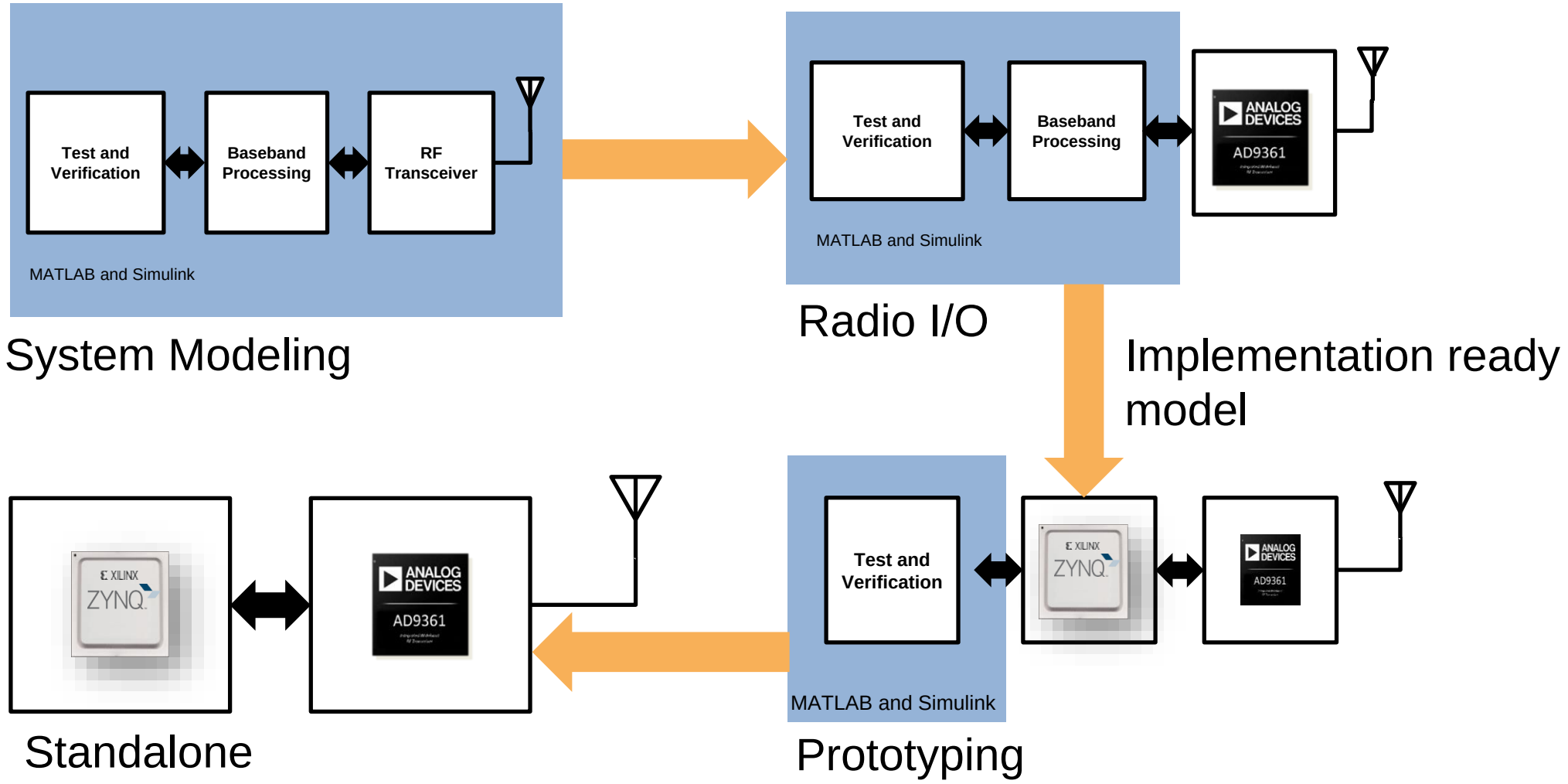
Verification via SDR Prototyping



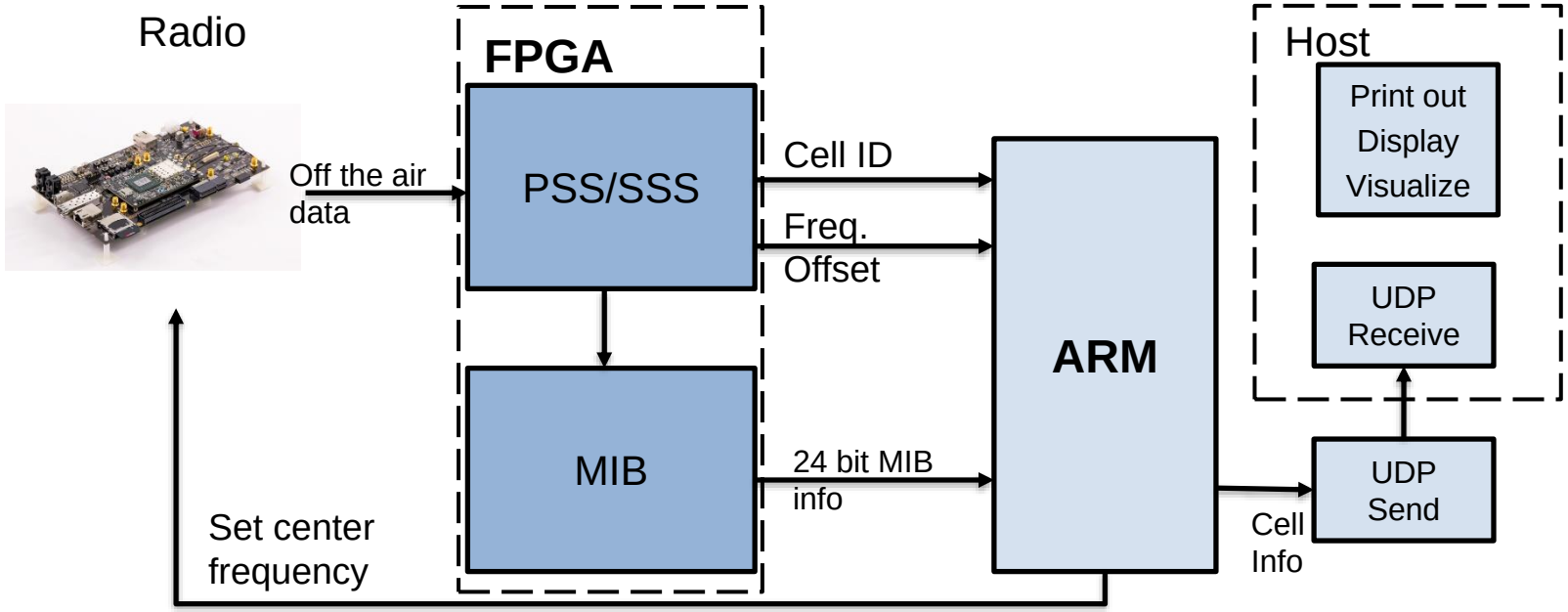
From Design to Prototype



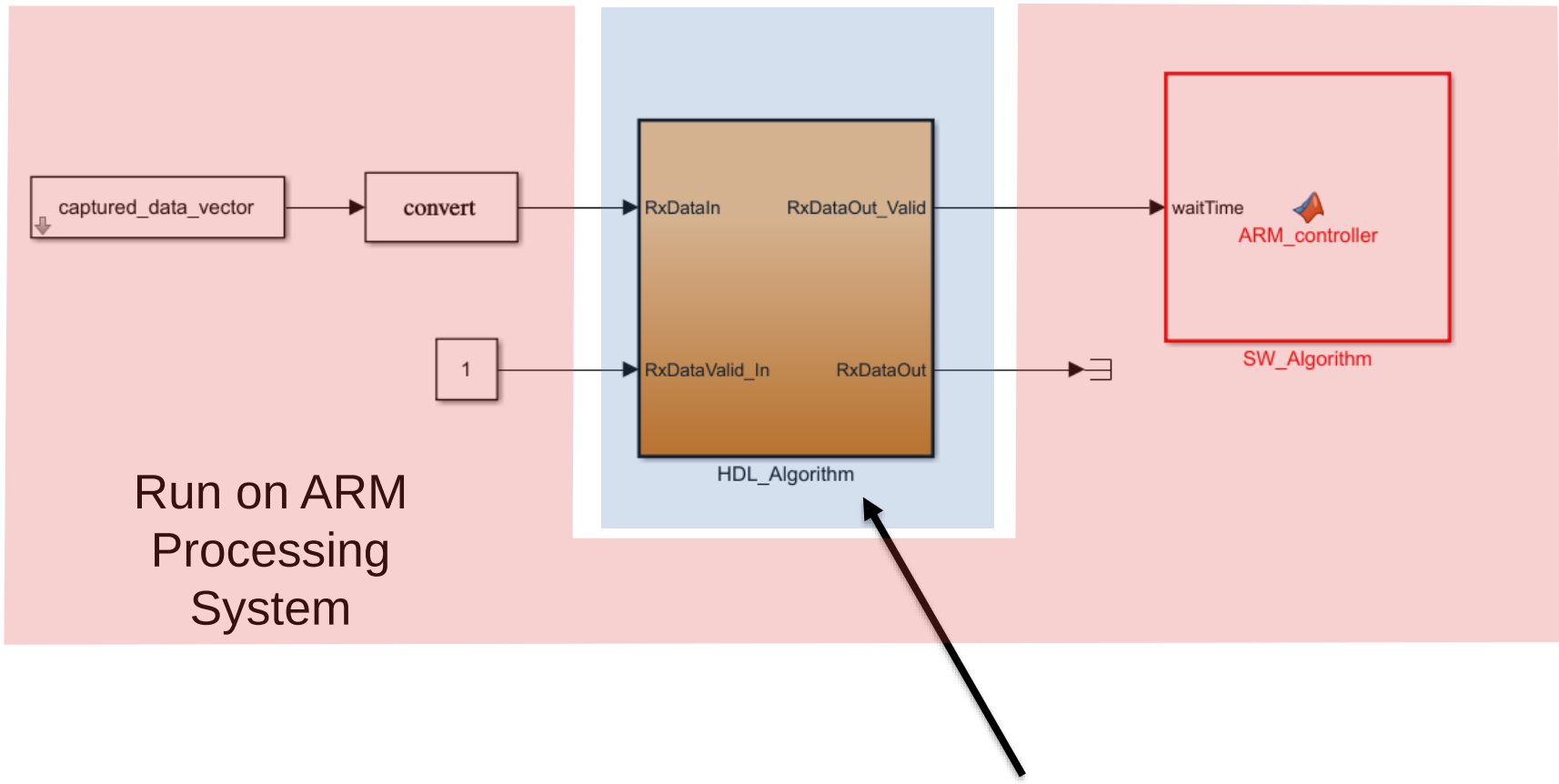
Verification via SDR Prototyping



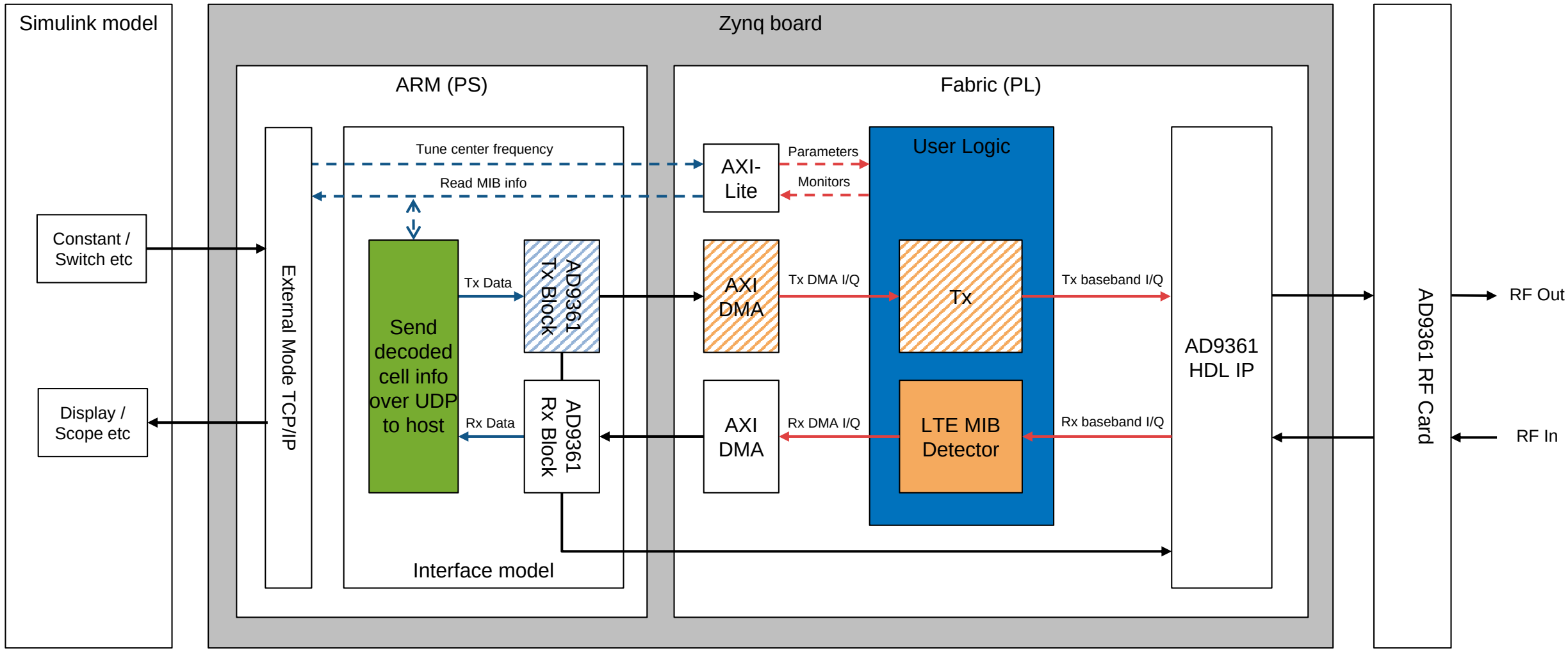
Real time LTE Frequency Scanner



Targeting an algorithm to the FPGA and ARM



HW/SW Co-Design Implementation of MIB Detector



SoC Workflow: HW/SW Co-design

SIMULINK

SDR HSP
Zynq HSPs
Vision HSP

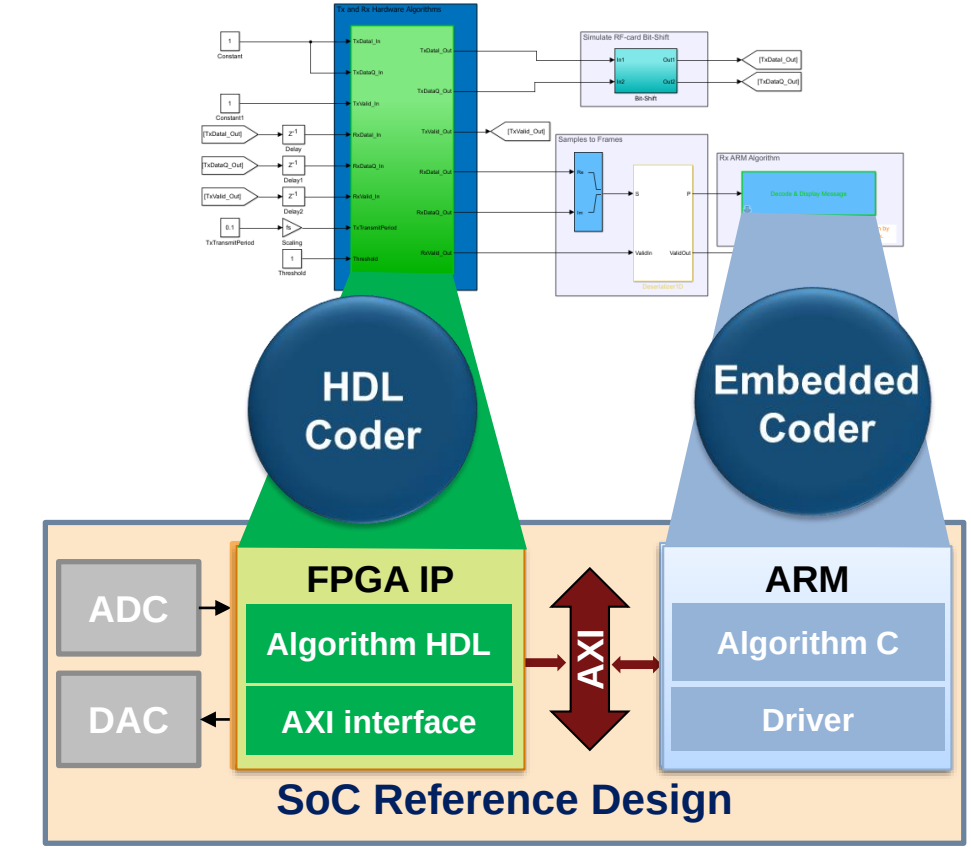
Algorithm design → **Prototyping algorithm on supported hardware system**

Algorithm Modeling → **Algorithm Simulation with test bench** → **Choose a shipping ref design in HSPs** → **Test on hardware system** → **Does the ref design represent the end platform?**

Yes

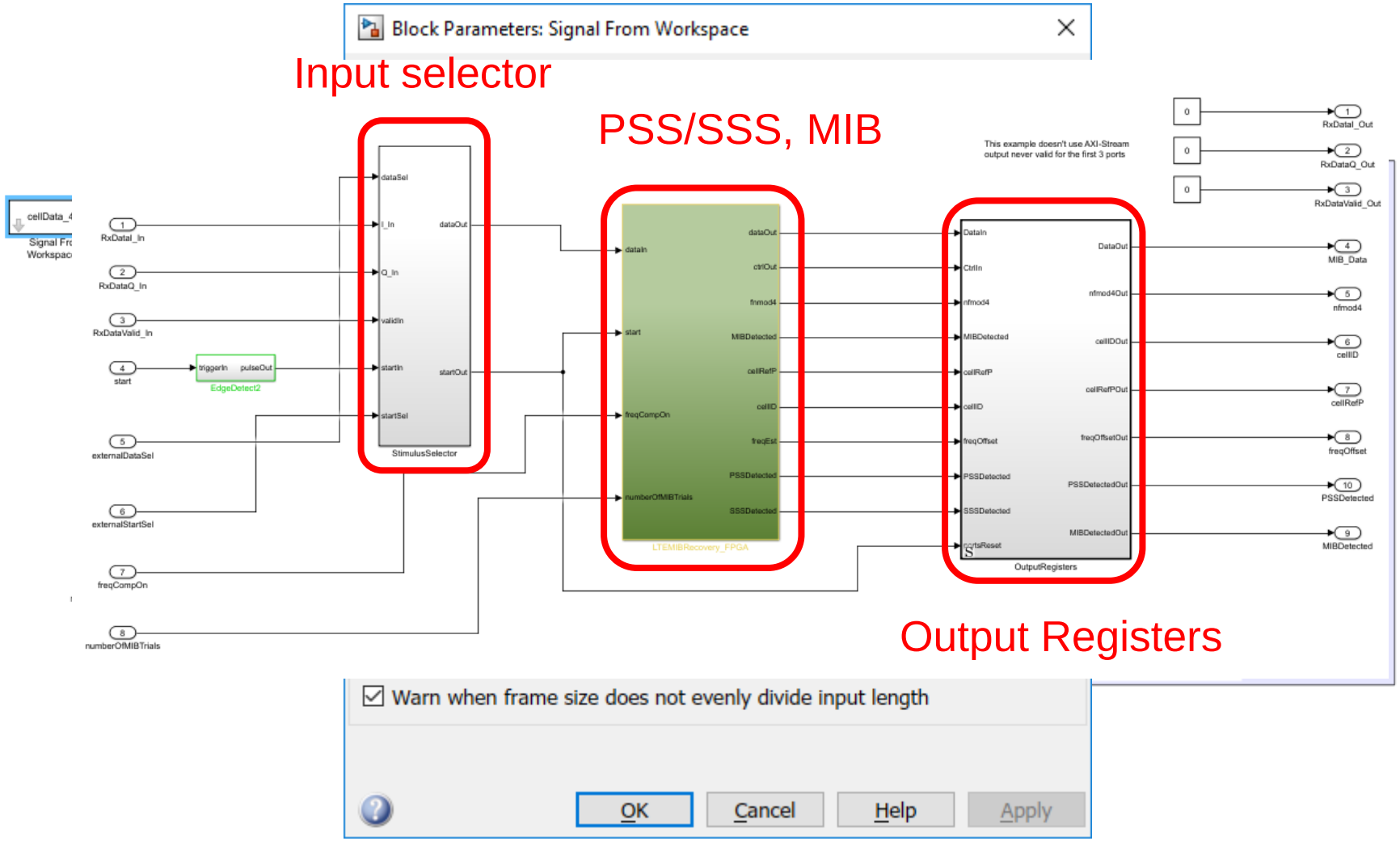
No → **Build a custom reference design**

Generate C and HDL code and implement on hardware



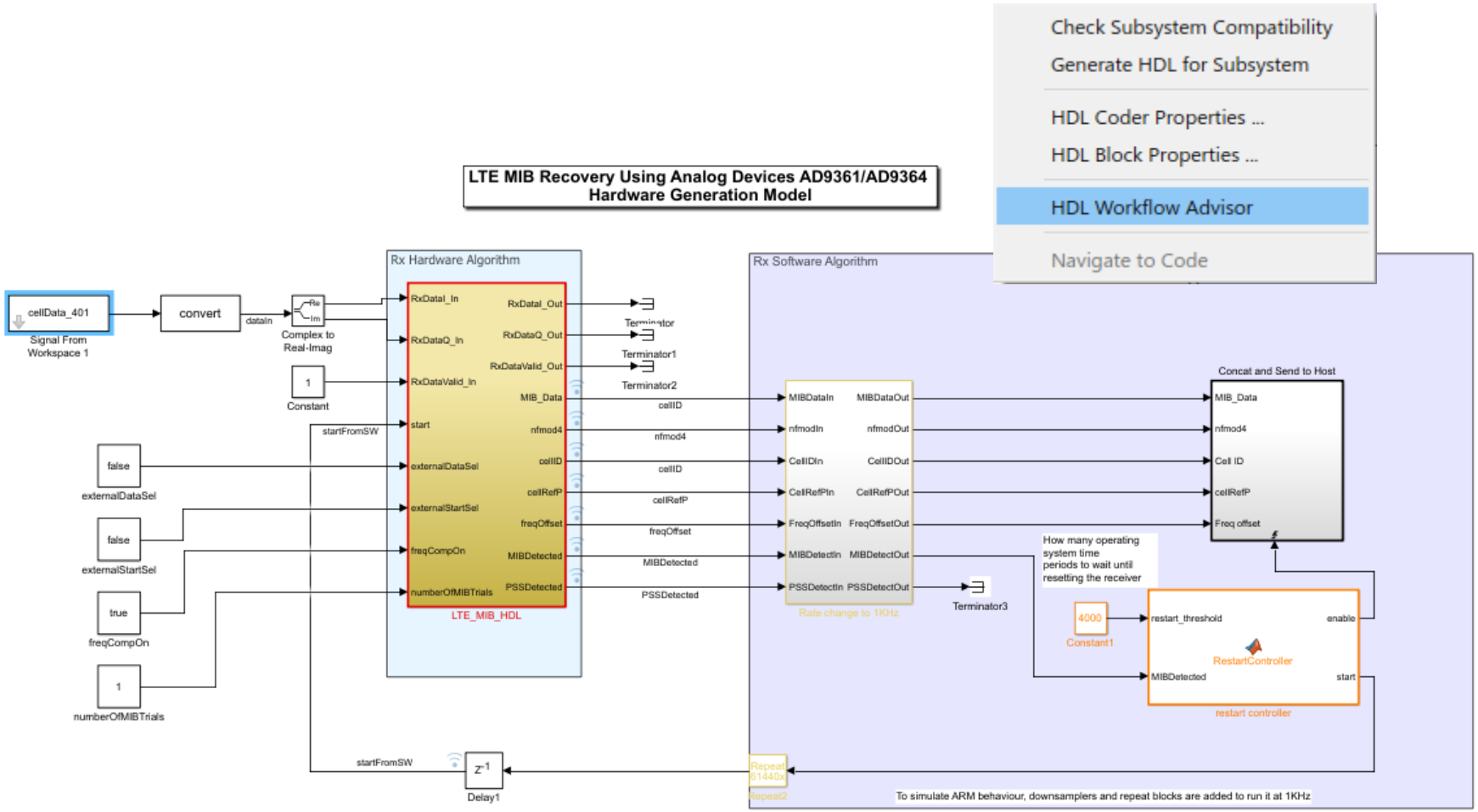
Zynq platform with AD9361 RF card

LTE Cell Scanner Example: Algorithm



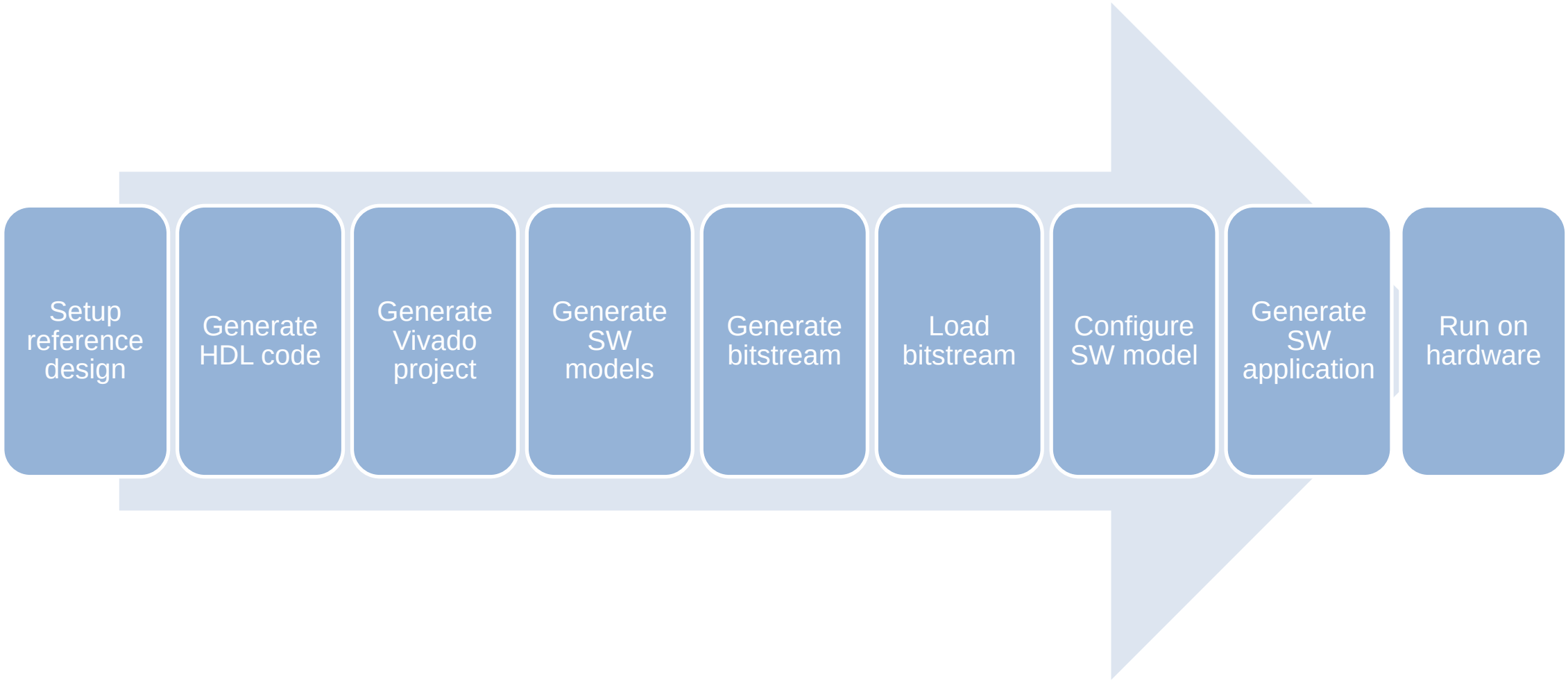
- Model algorithm
- Generate FPGA bitstream
- SW interface model
- Run on hardware

LTE Cell Scanner Example: Generation

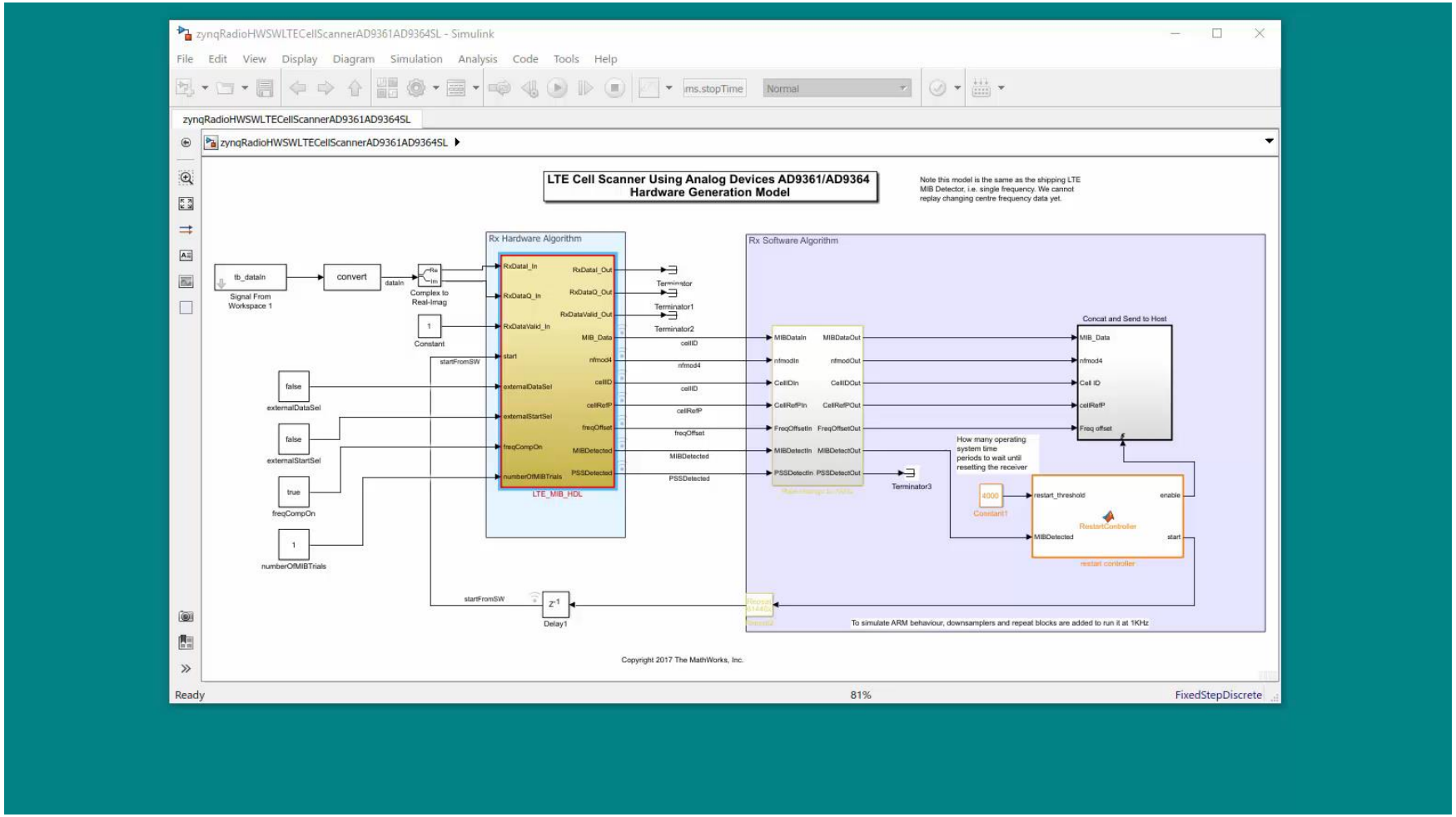


- Model algorithm
- Generate FPGA bitstream
- SW interface model
- Run on hardware

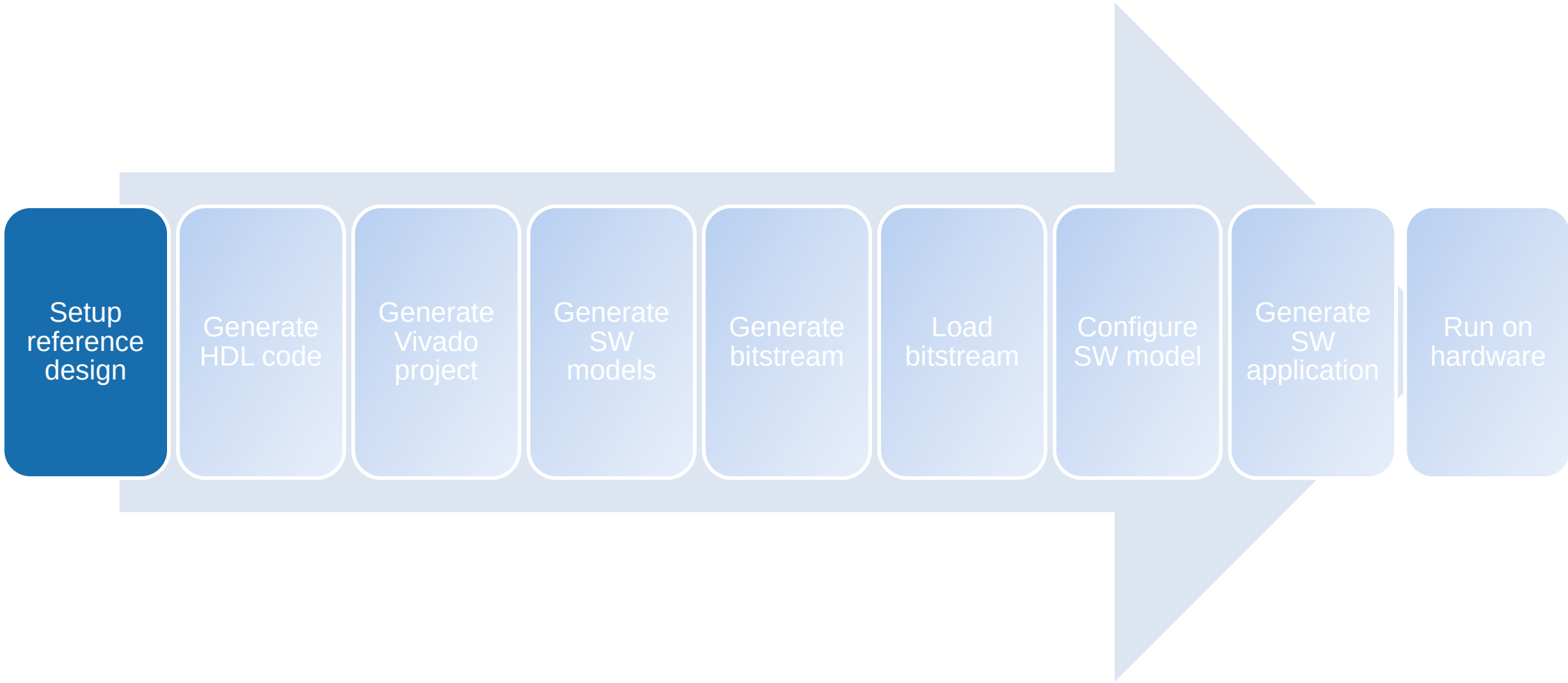
Targeting workflow



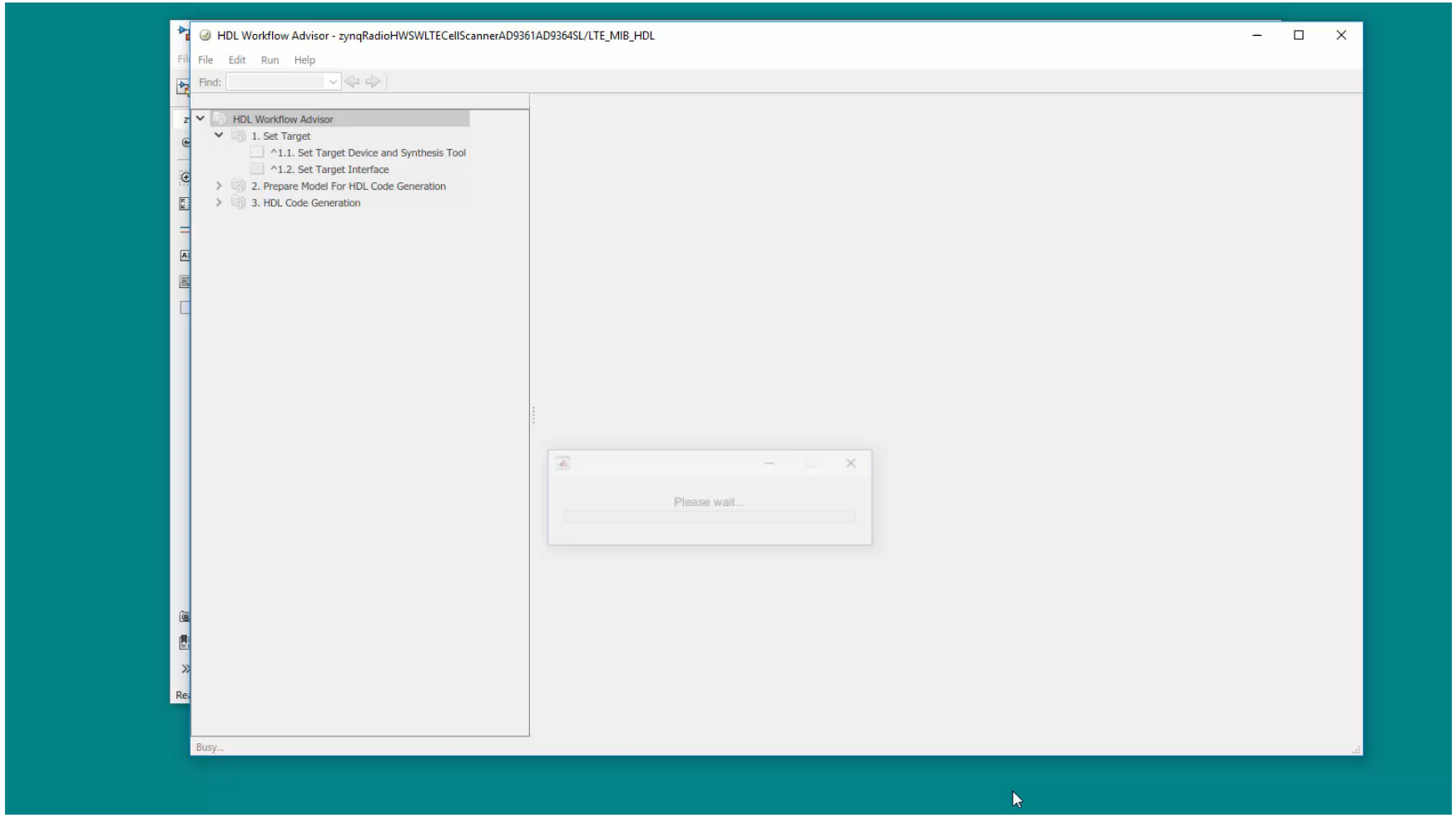
Video: Compile Model



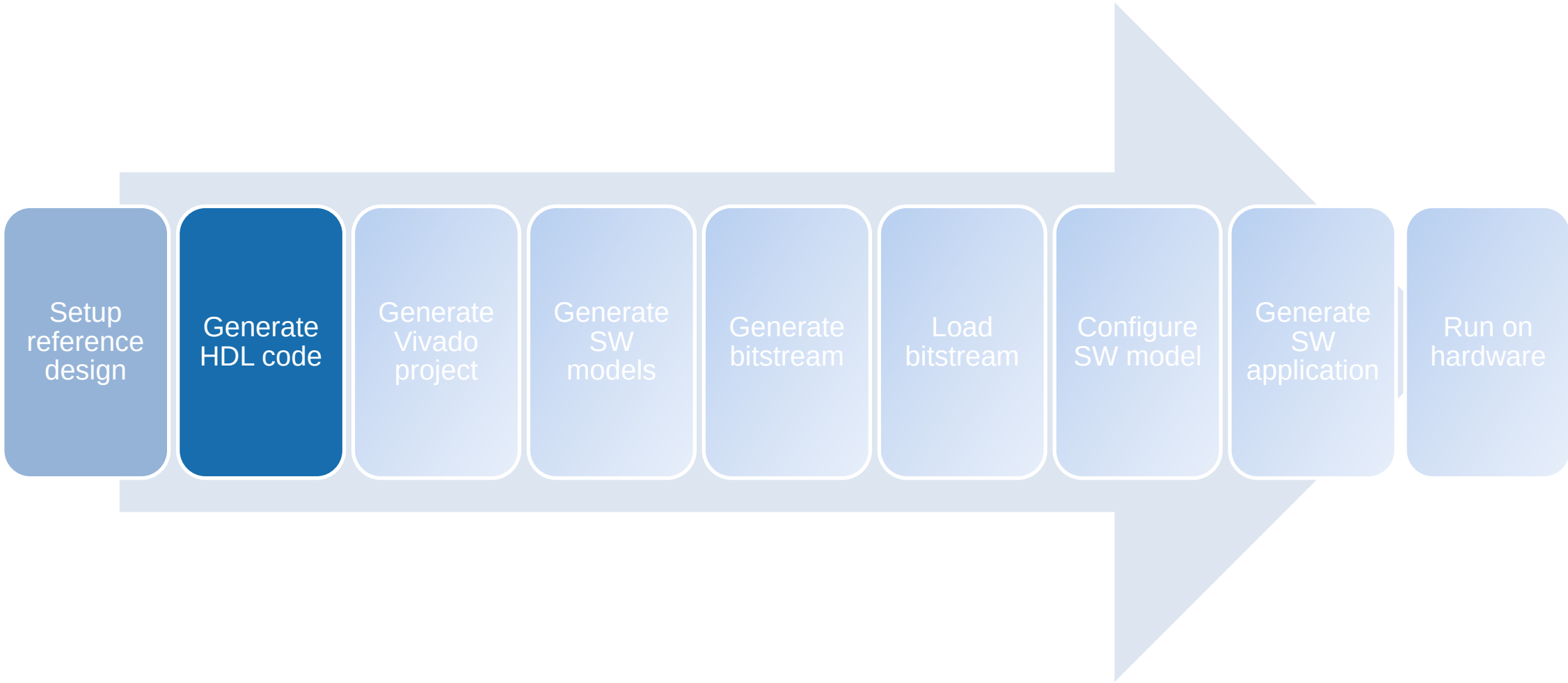
Targeting workflow



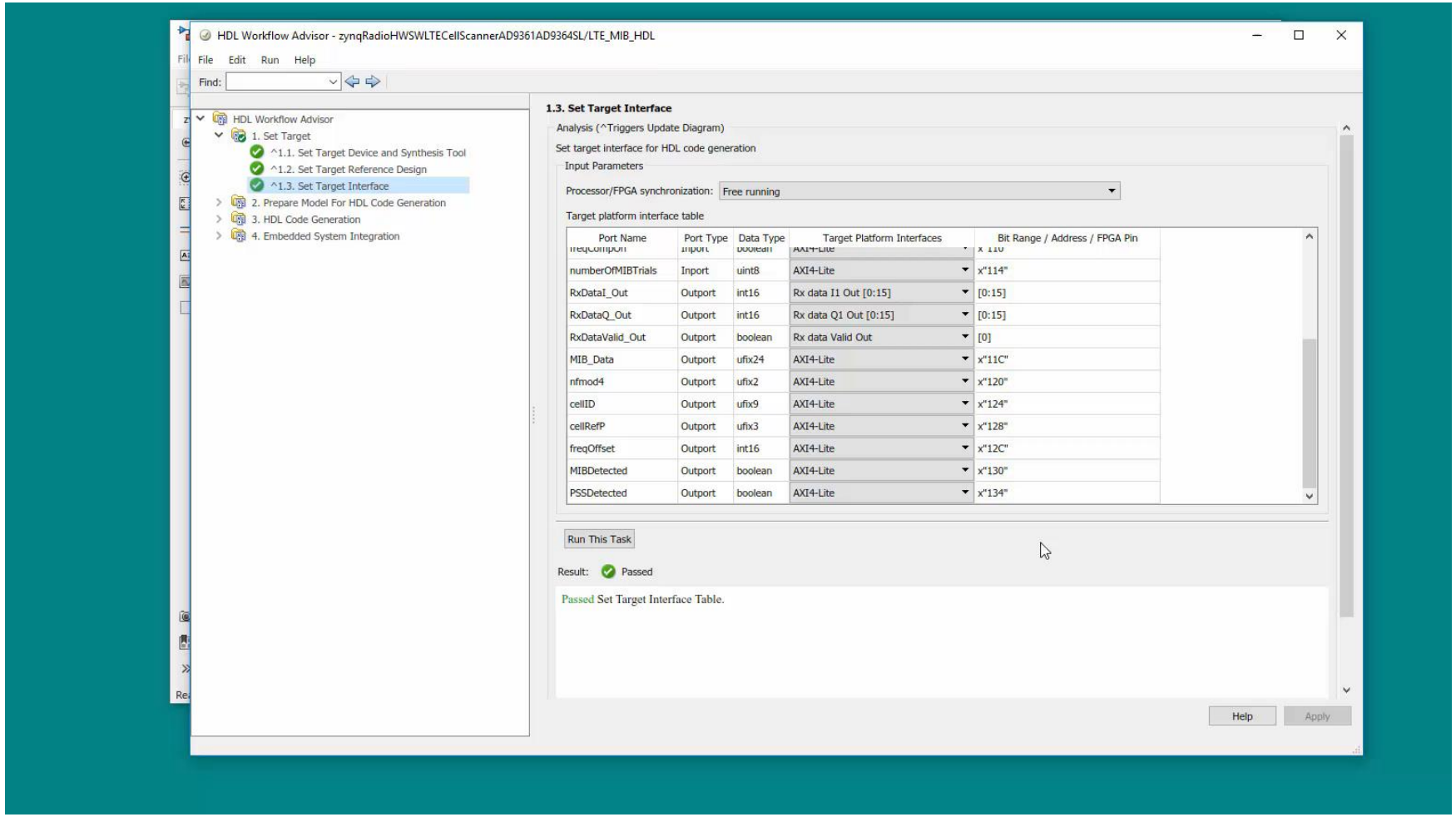
Video: Setup reference design



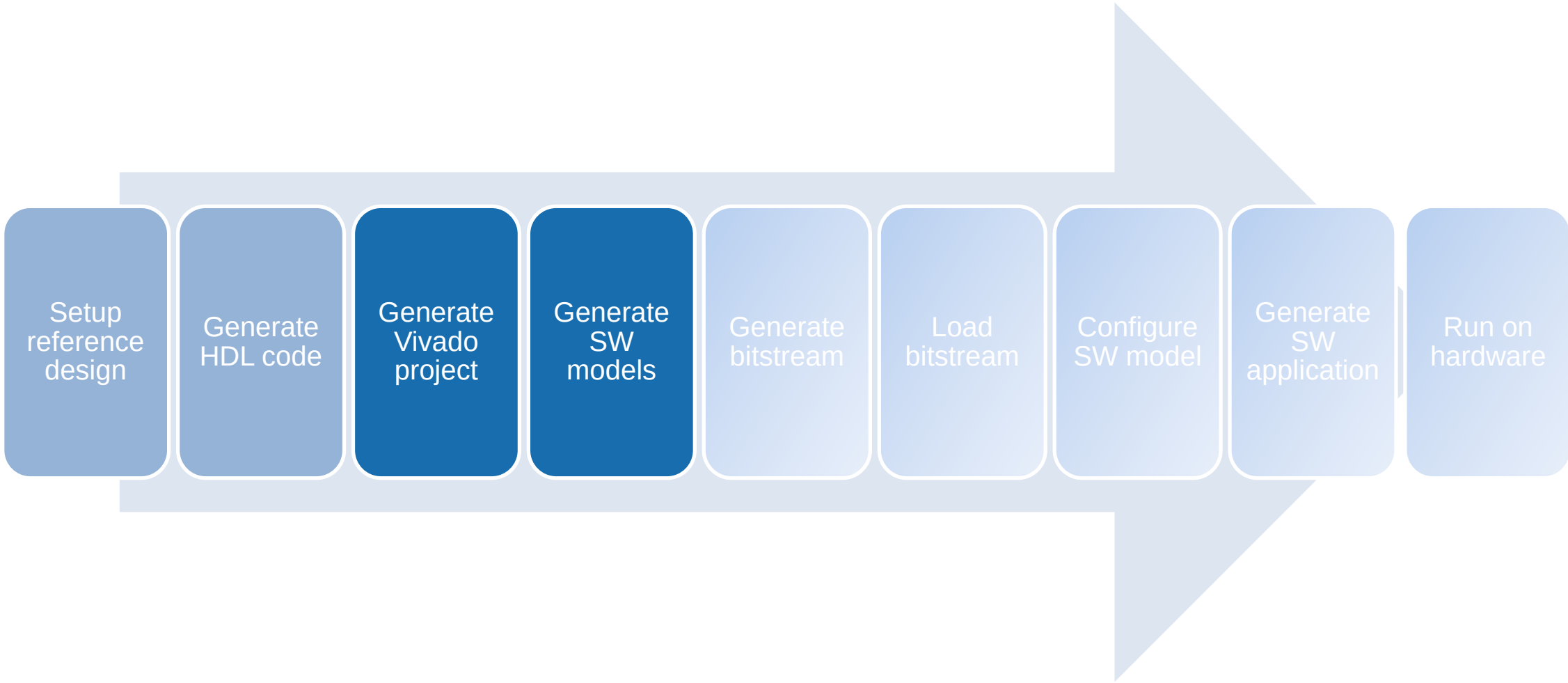
Targeting workflow



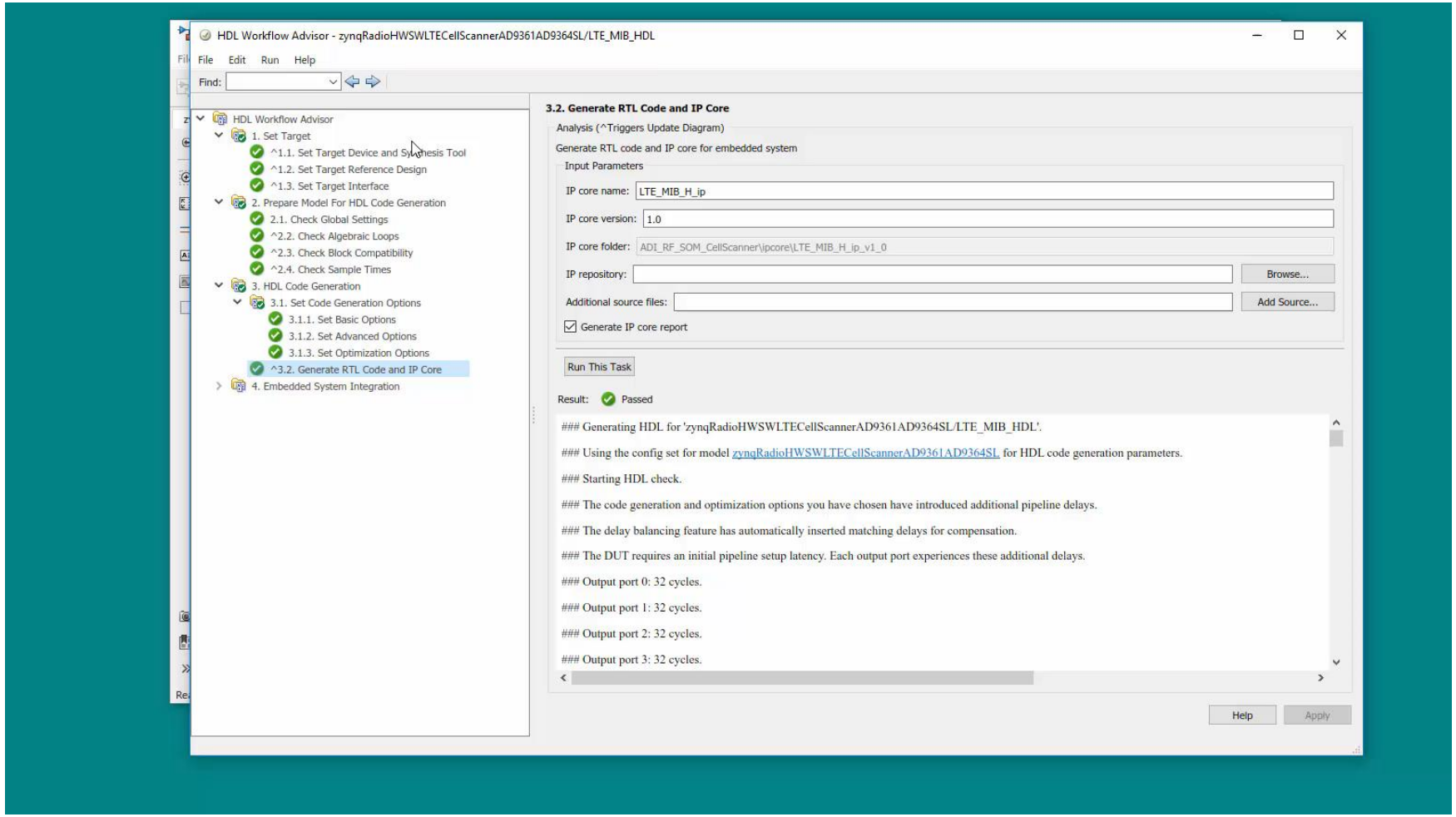
Video: Generate HDL code



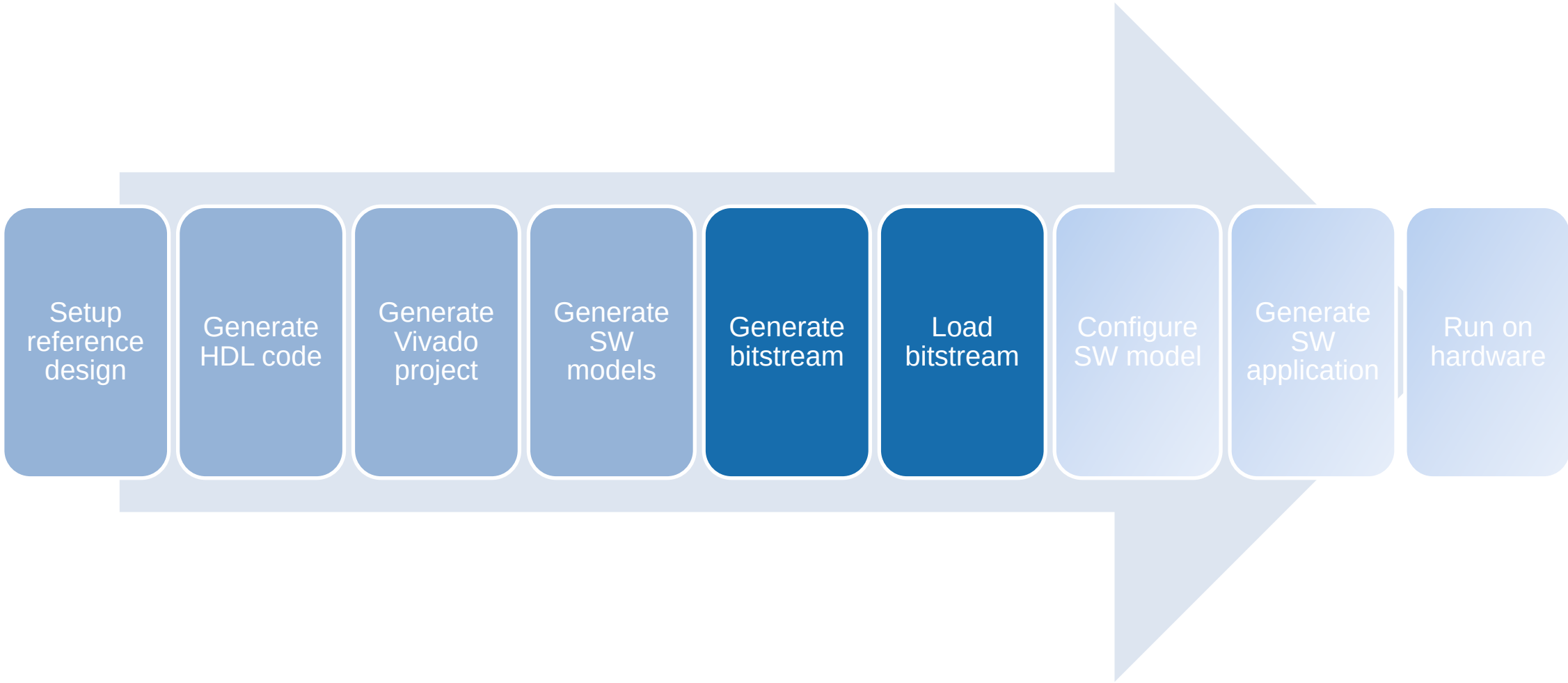
Targeting workflow



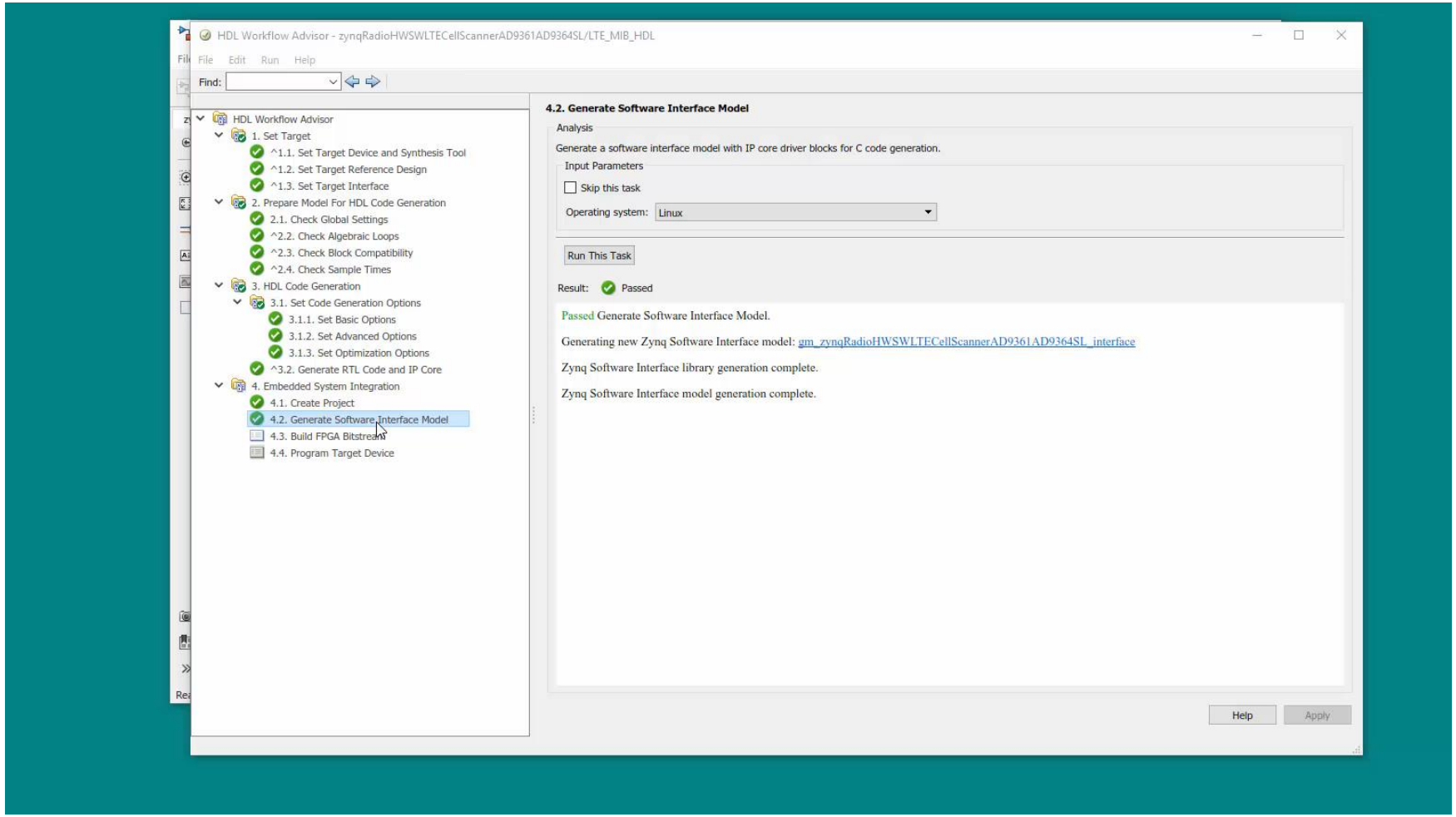
Video: Generate Vivado project and software models



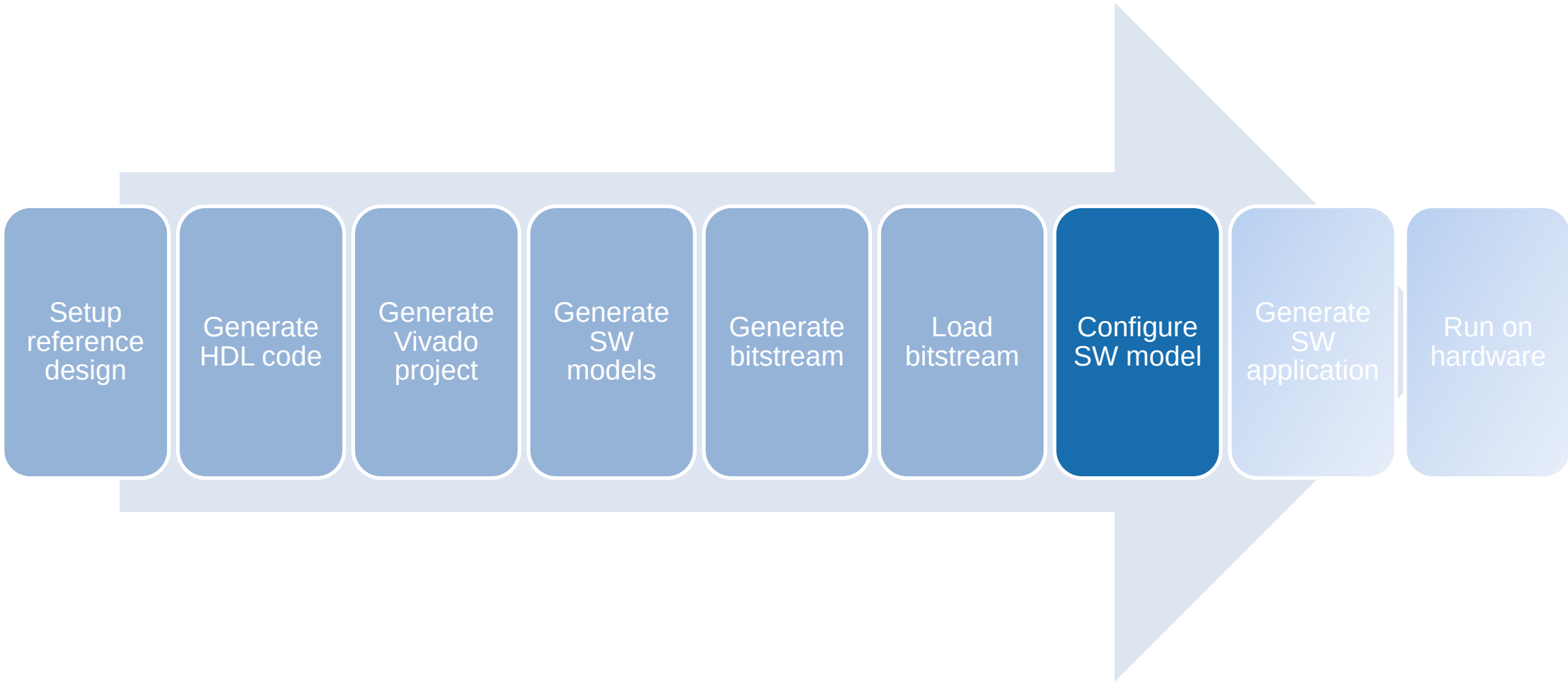
Targeting workflow



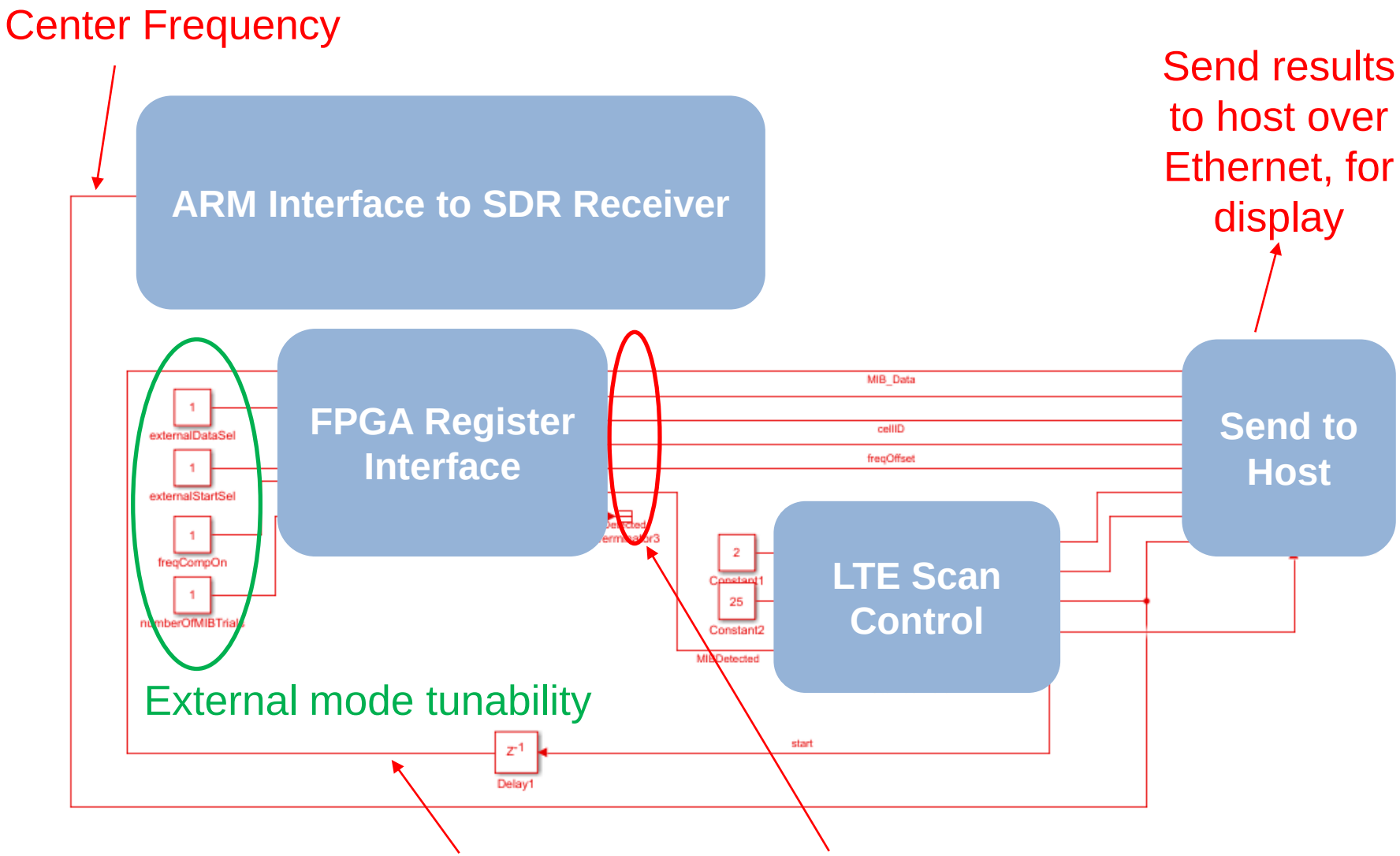
Video: Generate bitstream



Targeting workflow

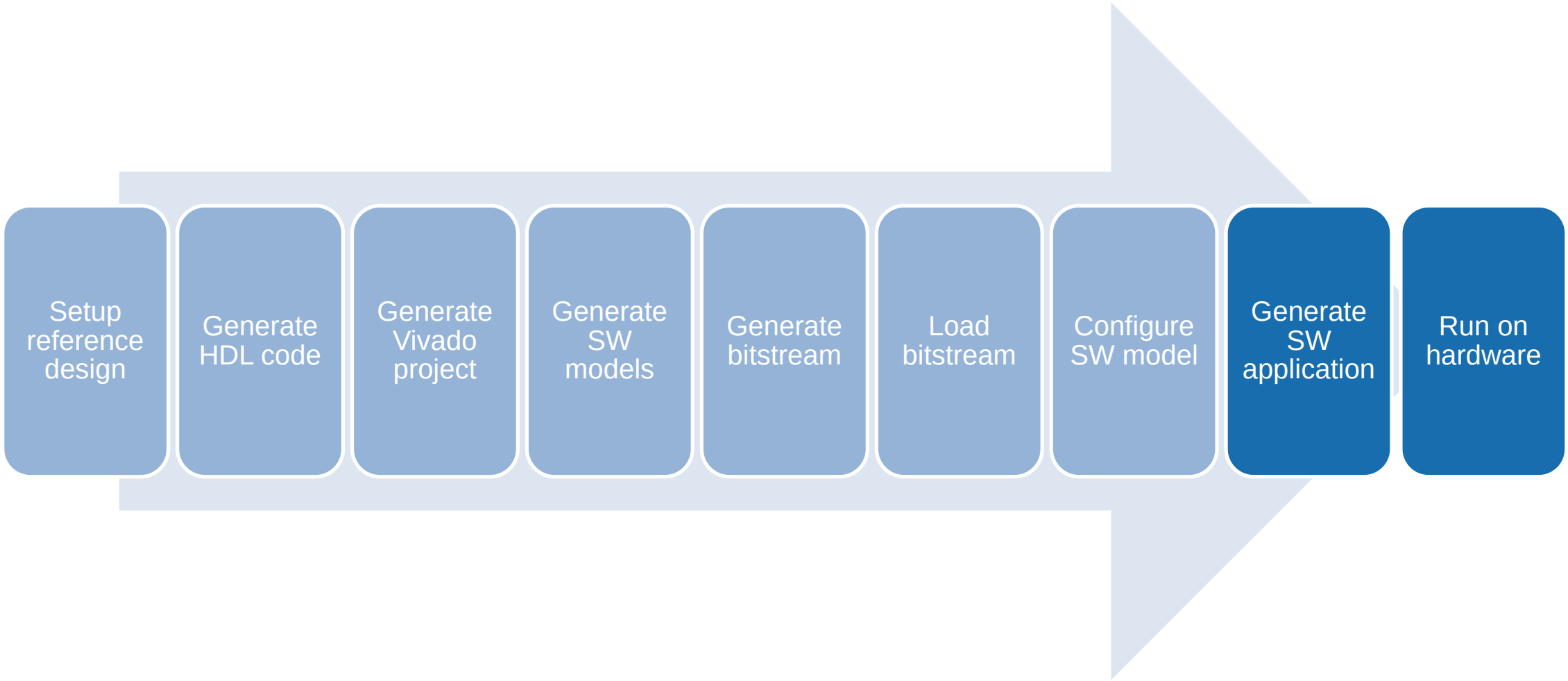


LTE Cell Scanner Example: Software

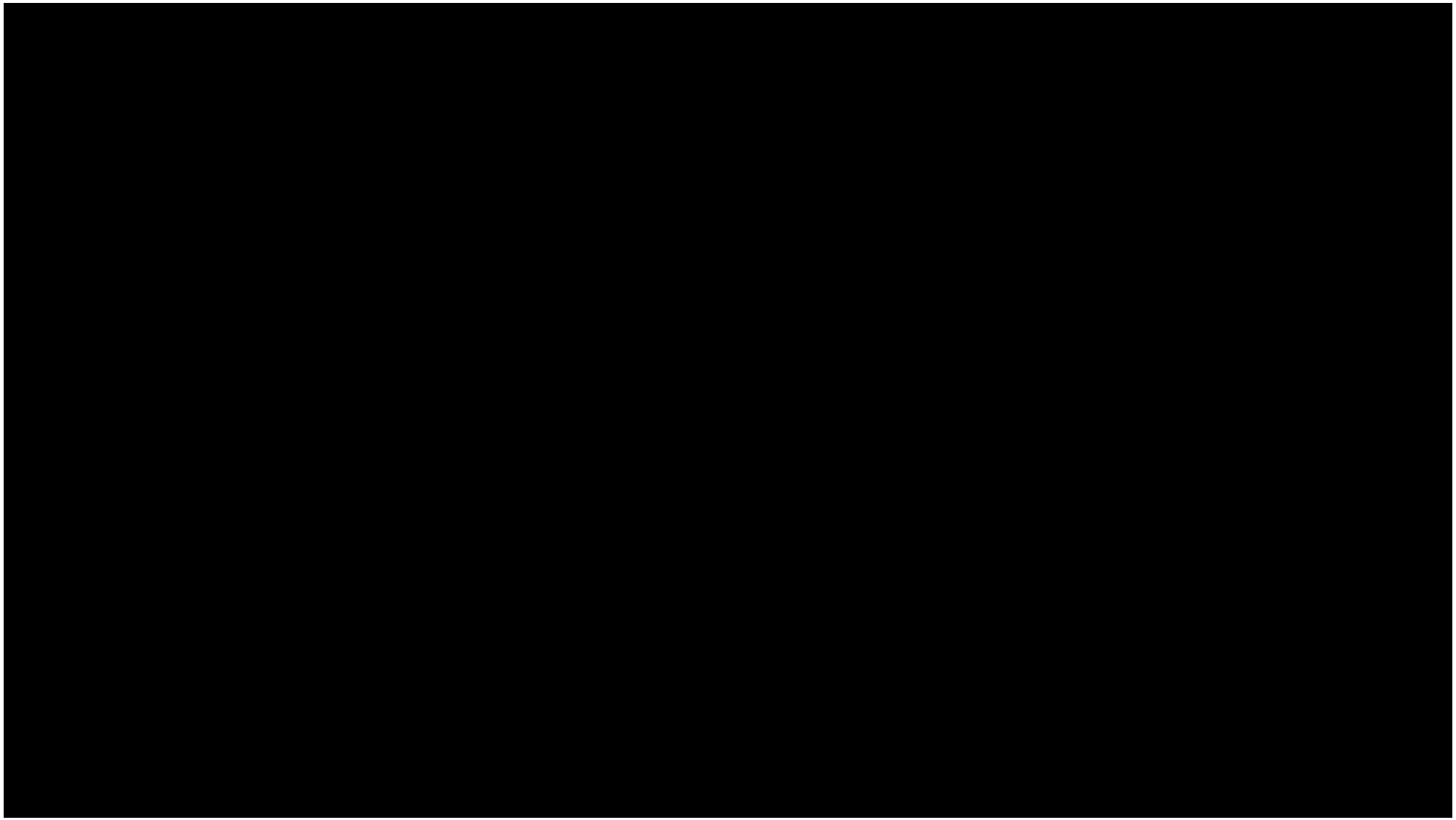


- Model algorithm
- Generate FPGA bitstream
- SW interface model
- Run on hardware

Targeting workflow



Video: Run on hardware



Thank you!