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Deploying Motor Control Algorithms to a TI C2000[™] Dual-core Microcontroller

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What is the most challenging part in your Motor Control Development process?

- 1. Motor control algorithm design
- 2. Write efficient code for embedded processors
- 3. Identify hardware and software architecture for multicore processors

Key Takeaways

- Simulate sensorless field-oriented control (FOC) on a dyno setup
- Complete Model-Based Design workflow for multicore microcontroller
- Hardware component and device driver behavior simulation
 - Enhanced on-device profiling





Dual CPUs PMSM Dyno Testing



Workflow for Implementing Field-Oriented Control



Simulate Motor Control System



Demo – PMSMs Dyno Model in FOC Sensorless Control



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Challenges of Deployment on the Embedded Systems..

Model

- System requirement
 - TI C2000 dual-core processors
- Controller sample rate is 20kHz
 - Field-oriented control (FOC)
 - Sensorless control
 - Dyno setup (2 motors)
- No sensor delays in my model
- ADC-PWM synchronization

Multicore Processor

- How to implement and partition controls into two separated cores?
- How to communicate between CPU1 and CPU2?
- How to make sure task execution meets software requirement?

Simulate Motor Control System with Peripherals and Task Execution



Model Multicore application Using SoC Blockset



Plant Subsystem



Input 0 voltage till Motor 2 torque control is enabled.

Hardware vs Simulation Analysis



Model Configuration

		soc_ayno_top " -	Simulink prerelease	use					
		SIMULATION	DEBUG	MODELING	FORMAT	SYSTEM ON CHIP	APPS	MODEL BLOCK	
		Hardware Board TI Delfino F28379D HARDWAI	LaunchPad RE BOARD soc_dyno_top dyno_top	Configure, Build & Deploy BUILD & DEPLOY	Hardware Settings	Peripheral Configuration	Execution Report RESULTS		
Configuration Parameters: soc_d	yno_top/Configuration (Active)		Top Model	:	×	Configuration	on Parameters: soc	_dyno_cpu1_speedcontrol/Configuration (Active)	
Q Search						Q Search		Mode	el l
Solver Data Import/Export Math and Data Types Diagnostics Hardware Implementation Model Referencing Simulation Target Code Generation Coverage HDL Code Generation Simscape Simscape Multibody	Hardware board: TI Delfin Code Generation system ta Device vendor: Texas Inst > Device details Feature set for selected ha Simulink or Embedded SoC Blockset Hardware board settings Processing Unit: None > Design mapping > Task profiling in simula > Task and memory sim	o F28379D LaunchP arget file: <u>ert tic</u> ruments rdware board: d Coder Hardware Sr ation	ad Device type: C upport Package	 ▼ 2000 ▼ 		Solver Data Impor Math and I > Diagnostic Hardware Model Refe Simulation > Code Gene Coverage > HDL Code	t/Export Data Types s mplementation rencing Target eration Generation	Hardware board: TI Delfino F28379D LaunchPad Code Generation system target file: ert.tlc Device vendor: Texas Instruments Device type Device details Feature set for selected hardware board: Osimulink or Embedded Coder Hardware Support Package SoC Blockset Hardware board settings Processing Unit c28xCPU1 Design mapping Task profiling on processor Target hardware resources 	 ▼ C2000 ▼
		ОК	Cancel	Help	·			OK	Help Apply

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Task Manager



- Model/Simulate
 - Periodic/async tasks
 - Task priorities
 - Latencies
 - Duration as normal distribution

Р	ercent N	lean	SD	Min	Max				
Specify task duration times as a normal distribution, or a combination of multiple normal distributions.									
Task o	Task duration settings								
Specify	Specify task duration via: Dialog								
🗌 Play	recorded tas	k exec	ution sequer	nce					
Main	Simulation								

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ADCInt properties

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0.7 0.8 0.9

1.0 1.1

1.2 1.3 1.4

1.6

1.5

1.7 1.8 1.9 2.0

Inter-Processor Communication with IPC Blocks

Block Parameters: Interprocess Data Channel 1

Model the communication buffering and delay



Interprocess Data Read



Interprocess Data Write



Interprocess Data Channel

Interprocess Data Channel								
Model data channel between two processes.								
Interprocess Data Write block writes the data to the channel from one process.								
Interprocess Data Read block reads the data from the channel from another process.								
Set Show event port to output a task trigger event when data is written to the channel.								
Parameters Define buffer size and timing delay Main Statistics Number of buffers: Image: Statistic statistics Propagation delay: 2e-6 Show event port Image: Statistic statistics								
OK Cancel Help Apply								

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🚹 Block Parameters: Interprocess Data Channel 1	\times						
Interprocess Data Channel							
Model data channel between two processes.							
Interprocess Data Write block writes the data to the channel from one process.							
Interprocess Data Read block reads the data from the channel from another process.	ı						
Set Show event port to output a task trigger event when data is written to the channel.							
Parameters							
Main Statistics Show number of Visualize buffer consumption and overwrites Show when suffer is overwritten							
OK Cancel Help Apply	1						

PWM Modeling

msg

PWM Interface

- PWM waveform simulation
- Event to synchronize with ADC or schedule a task

	Block Parameters: PWM Interface	X	x
	PWM Interface		
	Simulates the pulse width modulation	n (PWM)	+ End of Period End of Period
PWM	The block outputs either a switching the output. Also, it generates an "Event" which interrupts to trigger a control algorit	pulse width modulated waveform or pass the duty cycle value to can be used for synchronizing PWM with ADC or as PWM hm.	
~PWM	Main PWM output Phase	Event	
event	PWM waveform period (s):	50e-6	Image: Mid of Period End of Period Mid of Period Oscillator
	Output mode:	Switching -	Trigger
	Counter mode:	Up-Down -	
	Sampling mode:	End of PWM period	
	Dead time (s):	1e-6	
			Time
		OK Cancel Help Apply	

v in

3 3.3

SOC1 - Conversion

SOC1 - Conversion

event

SOC1 - S+H

SOC1 - S+H

ADC A

ADC B

SOC0 - S+H

SOC0 - S+H

SOC0 - Conversion

SOC0 - Conversion

ADC Modeling

start

X analog

ADC Interface

- Convert analog values to digital counts
- Model acquisition/conversion delays and trigger events

	Block Parameters: ADC Interface		×	1005	
	ADC Interface			n ⁴⁰⁹⁵ T	
	Simulates the analog-to-digital conversion	on (ADC)		D _{out}	$D_{out} = 4095 * V_{in}/3.3$
	The block samples the analog input bas digital value in counts. Also, it generate events which can be us	ed on a start event or sample time and outputs a representat sed for scheduling an algorithm.	ive	3072	zoomed in
	Acquisition time and Conversion time pa	arameter values sets the delays in the conversion.		lls	(4.)
event >	Main Multi channel Event			2048	
	Resolution (bits):	12	•	<u> </u>	
digital	Voltage reference (V):	3	-	ie in i	
	Acquisition time (s):	320e-9	:	2 ¹⁰²⁴	Analog Digital
	Conversion time (s):	240e-9	:	+	Input ADC Outputs
	Charge/discharge time constant (s):	0	:		
	Software triggered			0	
					Analog signal (volts)
		OK Cancel Help A	pply		
				1	End of Conversion

SoC Block set Key Functionalities – On-Device Profiling

- Real-time performance profiling on hardware, including
 - Task execution
 - CPU utilization
 - Communication buffering and delay
 - Real-time SDI view
 - Analysis report







Profile Tasks in Simulation and Hardware



Poll Question

Which topics do you want to discuss more?

- 1. Motor control design
- 2. Partition Multicore Processors
- 3. Simulate PWM/ADC and perform device profiling

Wrap Up

- Simulate sensorless field-oriented control (FOC) on a dyno setup
- Complete Model-Based Design workflow for multicore microcontroller
- Hardware component and device driver behavior simulation
 - Enhanced on-device profiling





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Learn More

- Recording webinars
 - Field Oriented Control Made Easy
 - Motor Control with TI Multicore MCUs Using Simulink
 - Implementing Motor and Power Electronics Control on an FPGA-Based SoC
- Shipping Demos
 - Partition Motor Control for Multiprocessor MCUs
 - Control PMSM Loaded with Dual Motor (Dyno)
 - Integrate MCU Scheduling and Peripherals in Motor Control Application



Field-Oriented Control on Dual CPU Processor



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Thank you



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