Sviluppo di un sistema di gestione delle batterie con Simulink

Maurizio Dalbard Aldo Caraceto











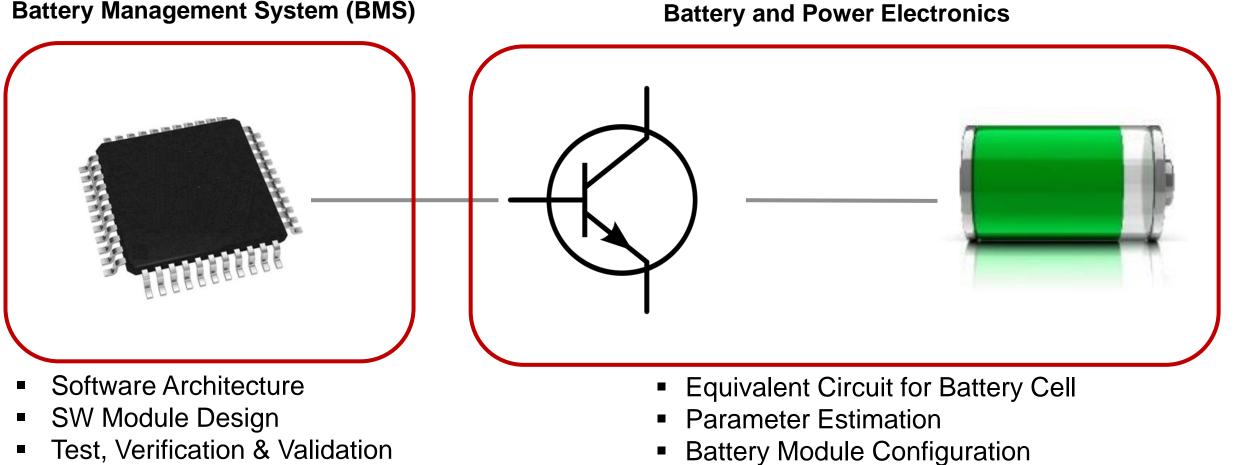








#### **Battery System**

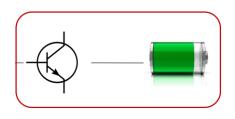


Charging & Balancing

- Test, Verification & Validation
- **BMS Integration Testing**



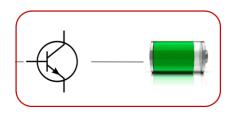
#### **Battery and Power Electronics**



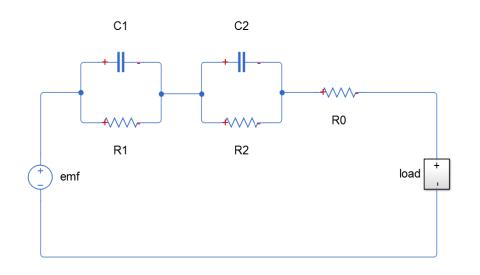
- Equivalent Circuit for Battery Cell
- Parameter Estimation
- Battery Module Configuration
- Charging & Balancing



#### **Battery and Power Electronics**

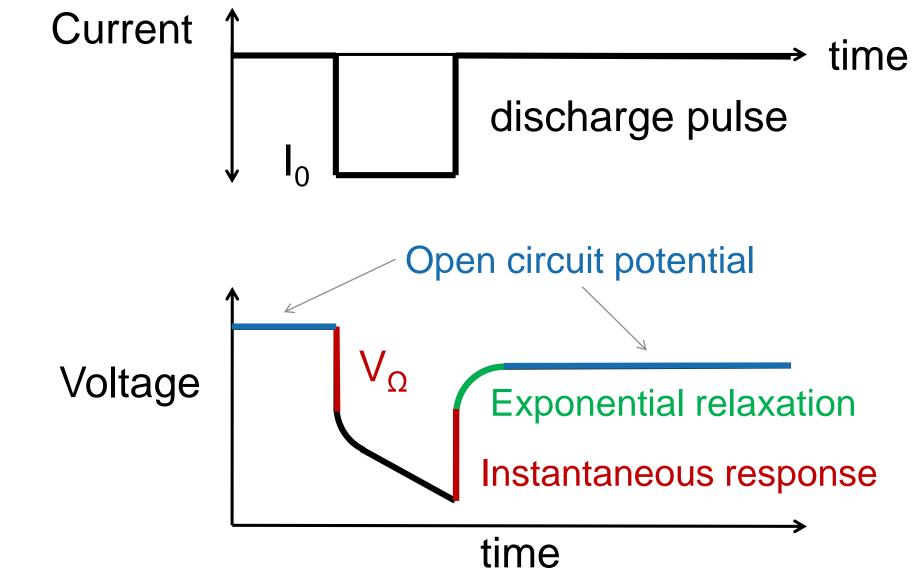


- Equivalent Circuit for Battery Cell
- Parameter Estimation
- Battery Module Configuration
- Charging & Balancing



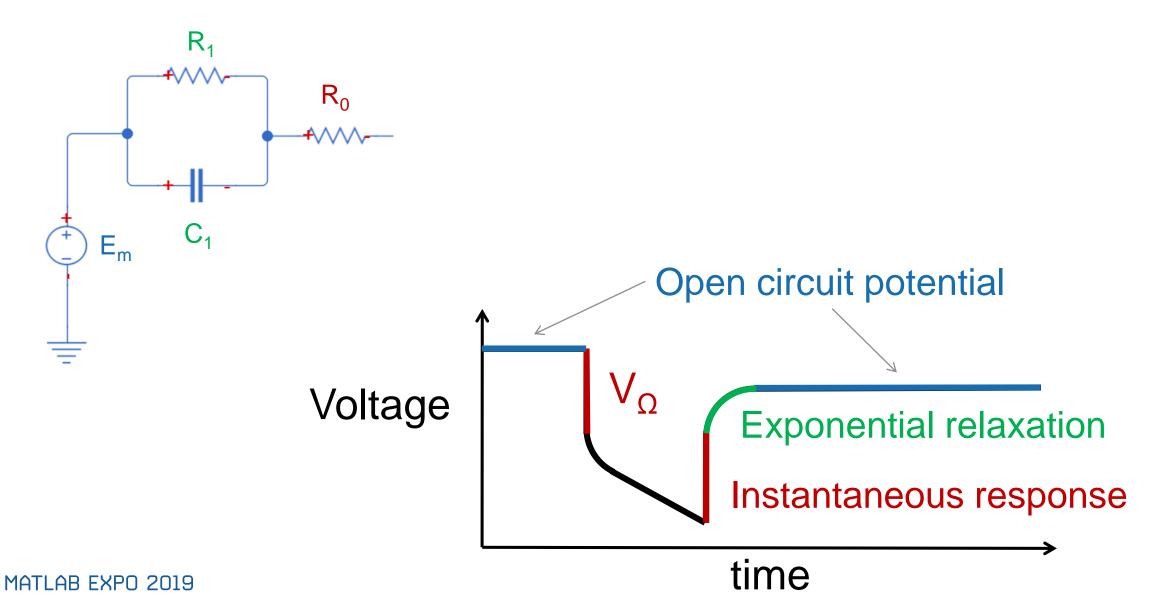


#### **Pulse Discharge**



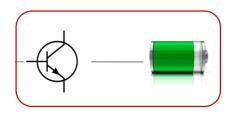


#### **Equivalent Circuit**

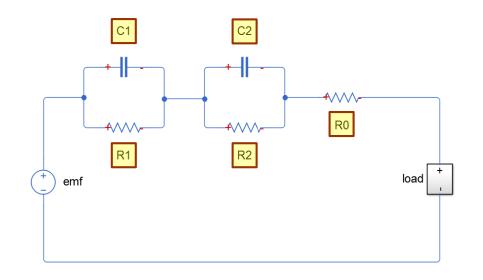




#### **Battery and Power Electronics**

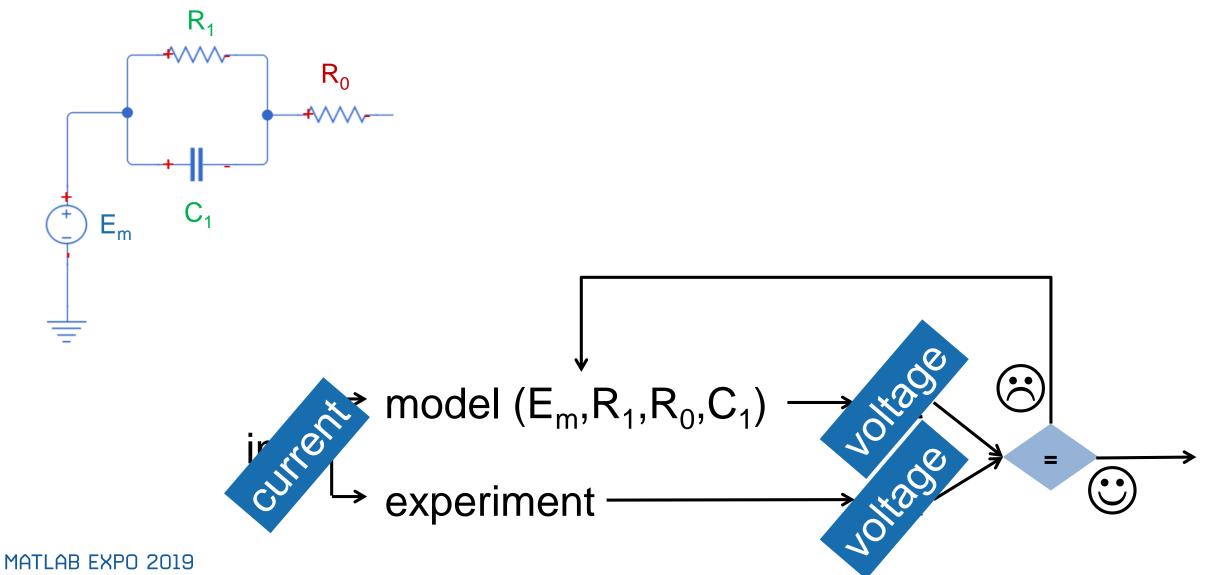


- Equivalent Circuit for Battery Cell
- Parameter Estimation
- Battery Module Configuration
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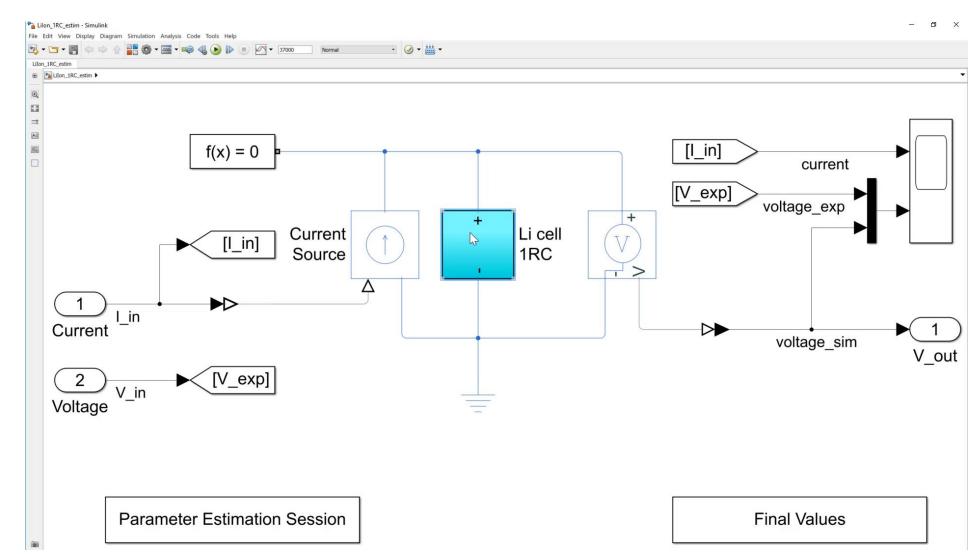


#### **Parameter Estimation**



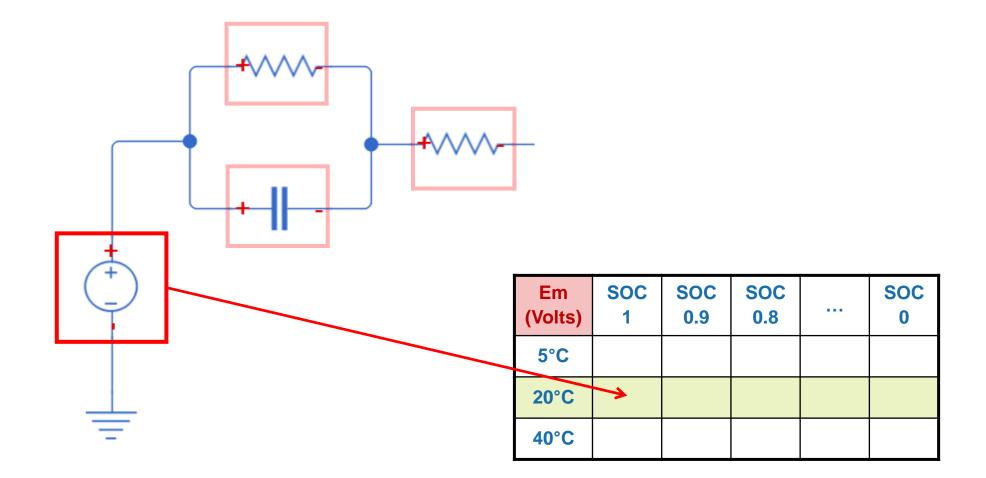


#### **Estimate Parameters**



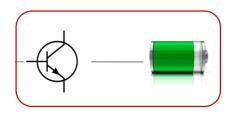


#### **Look-up Tables**





#### **Battery and Power Electronics**

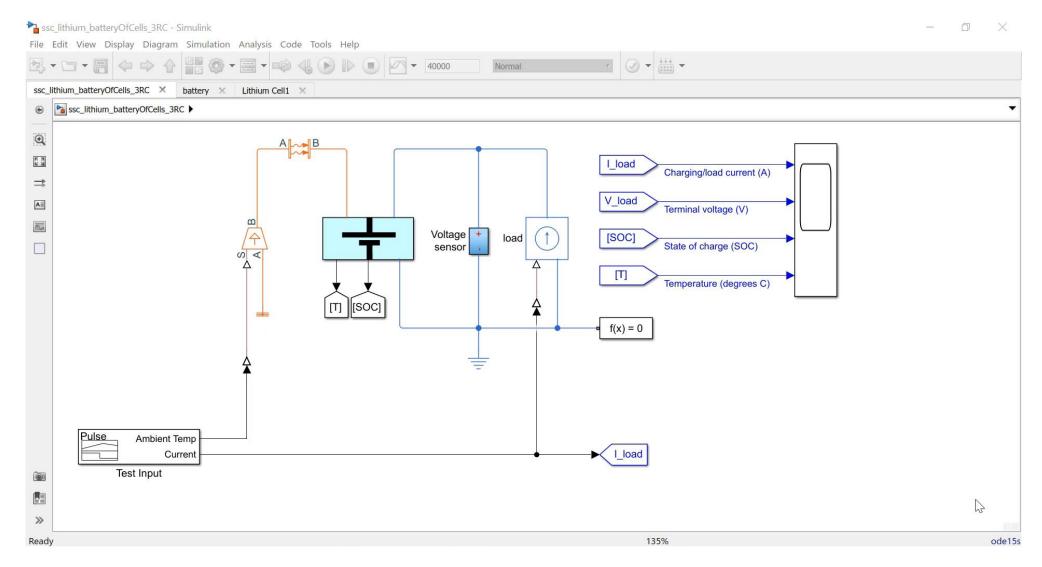


- Equivalent Circuit for Battery Cell
- Parameter Estimation
- Battery Module Configuration
- Charging & Balancing





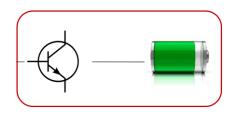
#### **Battery Pack**



MATLAL

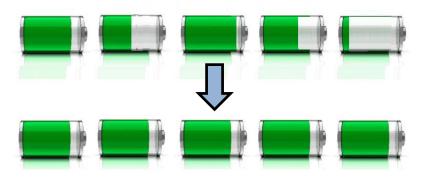


#### **Battery and Power Electronics**



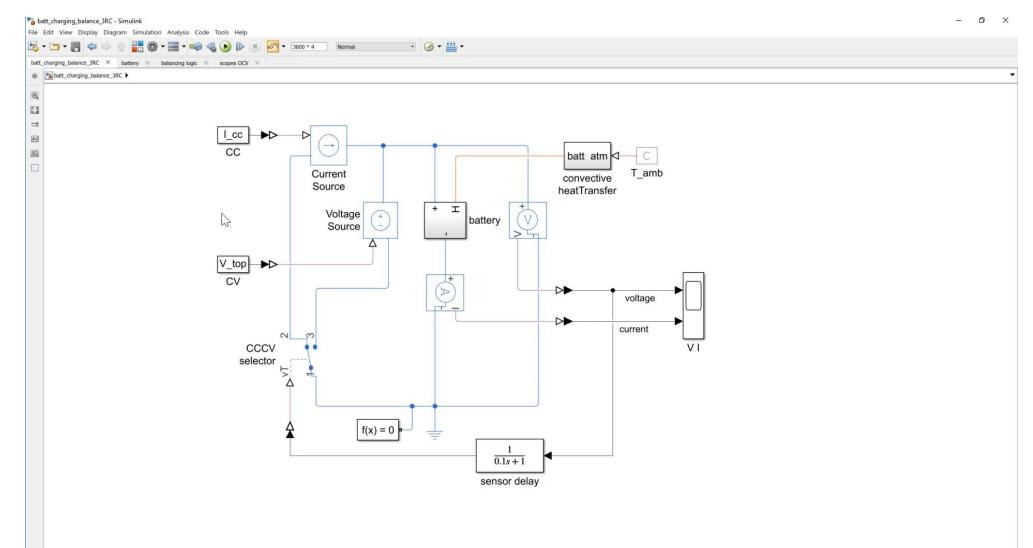
- Equivalent Circuit for Battery Cell
- Parameter Estimation
- Battery Pack Configurations
- Charging & Balancing





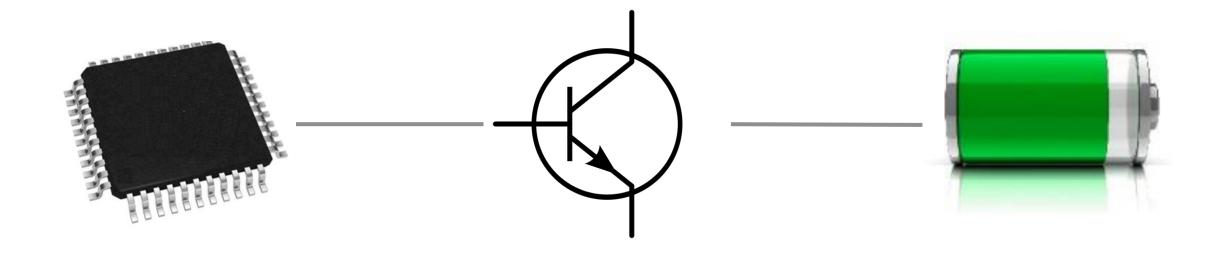


#### **Charging & Balancing**



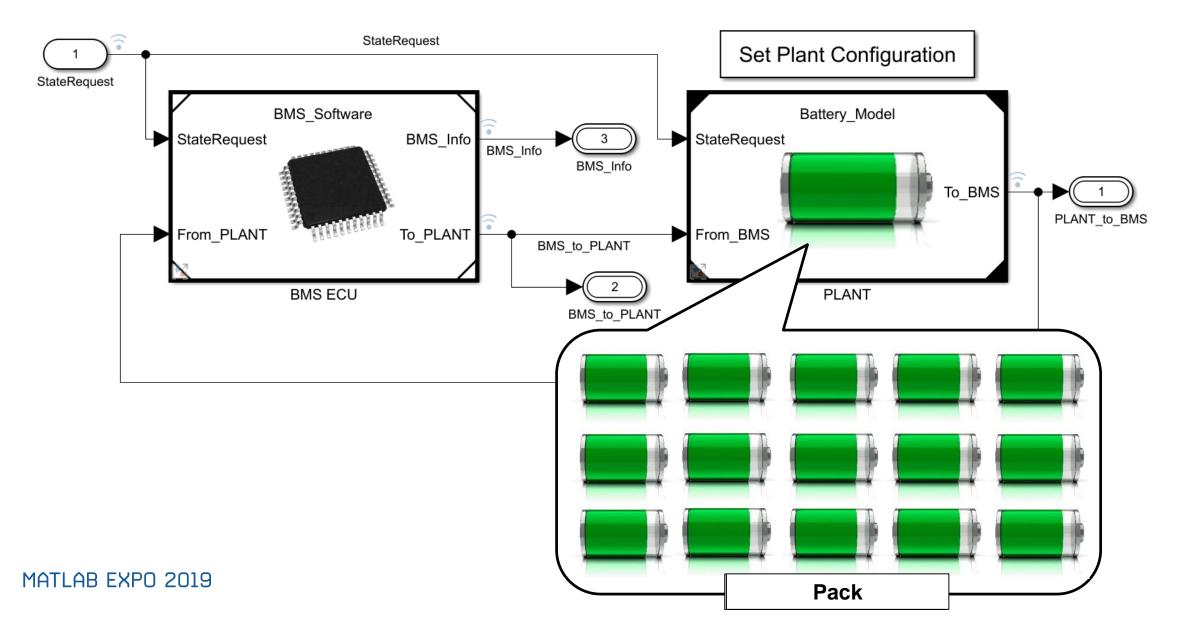


#### **Battery Management System**



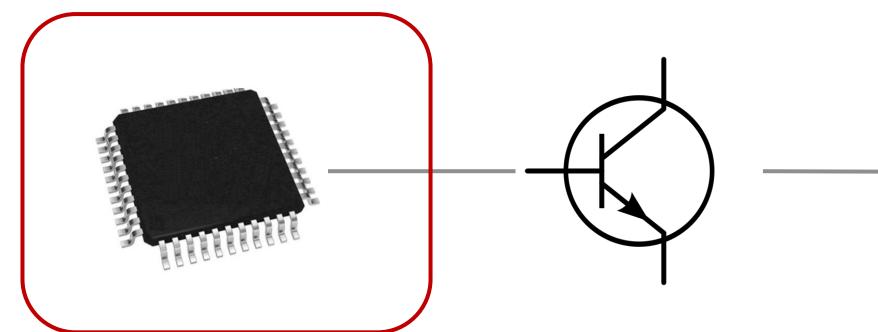


#### **Battery Management System – Professional Simulink Model**





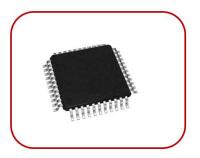
#### **Battery Management System**



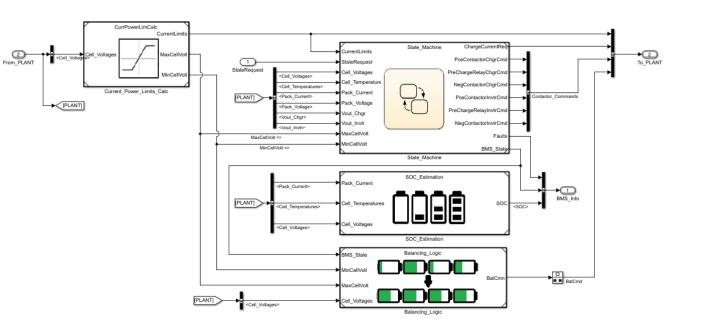


- Software Architecture
- SW Module Design
- Test, Verification & Validation
- BMS Integration Testing



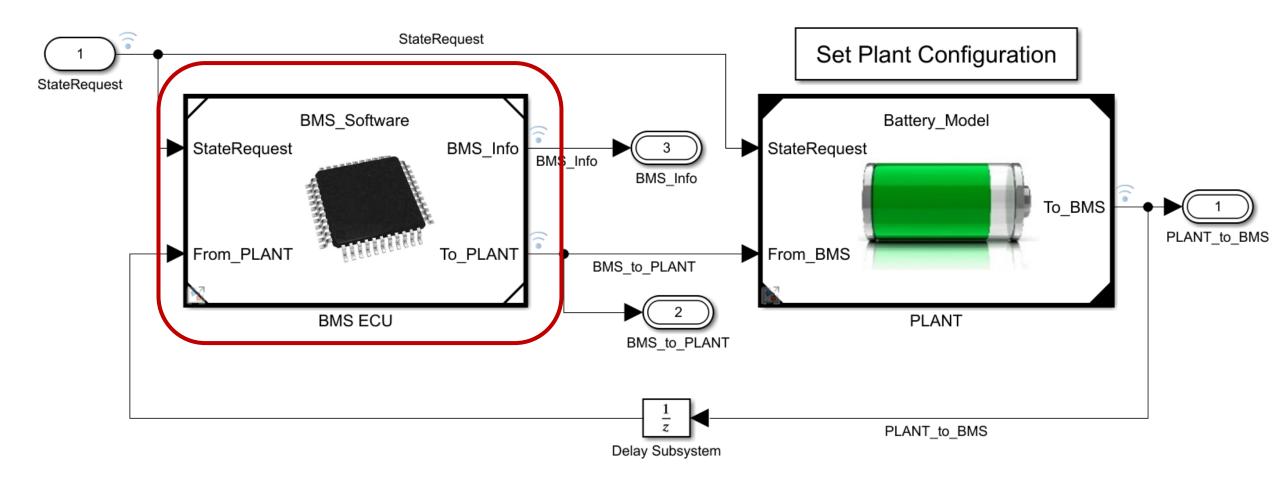


- Software Architecture
- SW Module Design
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- BMS Integration Testing

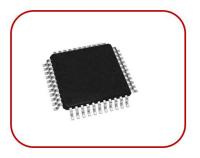




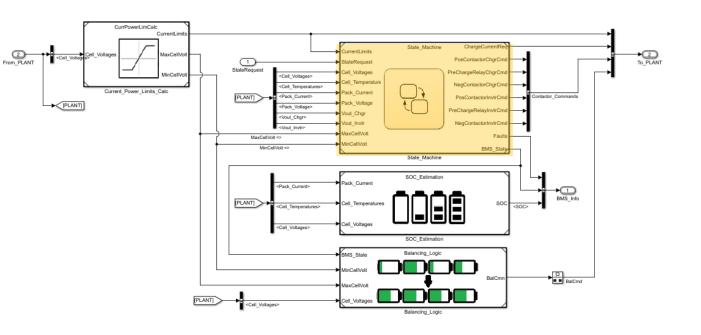
### **Battery Management System – Professional Simulink Model**





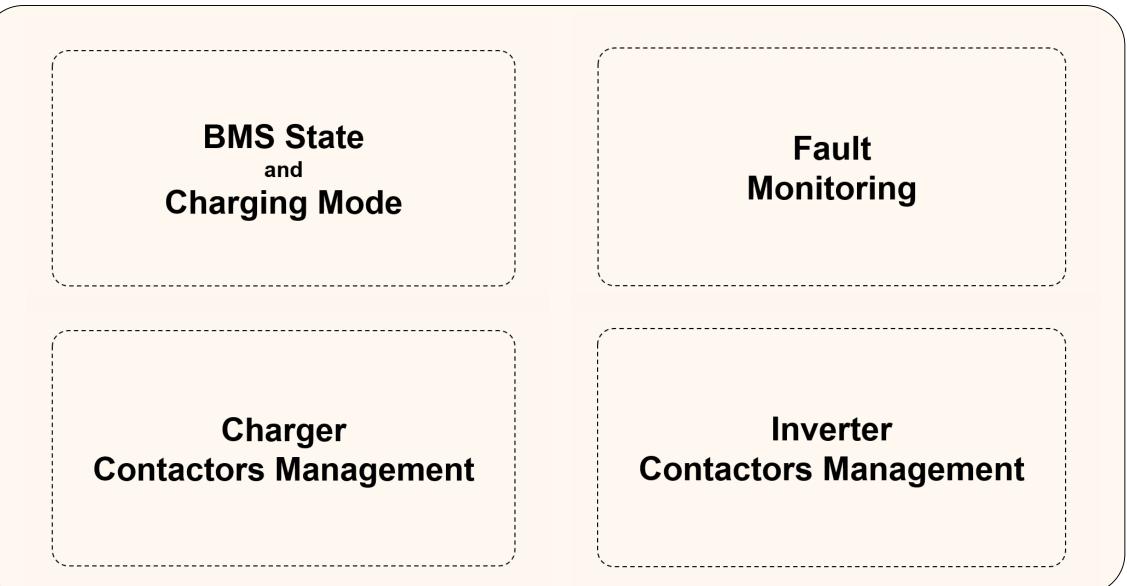


- Software Architecture
- SW Module Design
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- BMS Integration Testing



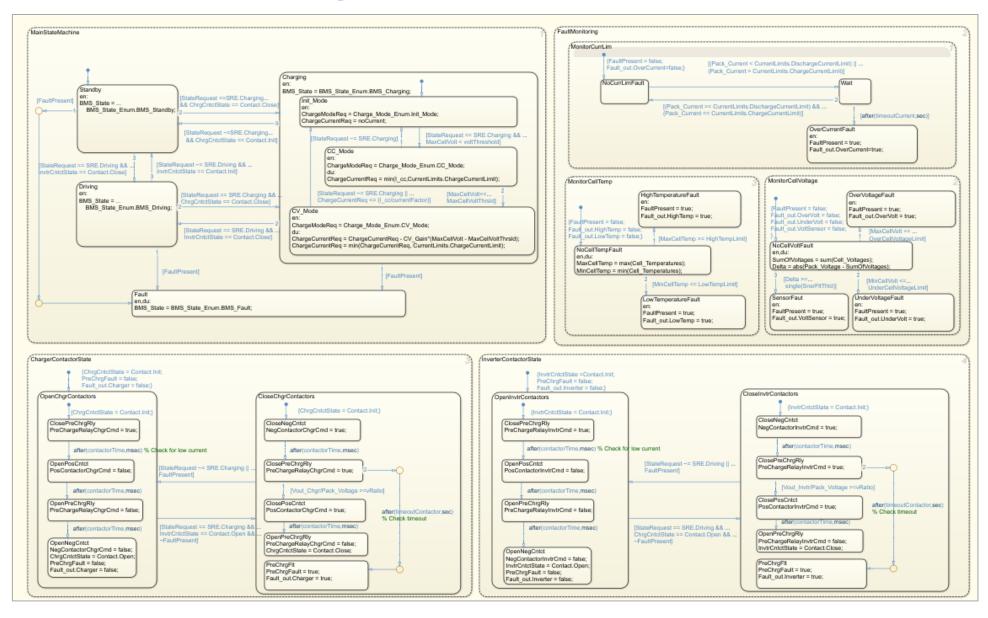


#### **State Machine Logic**

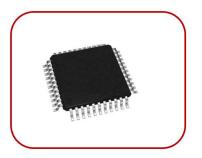




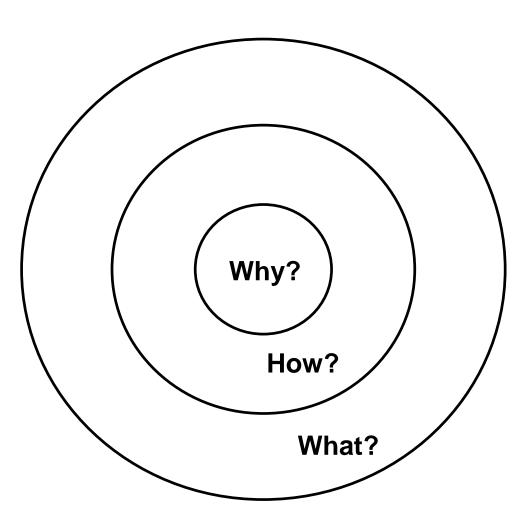
#### **State Machine Logic in Stateflow**



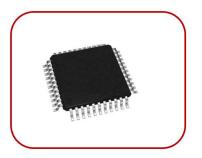




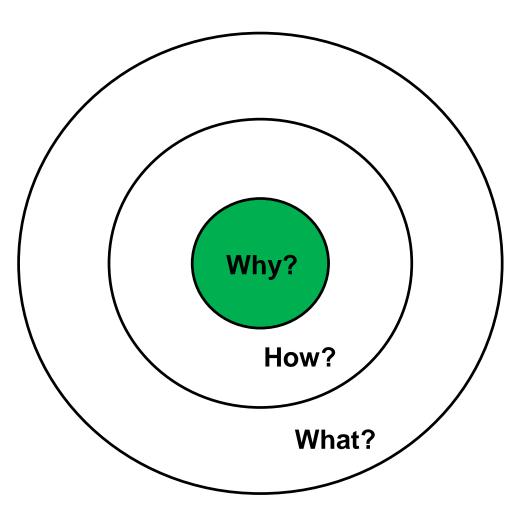
- Software Architecture
- SW Module Design
- Test, Verification & Validation
- BMS Integration Testing

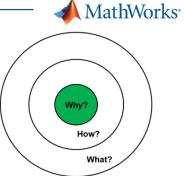


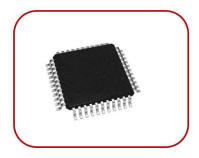




- Software Architecture
- SW Module Design
- Test, Verification & Validation
- BMS Testing







- Software Architecture
- SW Module Design
- Test, Verification & Validation
- BMS Integration Testing





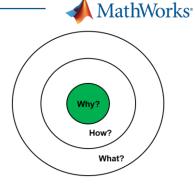


### Software Architecture

- SW Module Design
- Test, Verification & Validation
- BMS Integration Testing

### Battery Management System (BMS)

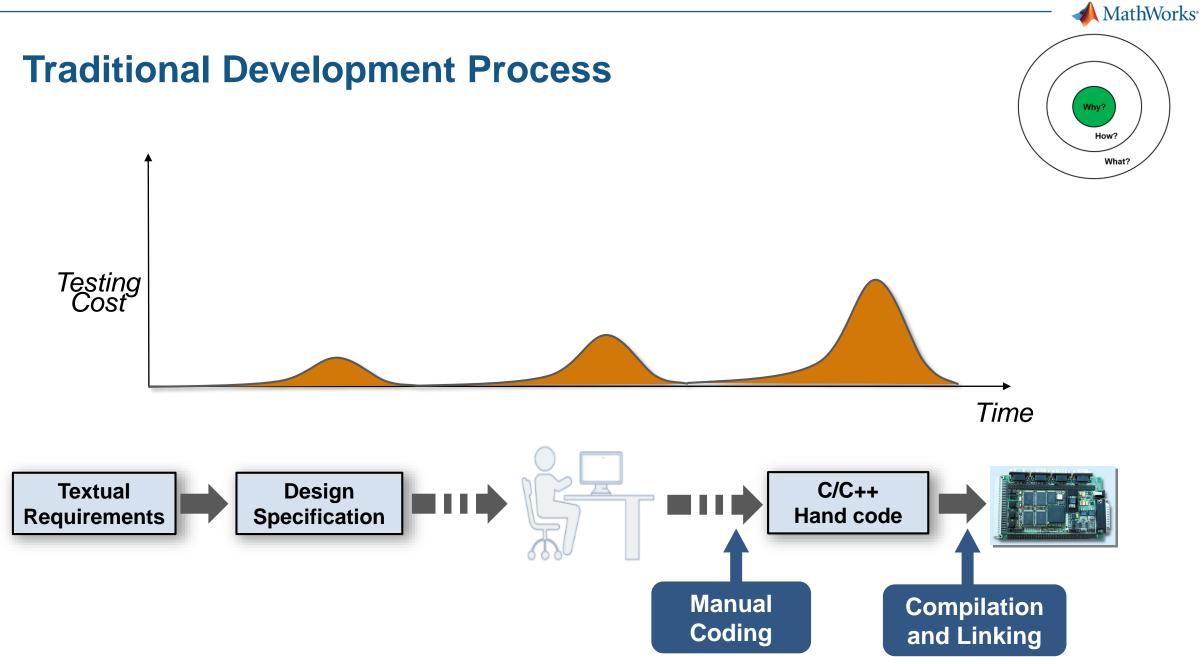




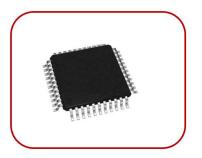
Safety Critical System

#### **Functional Safety Certification**

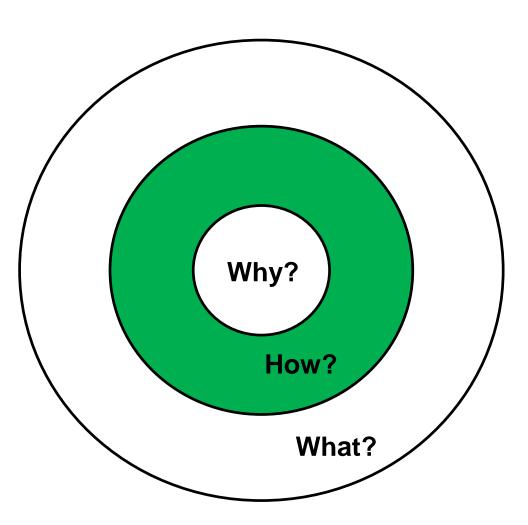


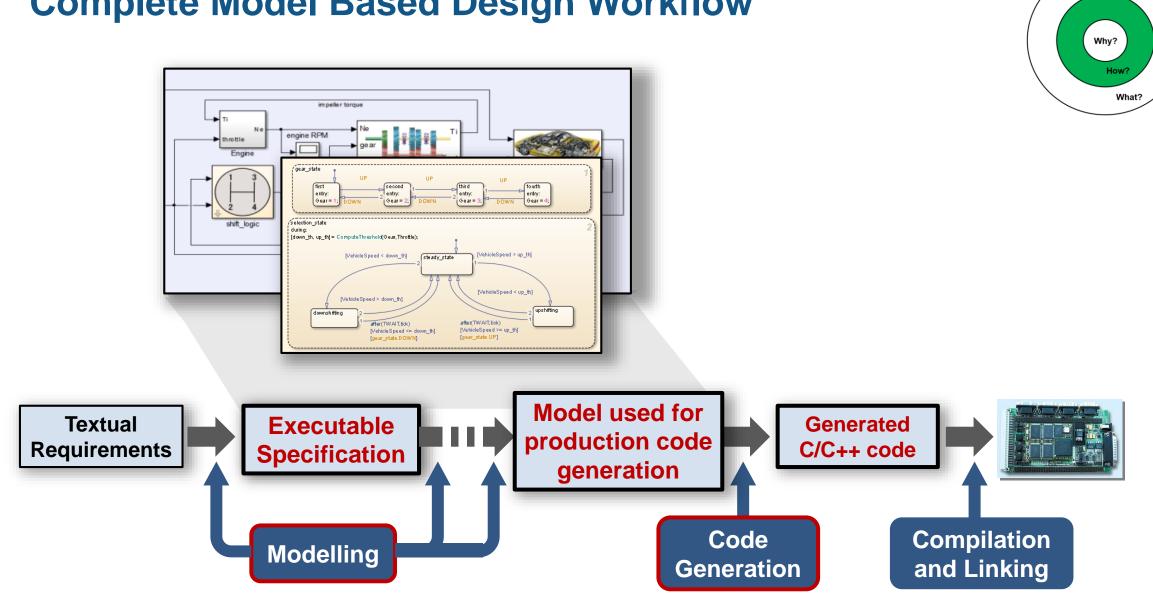






- Software Architecture
- SW Module Design
- Test, Verification & Validation
- BMS Integration Testing

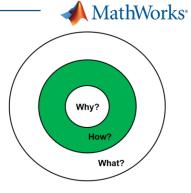


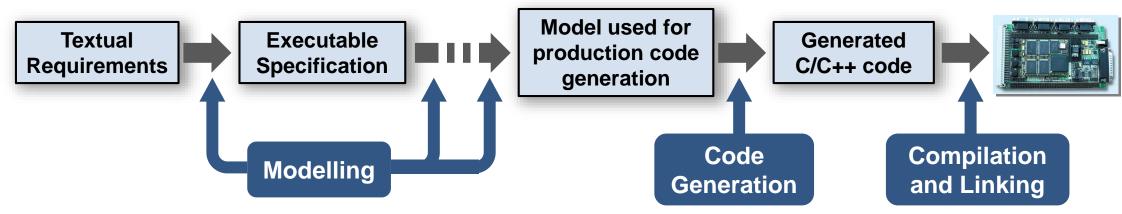


### **Complete Model Based Design Workflow**

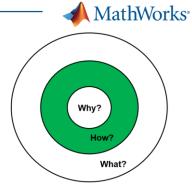
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### **Complete Model Based Design Workflow**

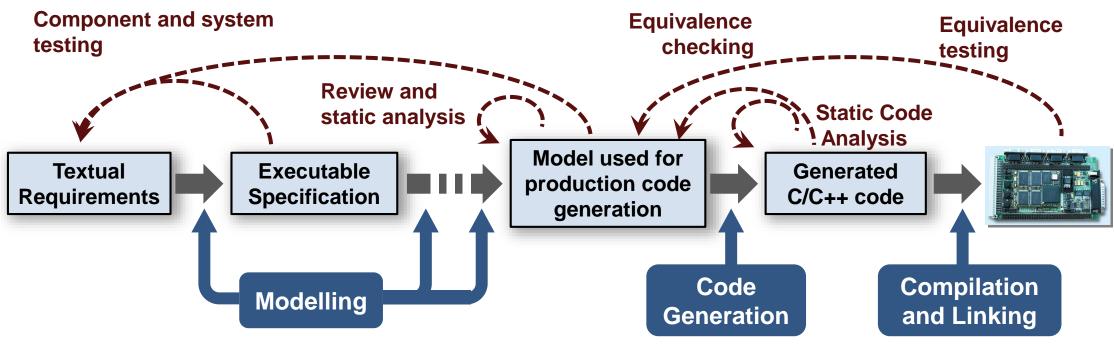


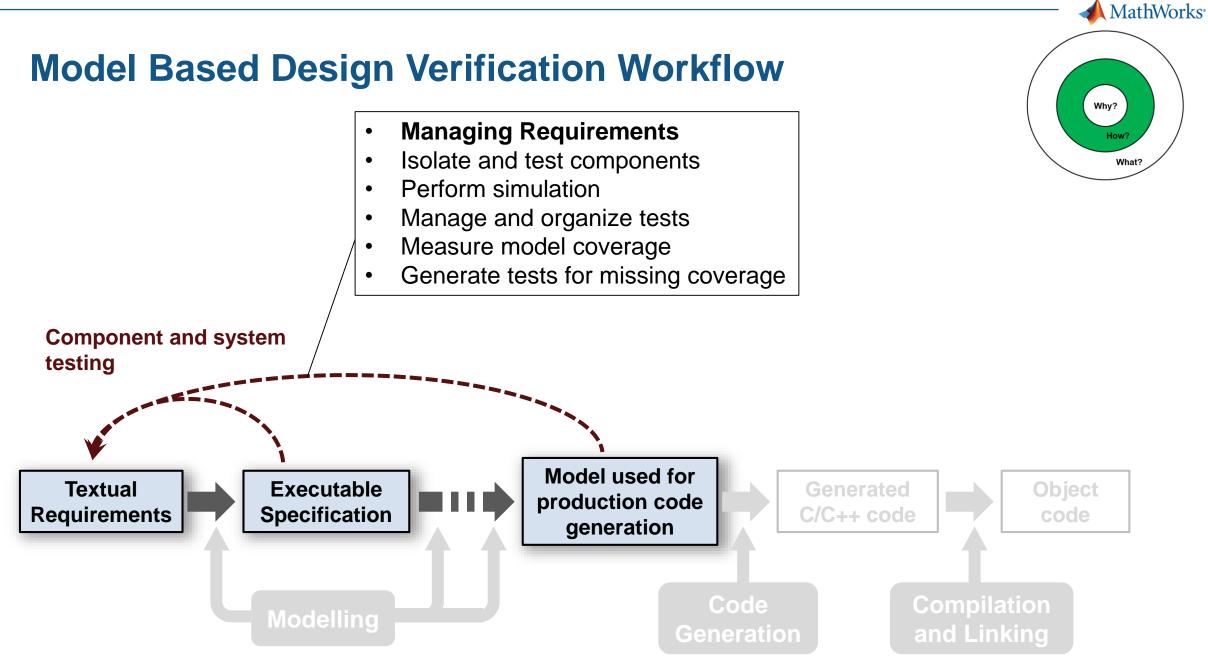


### **Complete Model Based Design Workflow**



#### get the complete confidence in your design







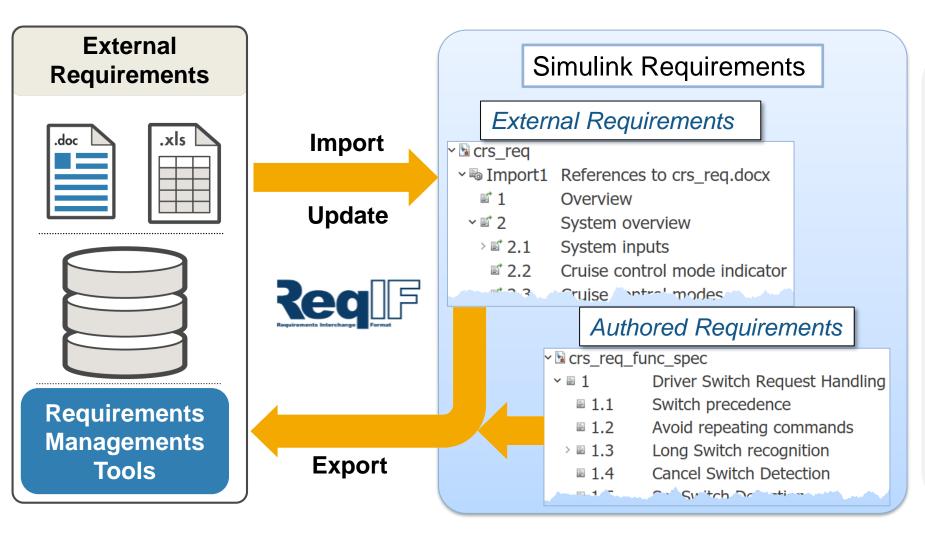
## Why do 71% of Embedded Projects Fail?

# **Poor Requirements Management**

Sources: Christopher Lindquist, Fixing the Requirements Mess, CIO Magazine, Nov 2005 MATLAB EXPO 2019

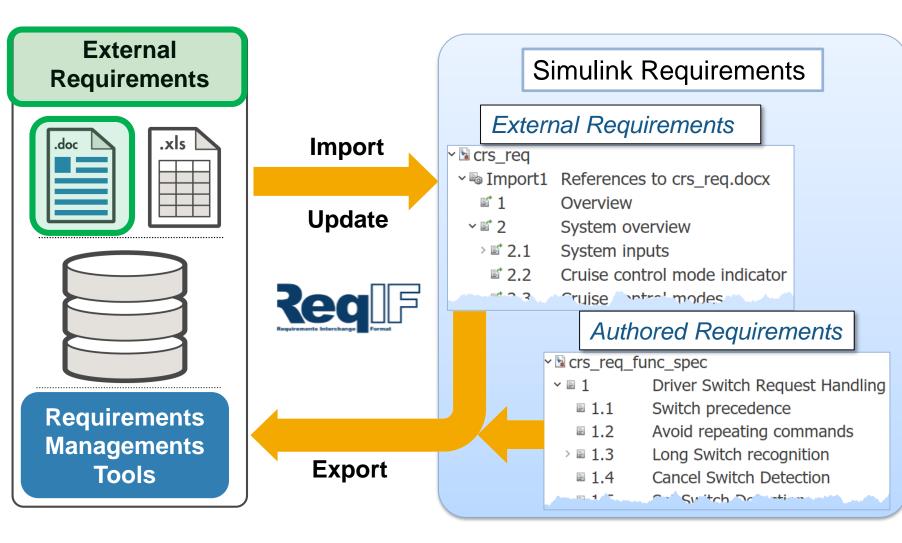


#### Integrate with requirements tools and author requirements



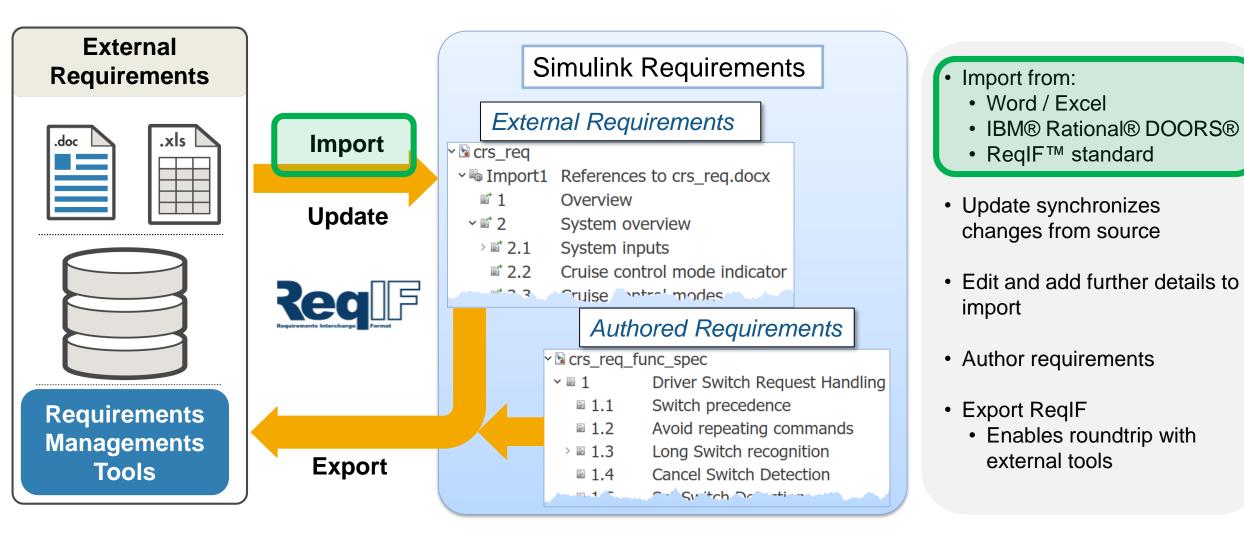
- Import from:
  - Word / Excel
  - IBM® Rational® DOORS®
  - ReqIF<sup>™</sup> standard
- Update synchronizes changes from source
- Edit and add further details to import
- Author requirements
- Export ReqIF
  - Enables roundtrip with external tools



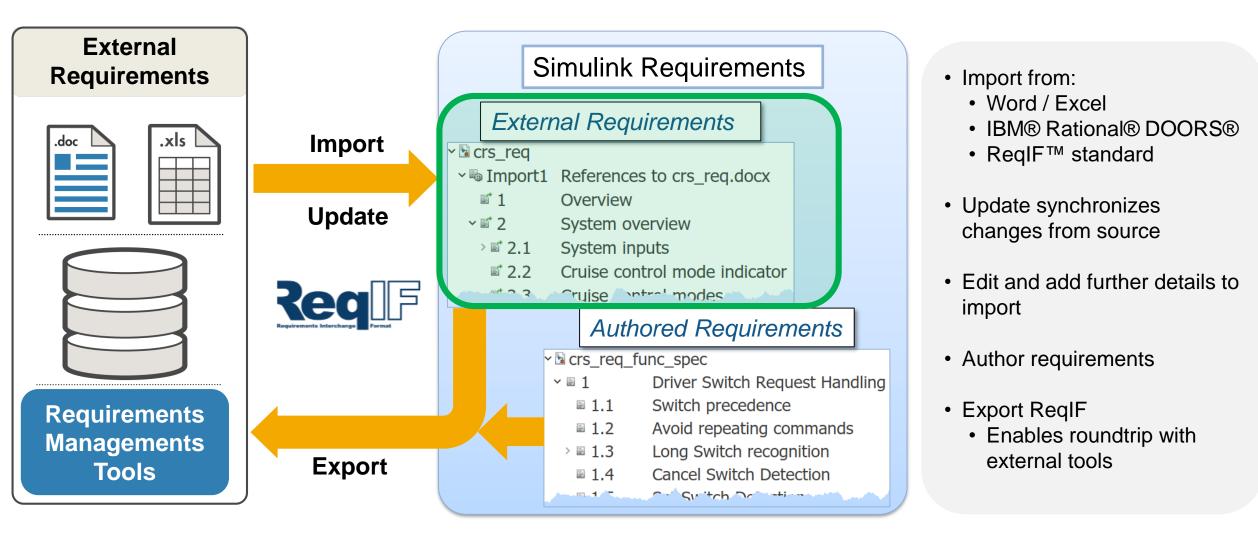


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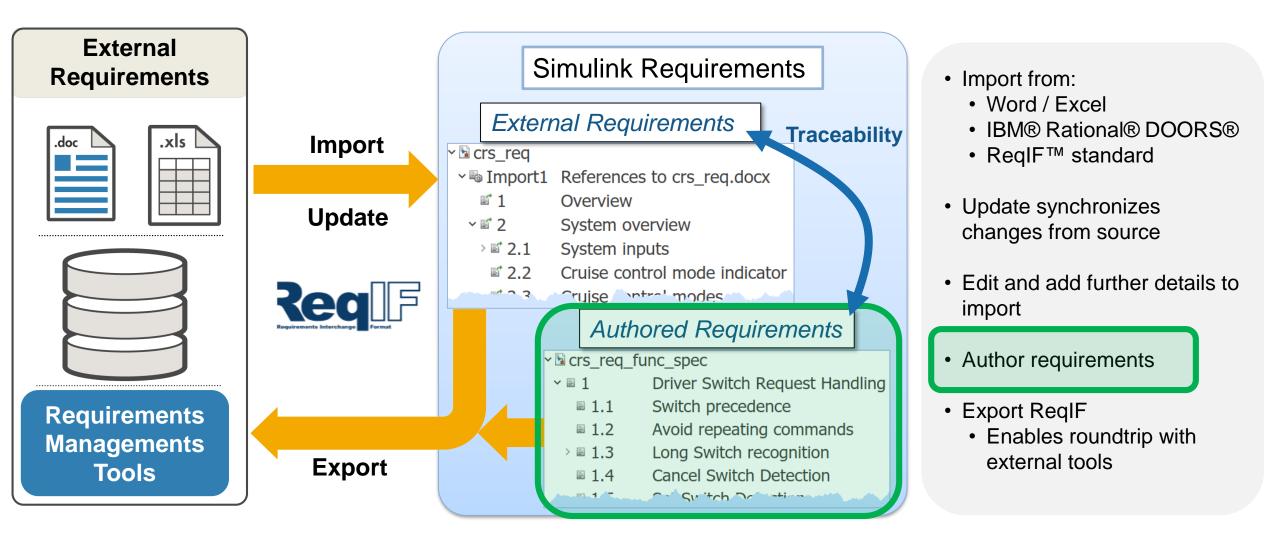




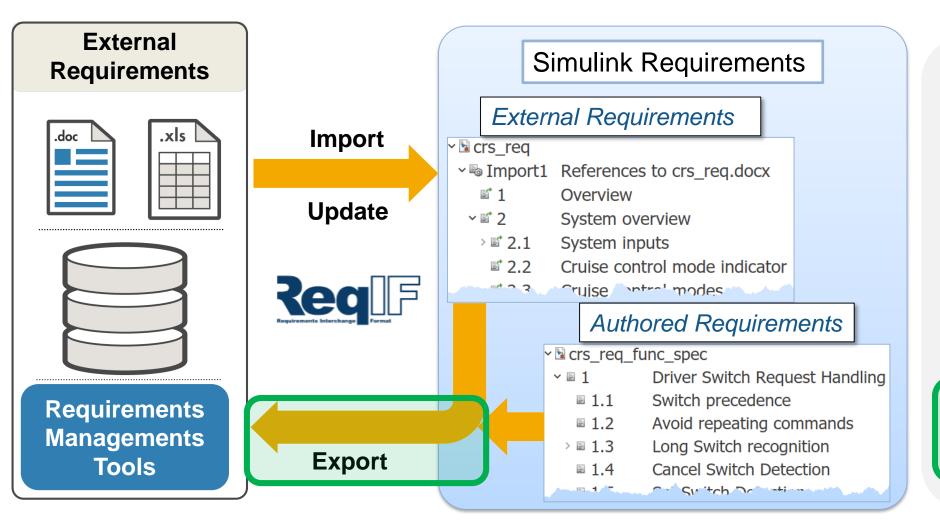








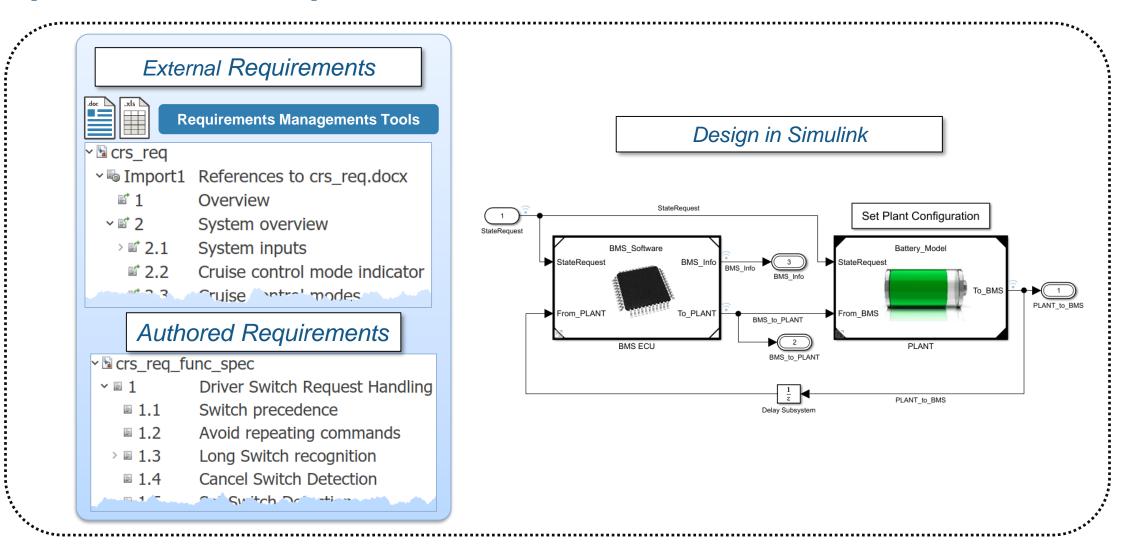




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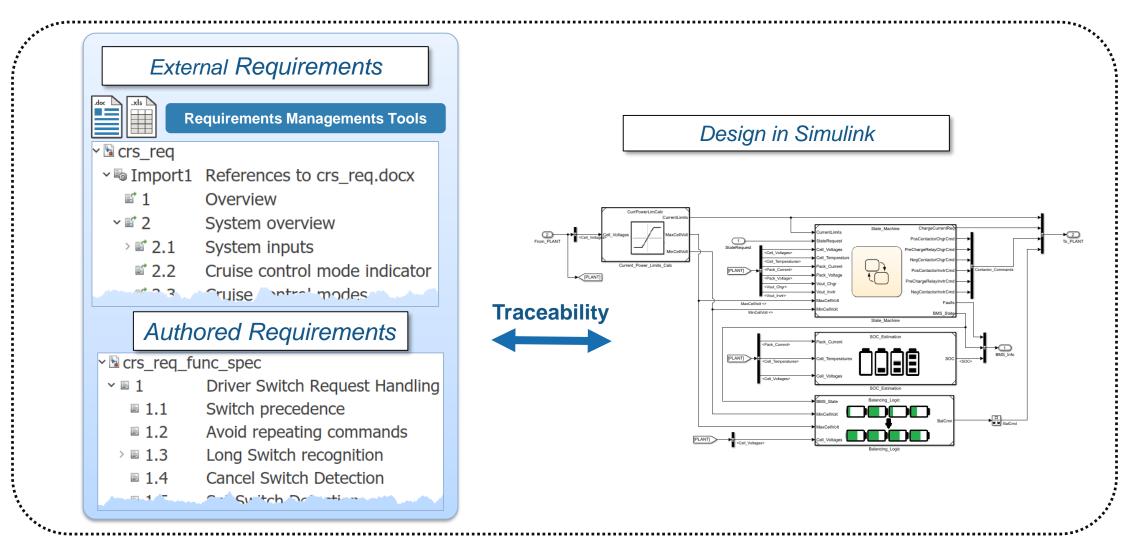


## **Requirements Perspective**





## **Traceability: Requirements - Design**

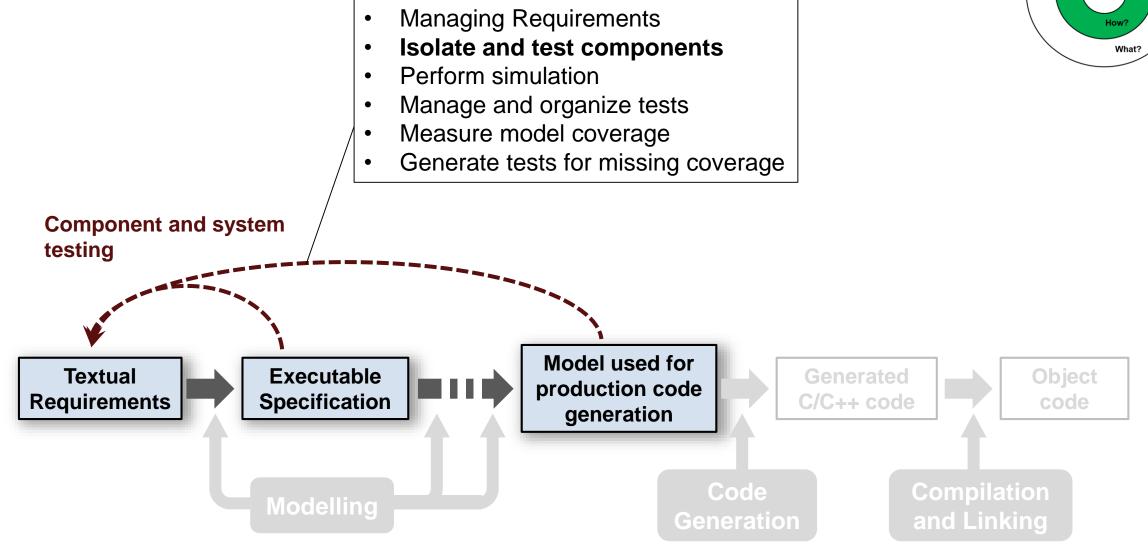




## **Requirements Implementation Status**

| Requirements - crs_controller |     |                                |                       |
|-------------------------------|-----|--------------------------------|-----------------------|
| ew: Requirements 🔻            |     | 1 e e 🔏 🔒 💼 🔍 (                | Ĉ                     |
| dex                           | ID  | Summary                        | Implemented           |
| crs_req_func_spec*            | —   | -                              |                       |
| > 1                           | #1  | Driver Switch Request Handling |                       |
| ✓                             | #19 | Cruise Control Mode            |                       |
| > 🖹 2.1                       | #20 | Disable Cruise Control system  |                       |
| > 🖹 2.2                       | #24 | Operation mode determination   |                       |
| ady                           |     |                                | > stic                |
| luy                           | _   |                                | Suc                   |
|                               |     |                                | Implementation Status |
|                               |     |                                | Implemented           |
|                               |     |                                | Justified             |
|                               |     |                                | Missing               |

# Model Based Design Verification Workflow

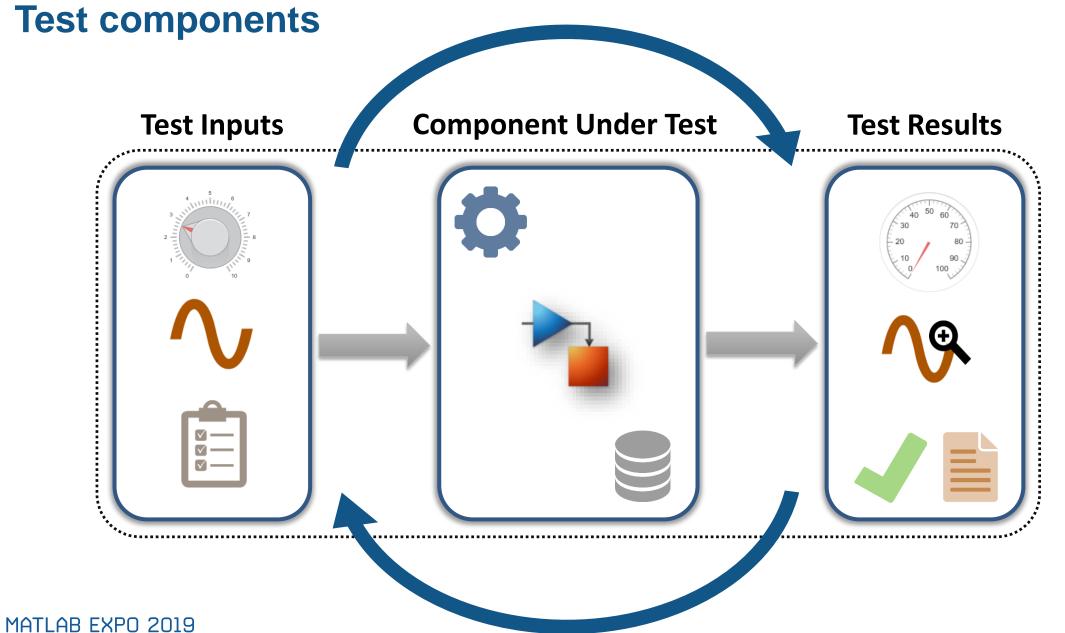


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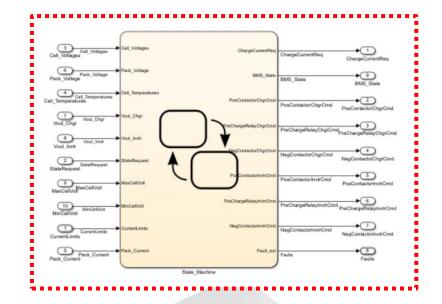
Why?

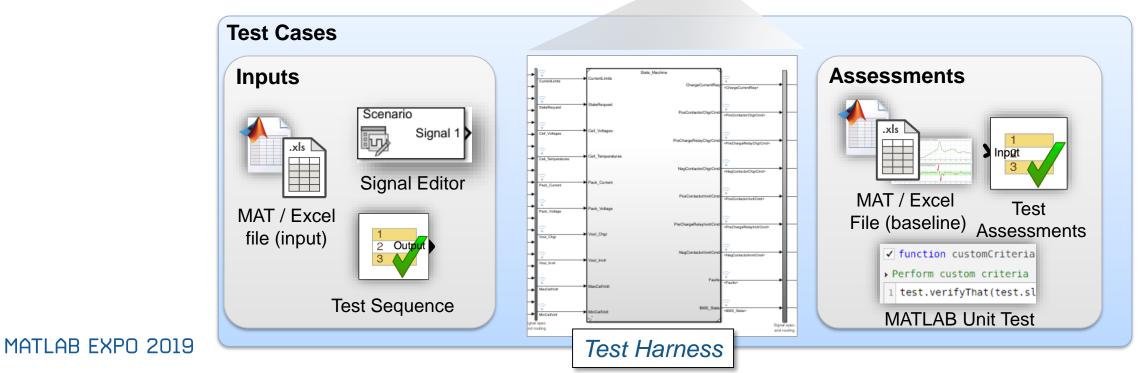
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## **Create Test Harnesses**

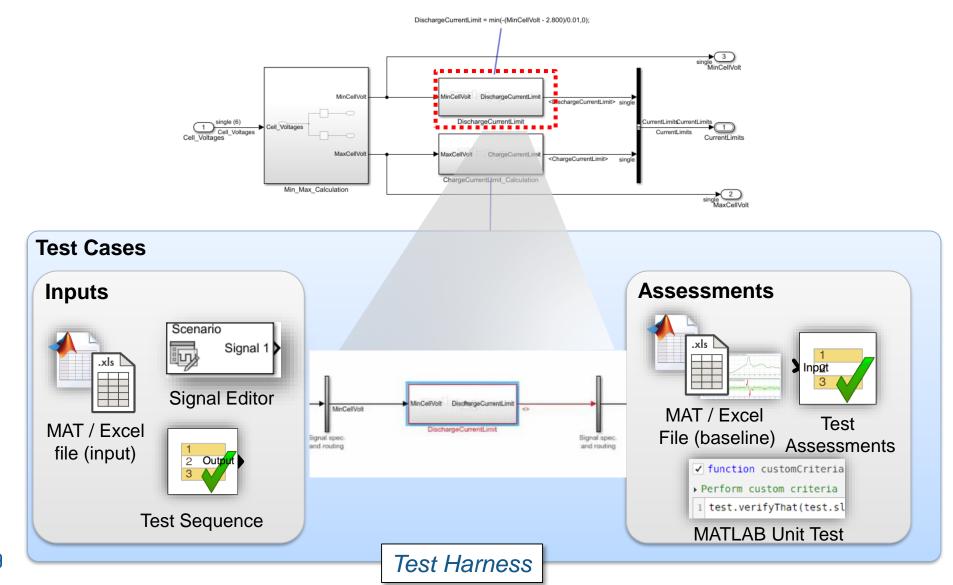


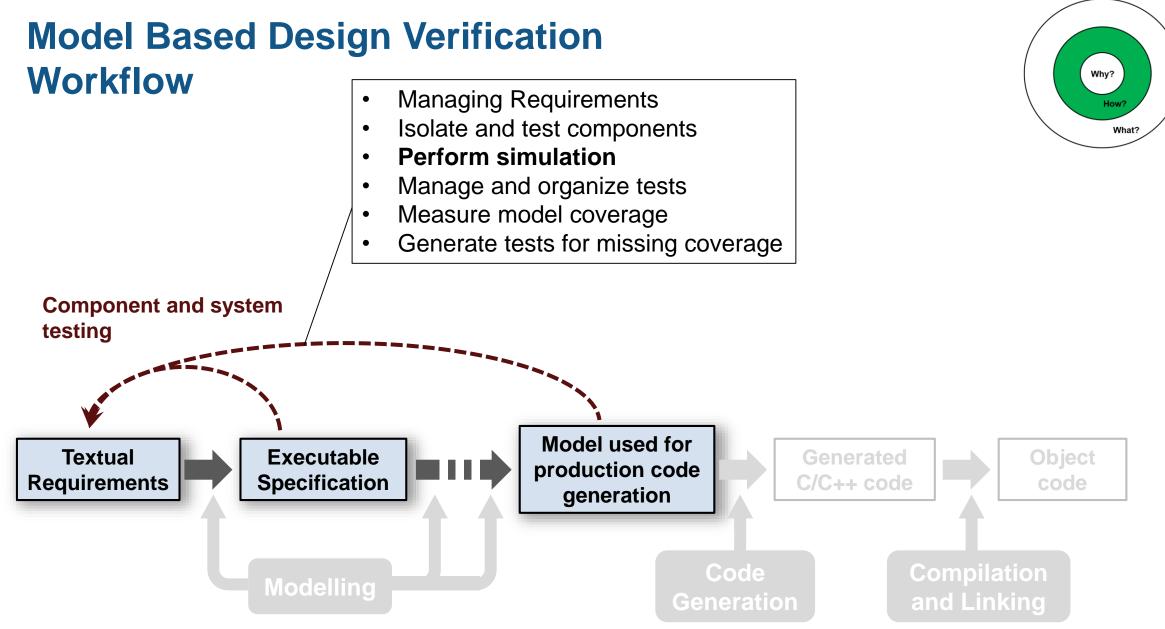


**47** 



## **Create Test Harnesses on Subsystems**



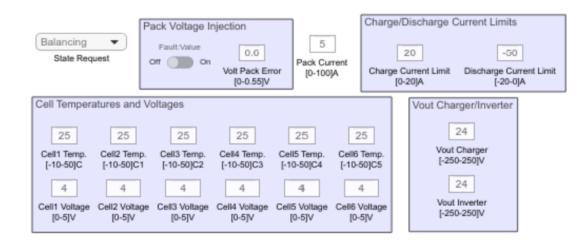


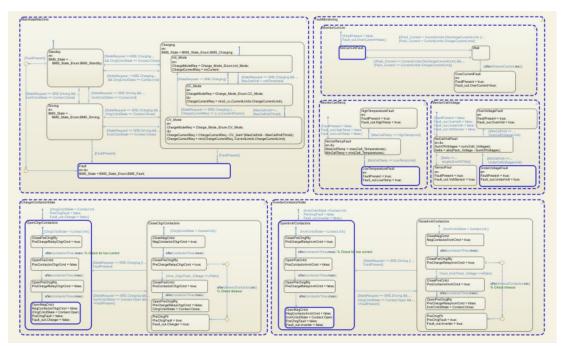
### MATLAB EXPO 2019

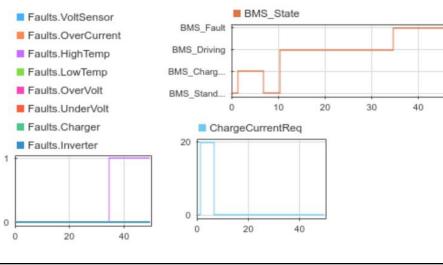
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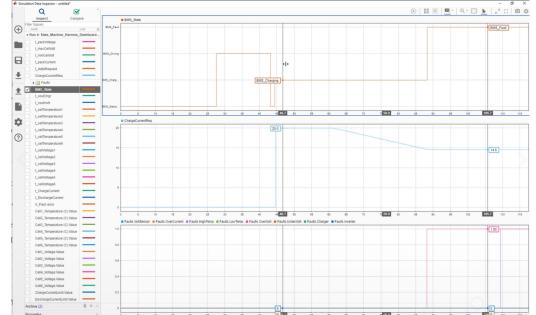


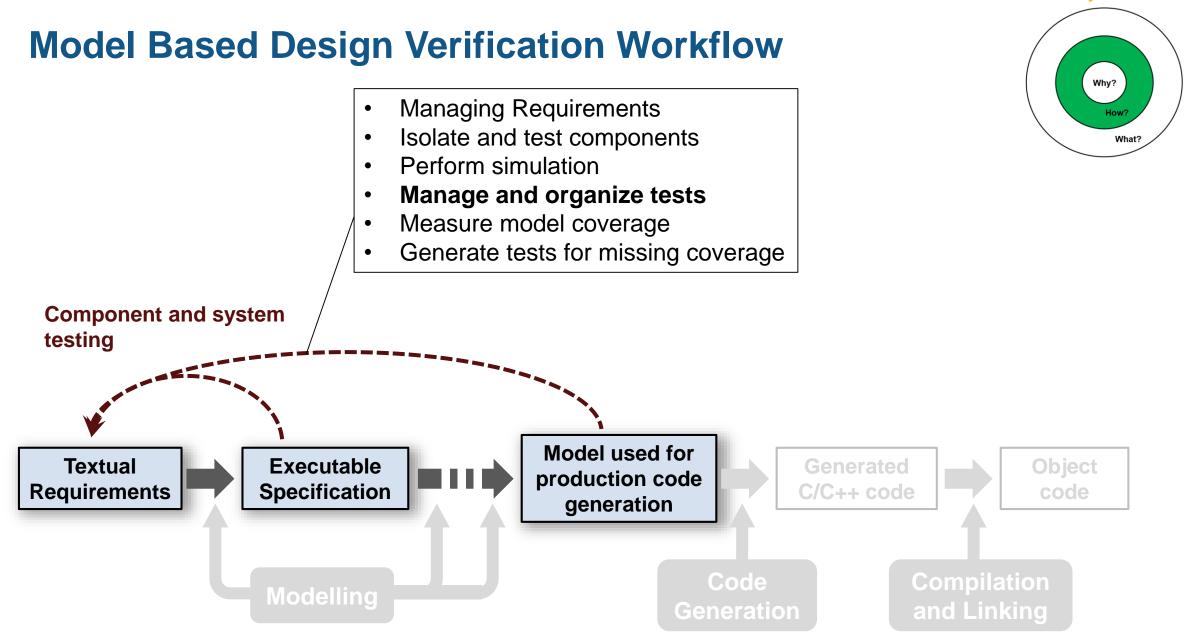
## **Test Ad-hoc with Dashboards**









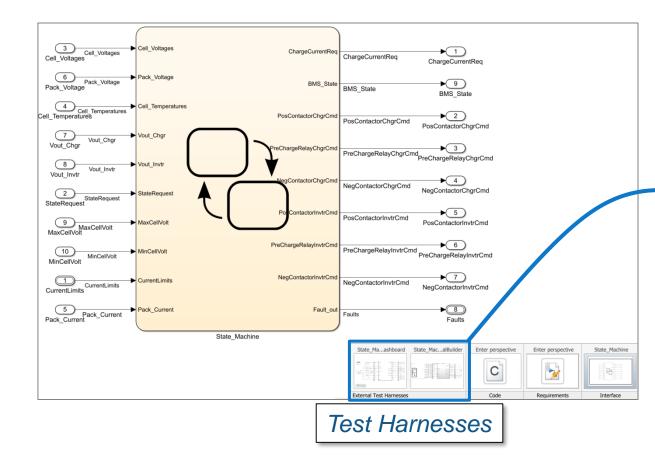


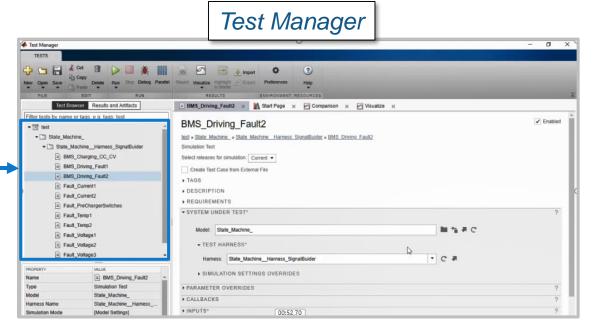
### MATLAB EXPO 2019

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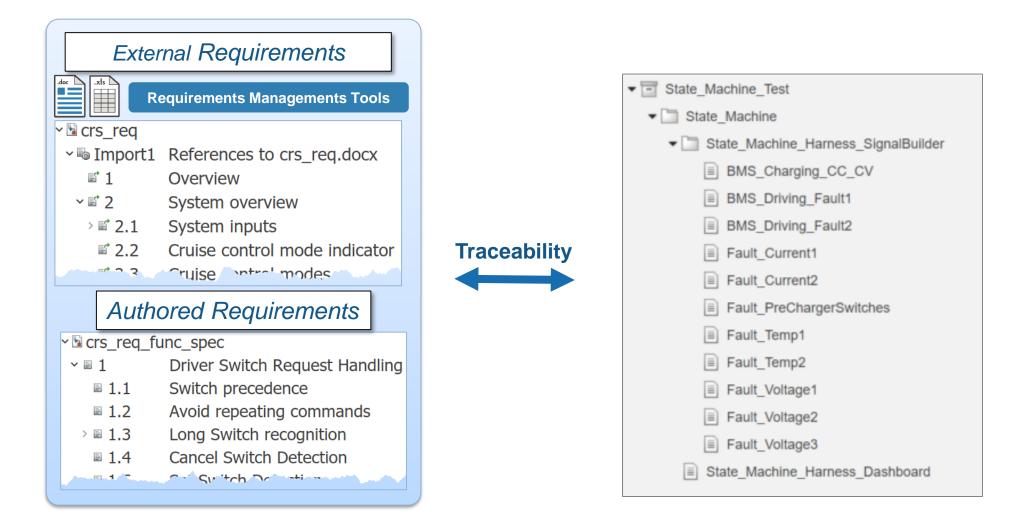
## **Test Harness Import in a Centralized Environment**





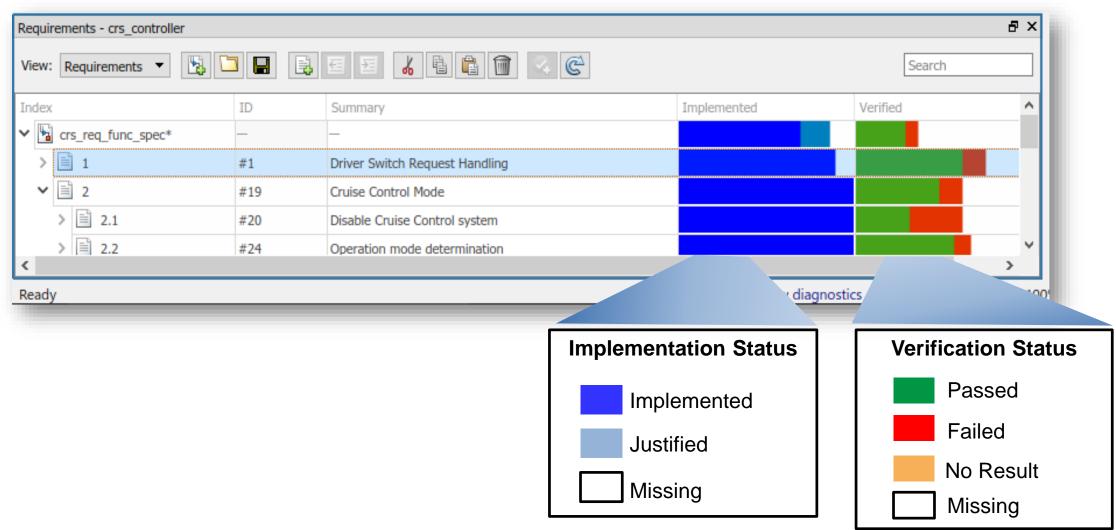


## **Traceability: Requirements - Tests**



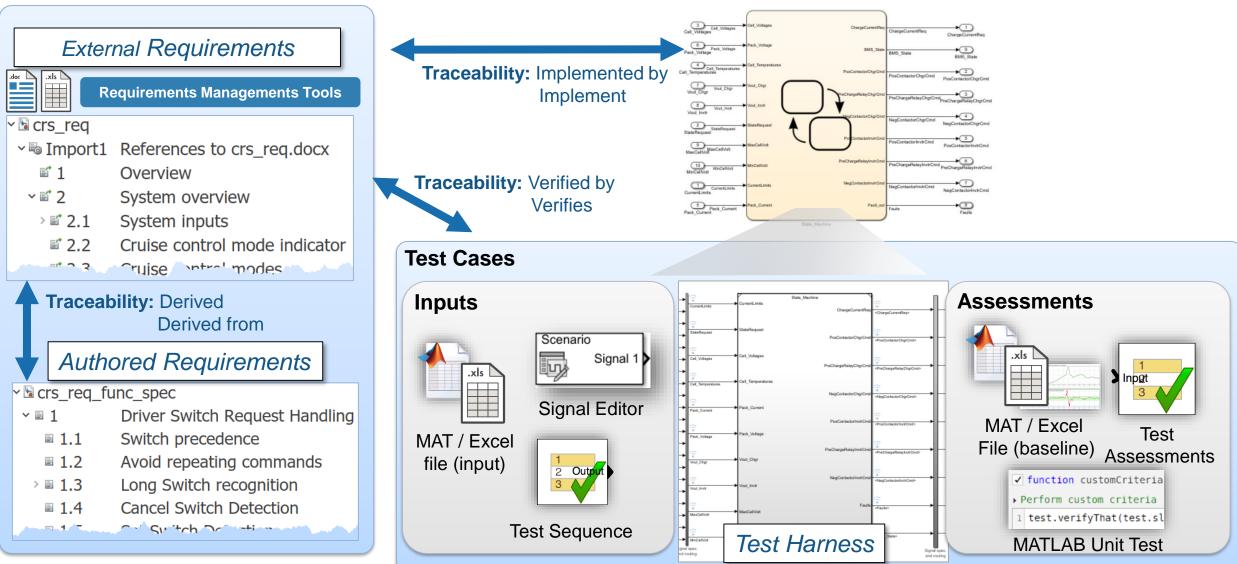


## **Requirements Verification Status**

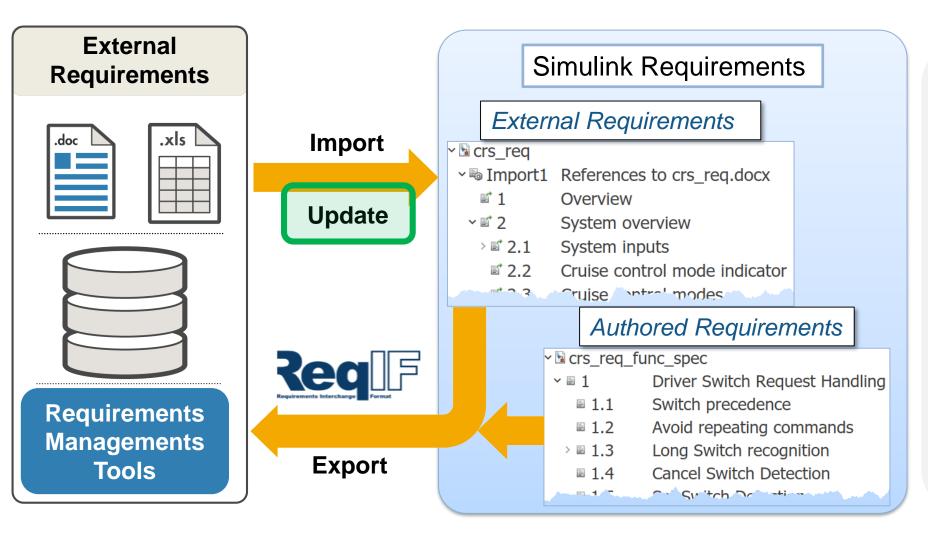




## **Requirements Verification with Simulink**







- Import from:
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  - IBM® Rational® DOORS®
  - ReqIF<sup>™</sup> standard
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- Export ReqIF
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## **Respond to Change – Impact Analysis**

### **Original Requirement**

### 3.2.4 BMS Current Limit Calculation: Charge Current Limit

Calculate the charge current limit following: ChargeCurrentLimit = min((4.500 - MaxCellVolt)/0.01,0);

### **Updated Requirement**

### 3.2.4 BMS Current Limit Calculation: Charge Current Limit

Calculate the charge current limit following: ChargeCurrentLimit = max((4.500 - MaxCellVolt)/0.01,0);



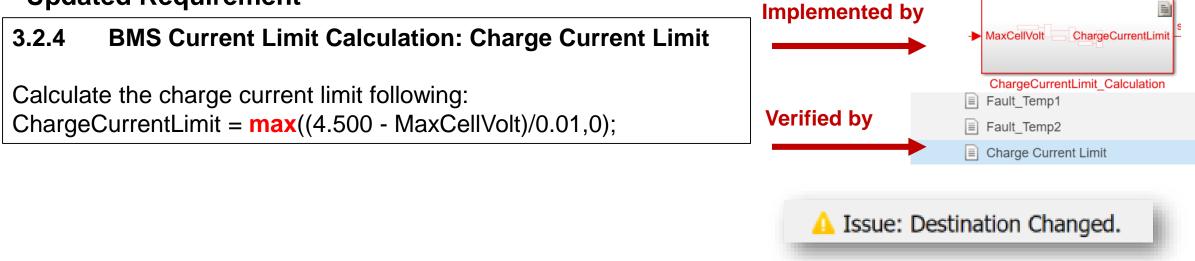
## **Respond to Change – Impact Analysis**

### **Original Requirement**

### 3.2.4 BMS Current Limit Calculation: Charge Current Limit

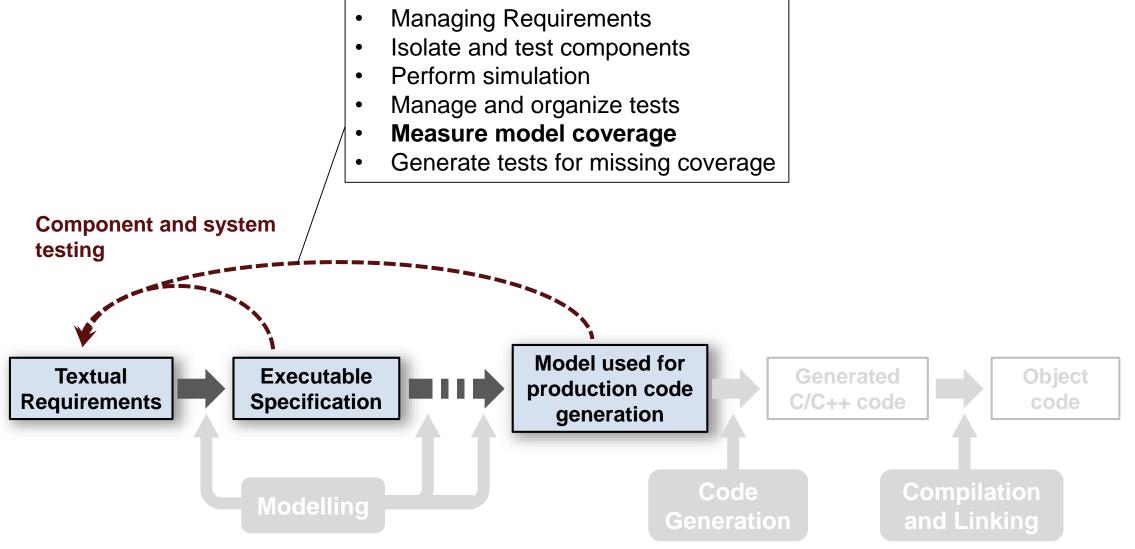
Calculate the charge current limit following: ChargeCurrentLimit = min((4.500 - MaxCellVolt)/0.01,0);

### **Updated Requirement**





## **Model Based Design Verification Workflow**





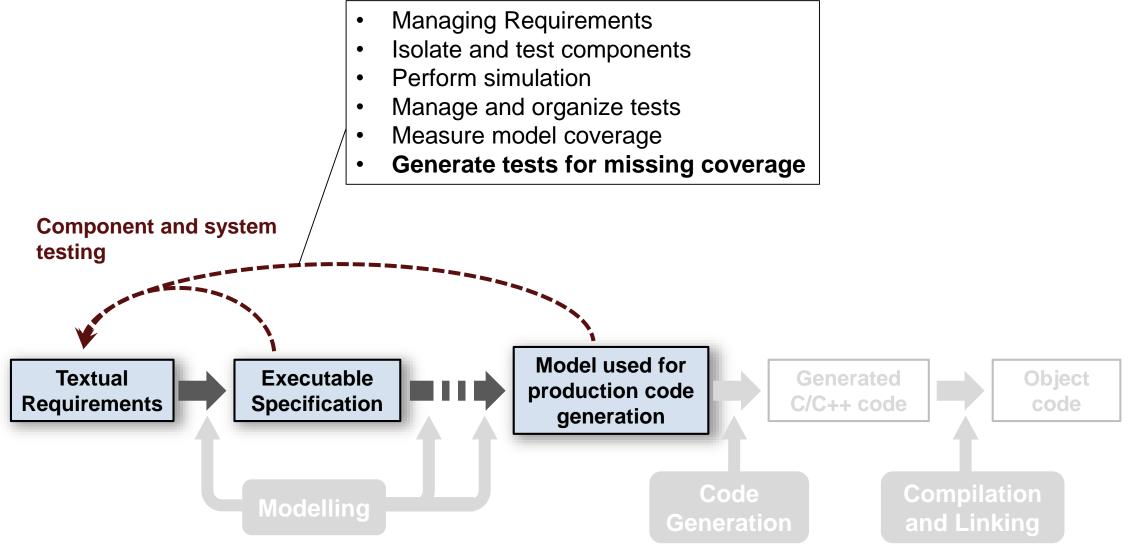
## Why we didn't achieve full model coverage?

## A. Missing tests

- B. Missing requirements
- c. Design errors

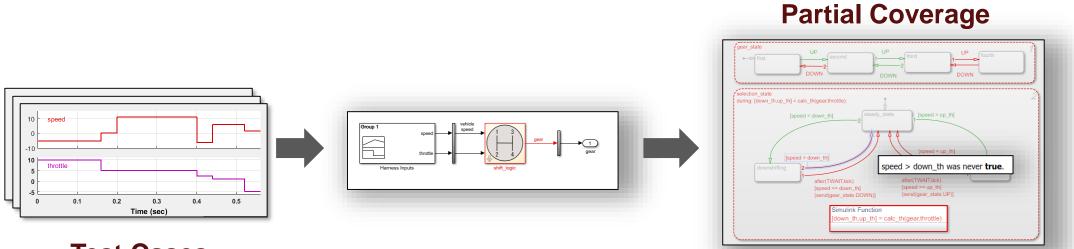


## **Model Based Design Verification Workflow**





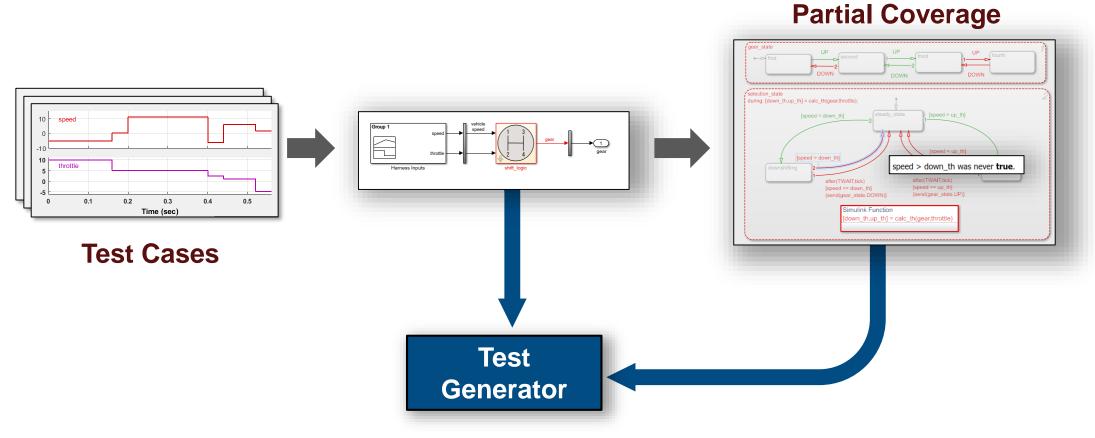
## **Addressing Missing Coverage**



**Test Cases** 



## **Addressing Missing Coverage**



**Simulink Design Verifier** 



**Partial Coverage** 

speed > down\_th was never **true**.

[speed >= up\_th

lection\_state

uring: [down\_th,up\_th] = calc\_th(gear,throttle

speed > down\_th

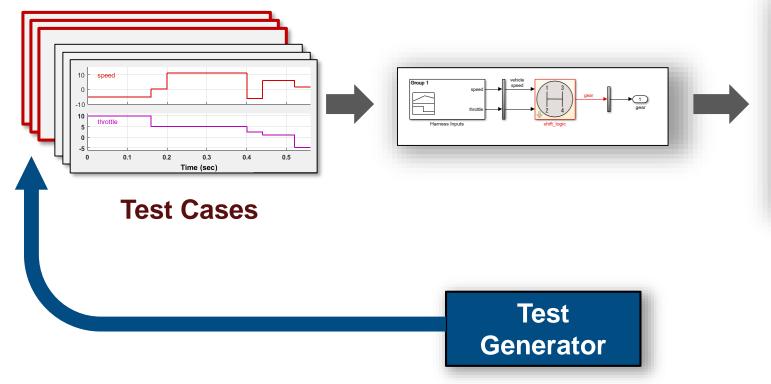
[speed <= down\_th] [send(gear\_state.DOWN)

mulink Function

n\_th,up\_th] = calc\_th(gear,throttle

## **Addressing Missing Coverage**

### **New Test Cases**

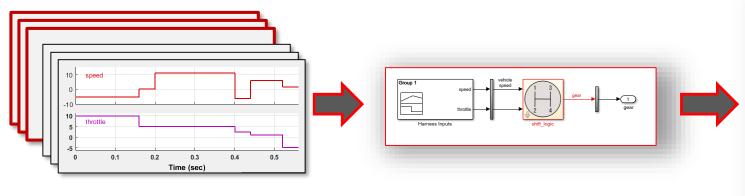


**Simulink Design Verifier** 



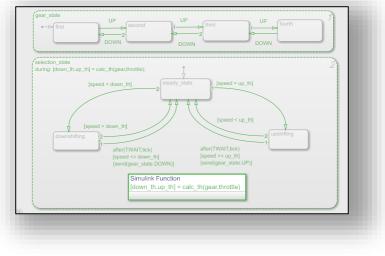
## **Addressing Missing Coverage**

### **New Test Cases**



### **Test Cases**

### **Full Coverage**



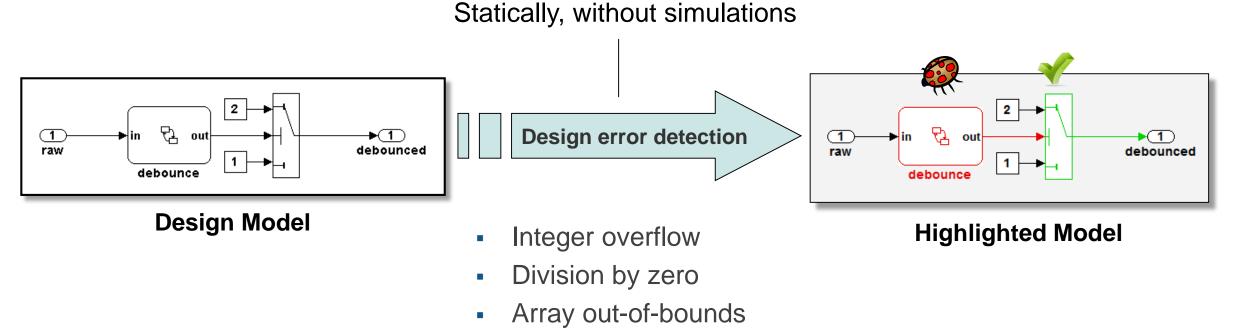


## Why we didn't achieve full model coverage?

- A. Missing tests
- B. Missing requirements
- c. Design errors



## **Detecting Hidden Run-Time Design Errors**



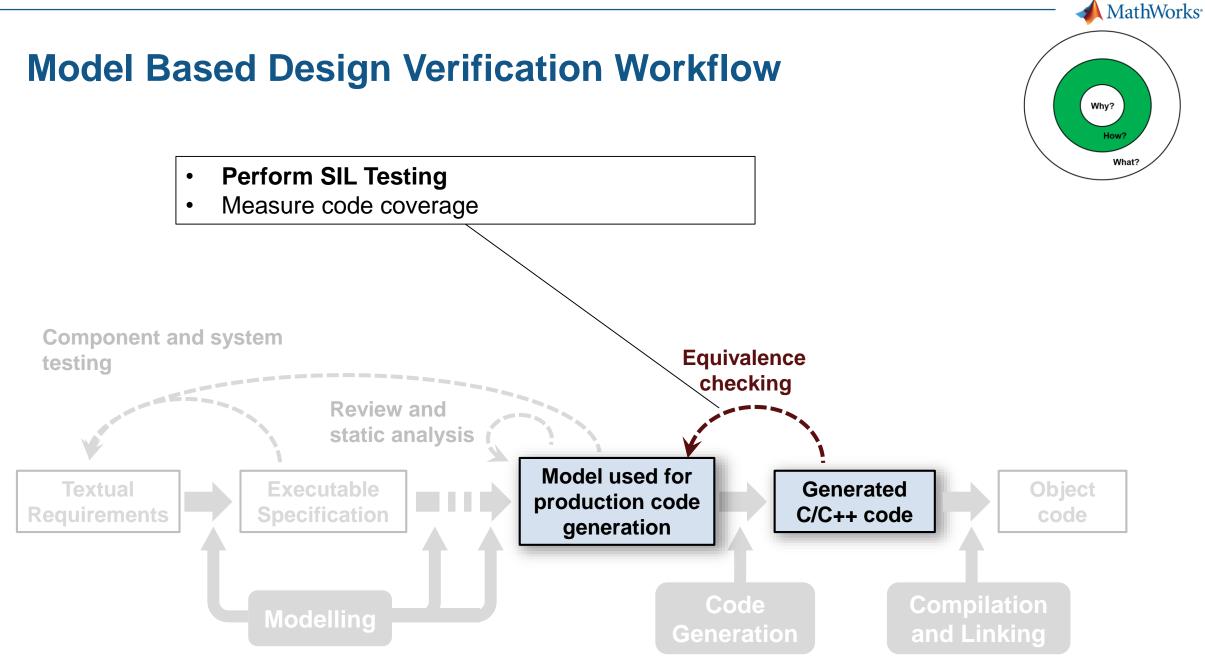
- Range violations
- Dead Logic

### Why? How? What? **Component and system** testing **Review and** static analysis Model used for **Textual Executable** Generated **Object** production code Requirements **Specification** C/C++ code code generation Code Modelling Generation

**Model Based Design Verification Workflow** 

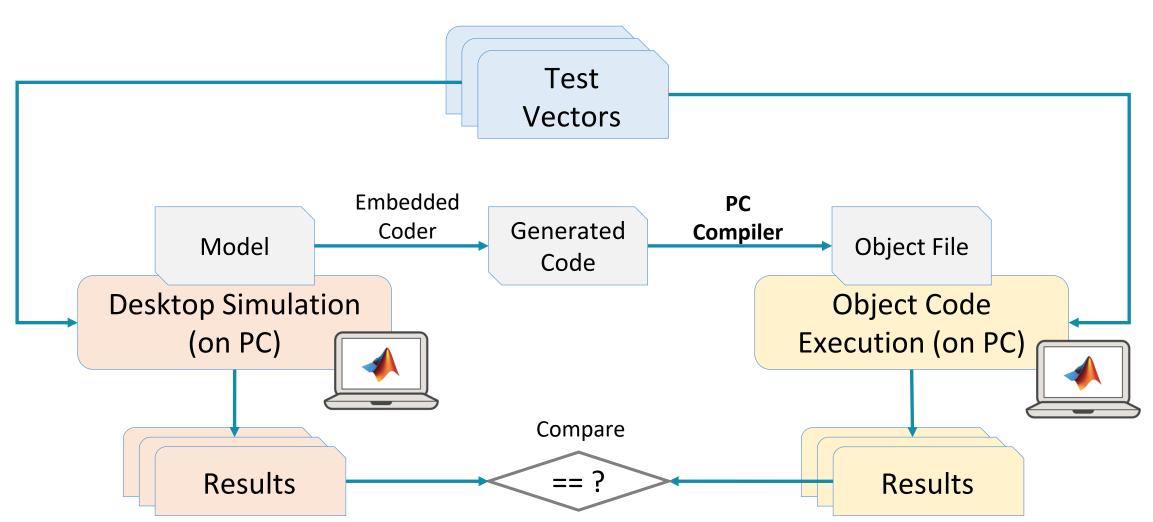
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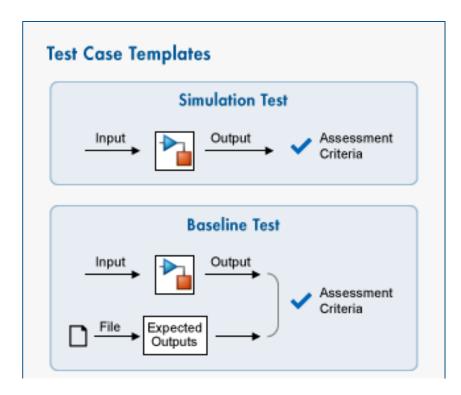
## Software In the Loop (SIL) Testing





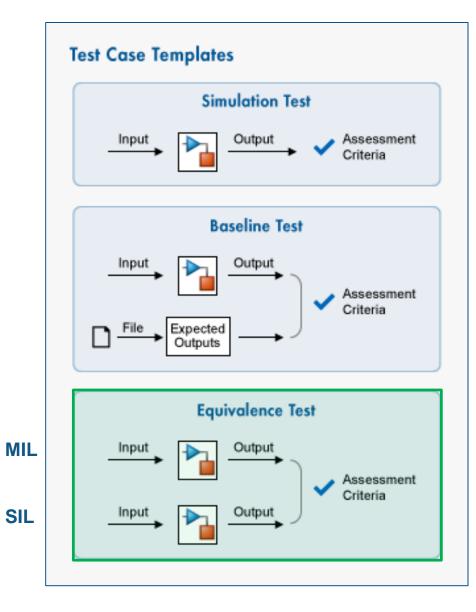
| Test Case Templates              |  |
|----------------------------------|--|
| Simulation Test                  |  |
| Input Output Assessment Criteria |  |

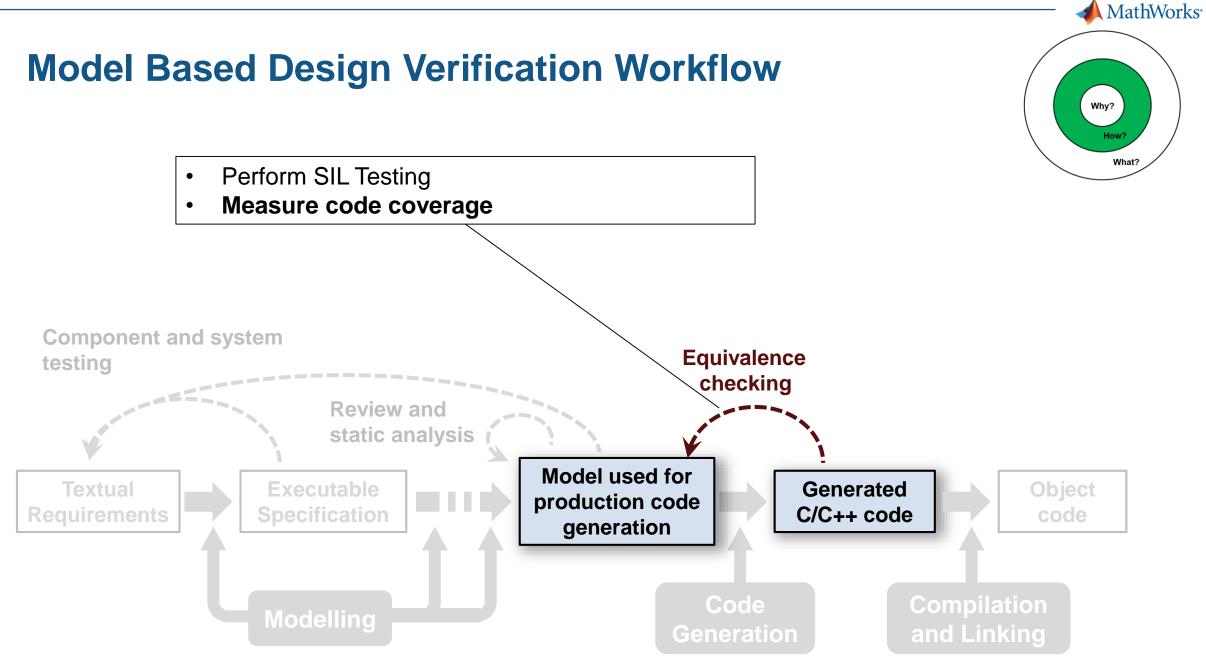




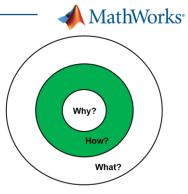


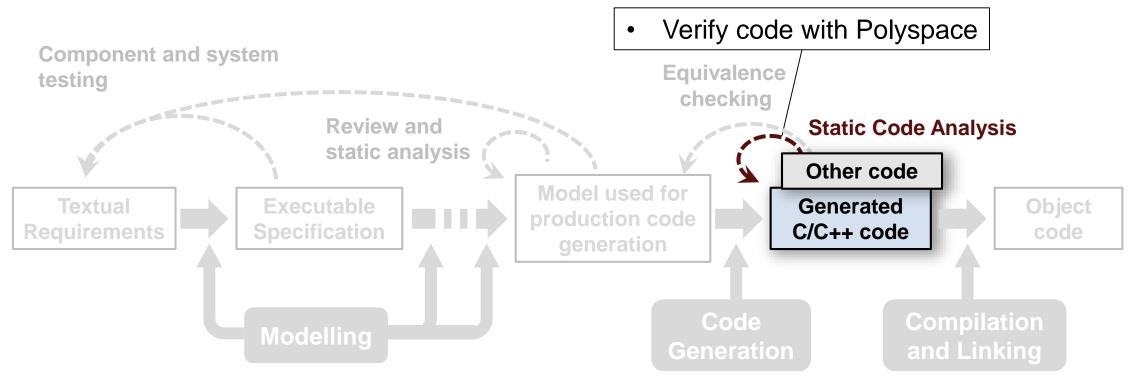
## **MIL vs SIL**





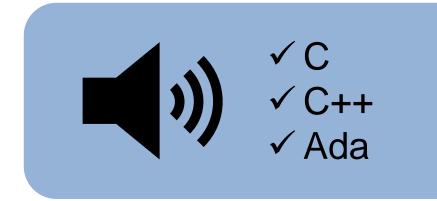
## **Static Code Analysis**





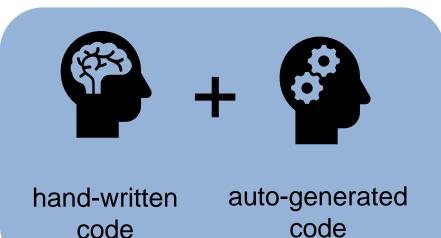


## **Polyspace Tools**





Method: <u>Formal Method based</u> semantic analysis →Abstract Syntax Interpretation

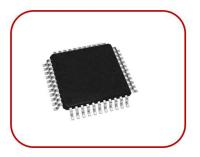


### Goal:

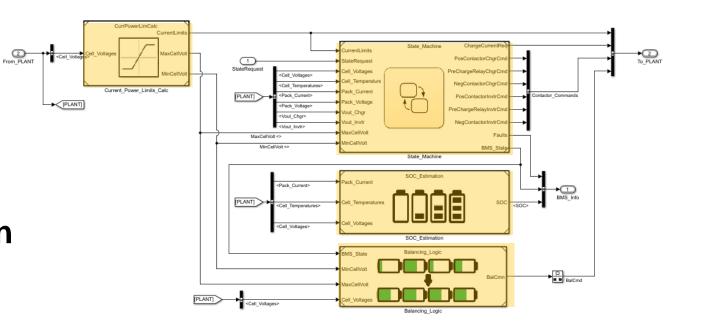
- ✓ Find Runtime Errors (division by zero, overflows, etc.)
  - Find MISRA violations
  - ✓ Provide code metrics
  - ✓ Prove absence of Runtime Errors



## **Battery Management System (BMS)**

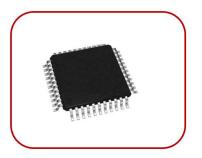


- Software Architecture
- SW Module Design
- Test, Verification & Validation
- BMS Integration Testing

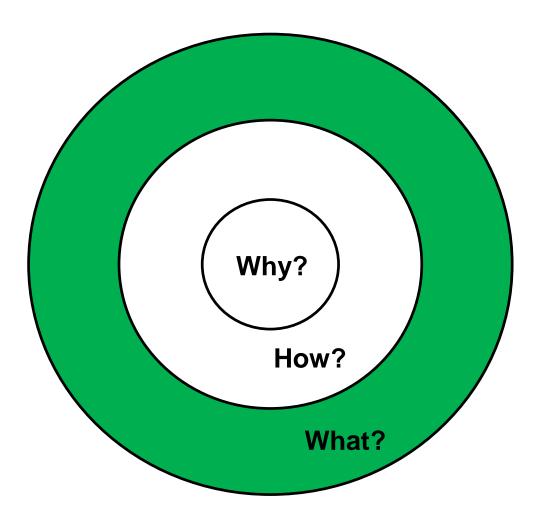




## **Battery Management System (BMS)**

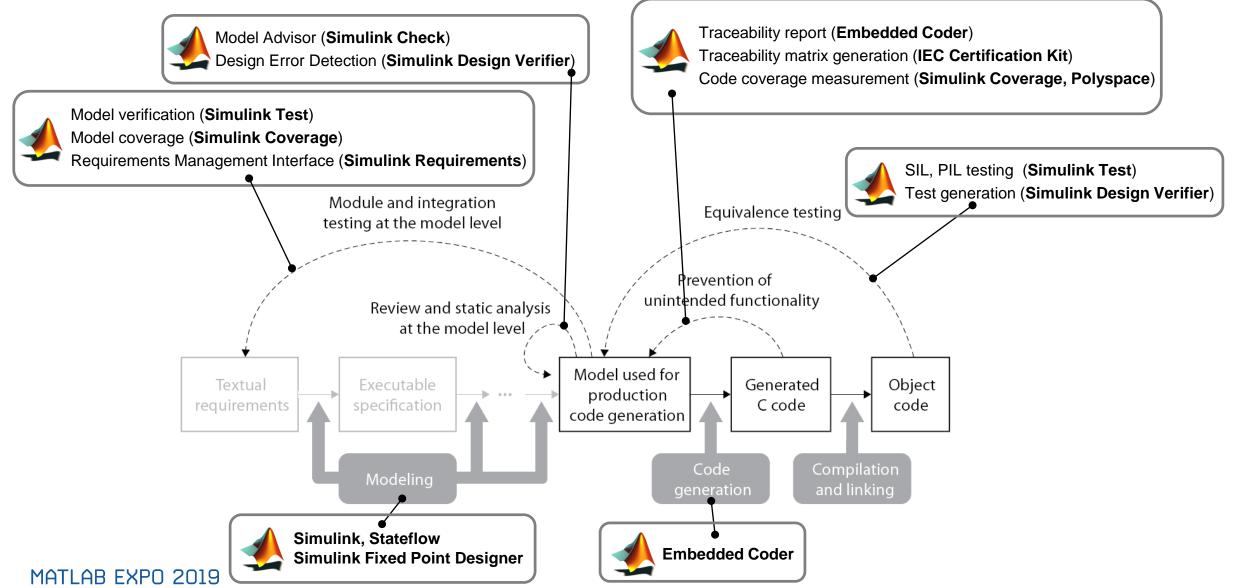


- Software Architecture
- SW Module Design
- Test, Verification & Validation
- BMS Integration Testing



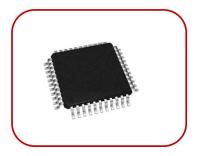


## **Model Based Design Verification Workflow**

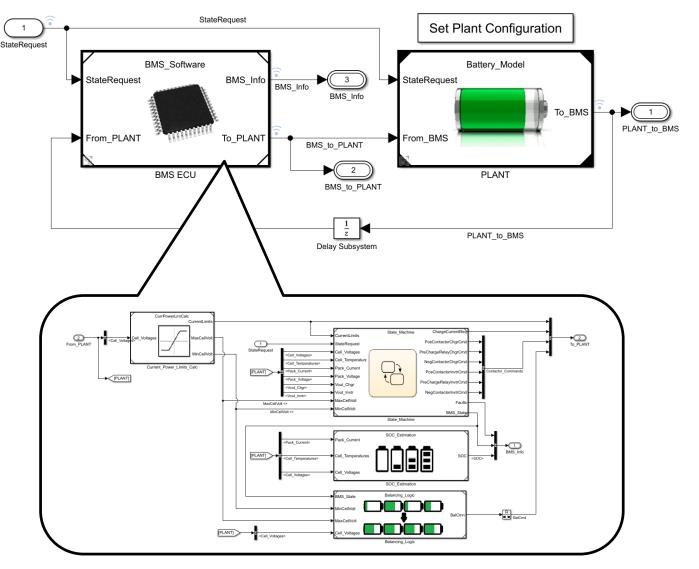




## **Battery Management System (BMS)**

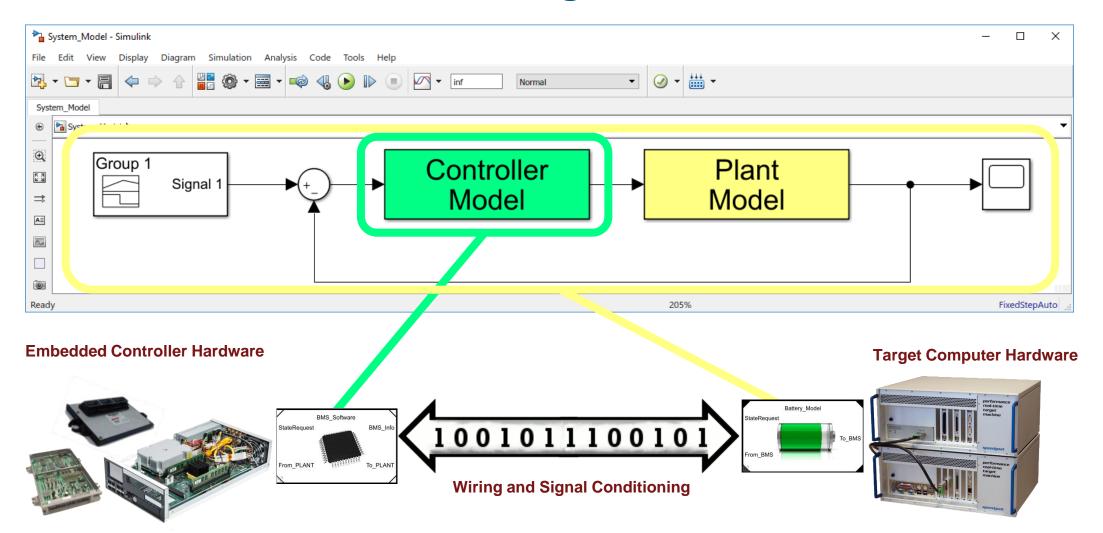


- Software Architecture
- SW Module Design
- Test, Verification & Validation
- BMS Integration Testing



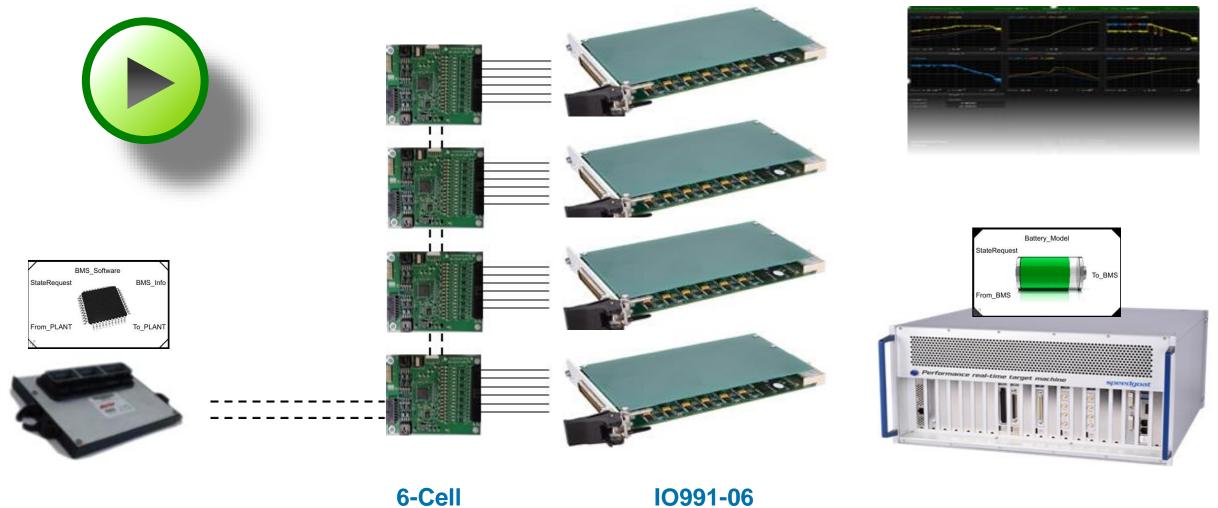


## **Real-time Simulation and Testing**





## **HIL Testing – Speedgoat Solution**



6-Cell Modules



