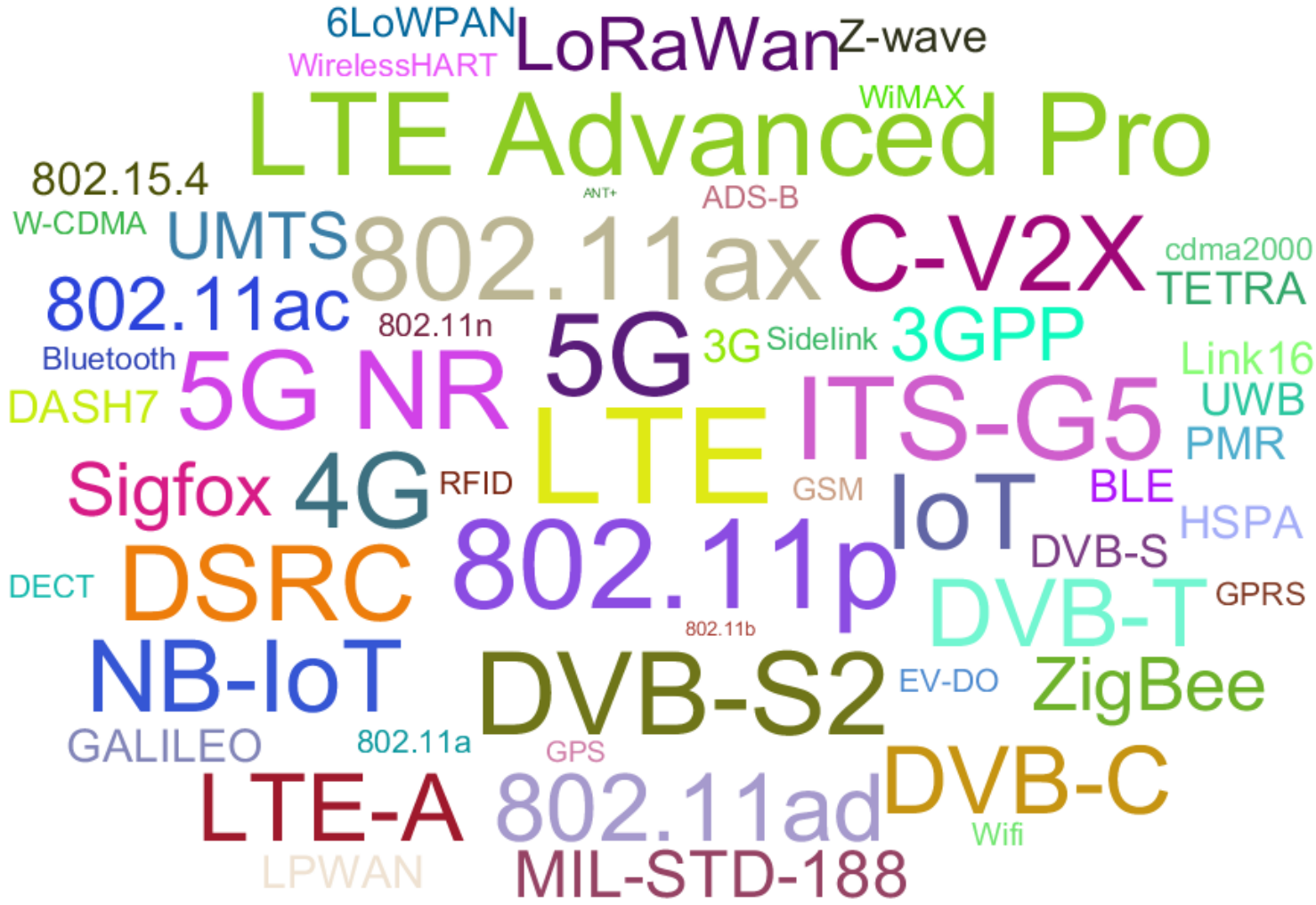
MATLAB EXPO 2018

Simulation, prototyping and verification of standards-based wireless communications

Gerald Albertini

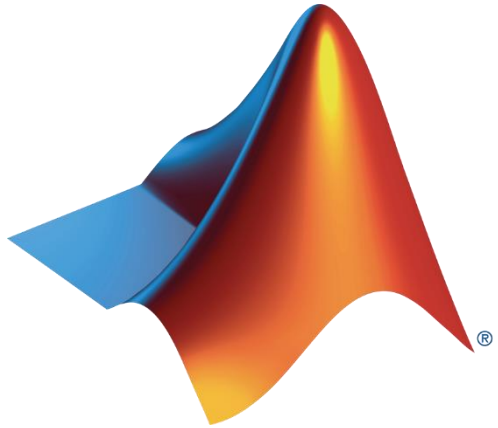
A Myriad of Wireless Standards

…and growing complexity

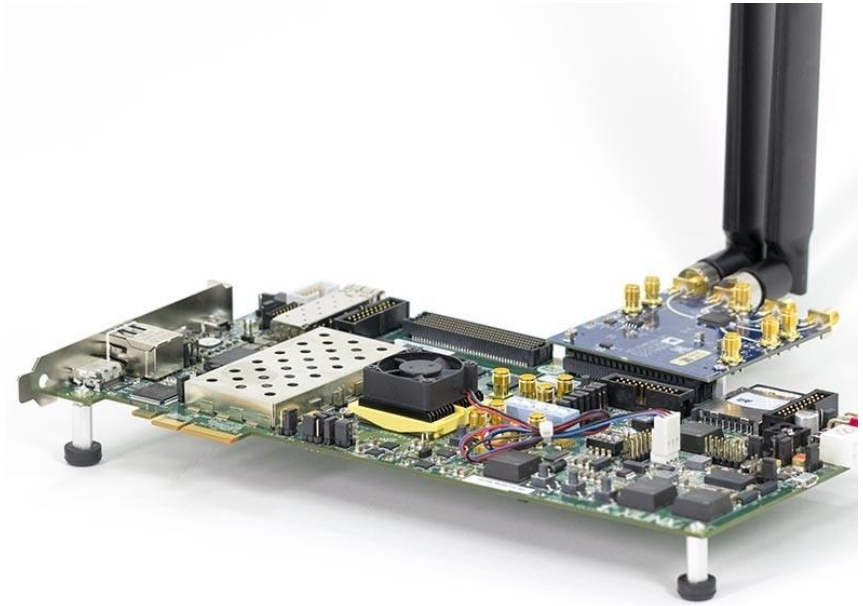


From Design to Prototype
and beyond

- A **common** design environment across multiple teams
- Target **off-the-shelf** hardware for **prototype** development
- Minimize time to market



MATLAB&SIMULINK



Modeling Wireless Standards with MATLAB & Simulink

LTE

5G

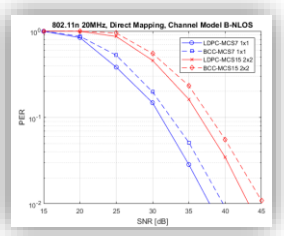
WLAN

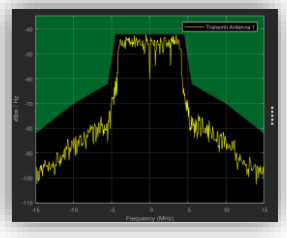
UMTS/cdma2000

ZigBee

NFC

Typical Use Cases





```
VHT format detected
Decoding L-SIG...
L-SIG check pass
L-SIG EVM: 1.89% RMS
RXTIME: 84us
Number of samples in packet: 6720
```

Golden Reference for Verification

Verify in-house PHY models

End-to-End Link-Level Simulation

How do design choices affect system performance?

Signal Generation and Analysis

Test with live data

Signal Information Recovery

Decode real-world signals

WLAN System Toolbox

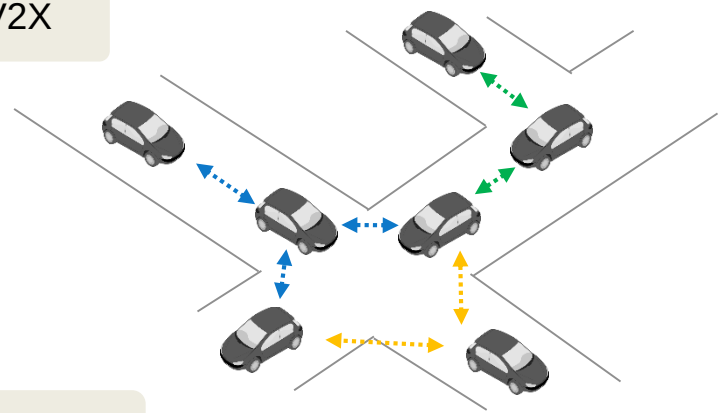
Supported Standards

802.11ah

S1G – Sub 1 GHz
900 MHz
long range
low power
IoT

Non-HT
5.9 GHz
V2V/V2X

802.11p



VHT – Very High Throughput
HT – High Throughput
Non-HT
2.4/5 GHz
medium range
general access

802.11b/g/n

802.11a/ac/ax

802.11ad

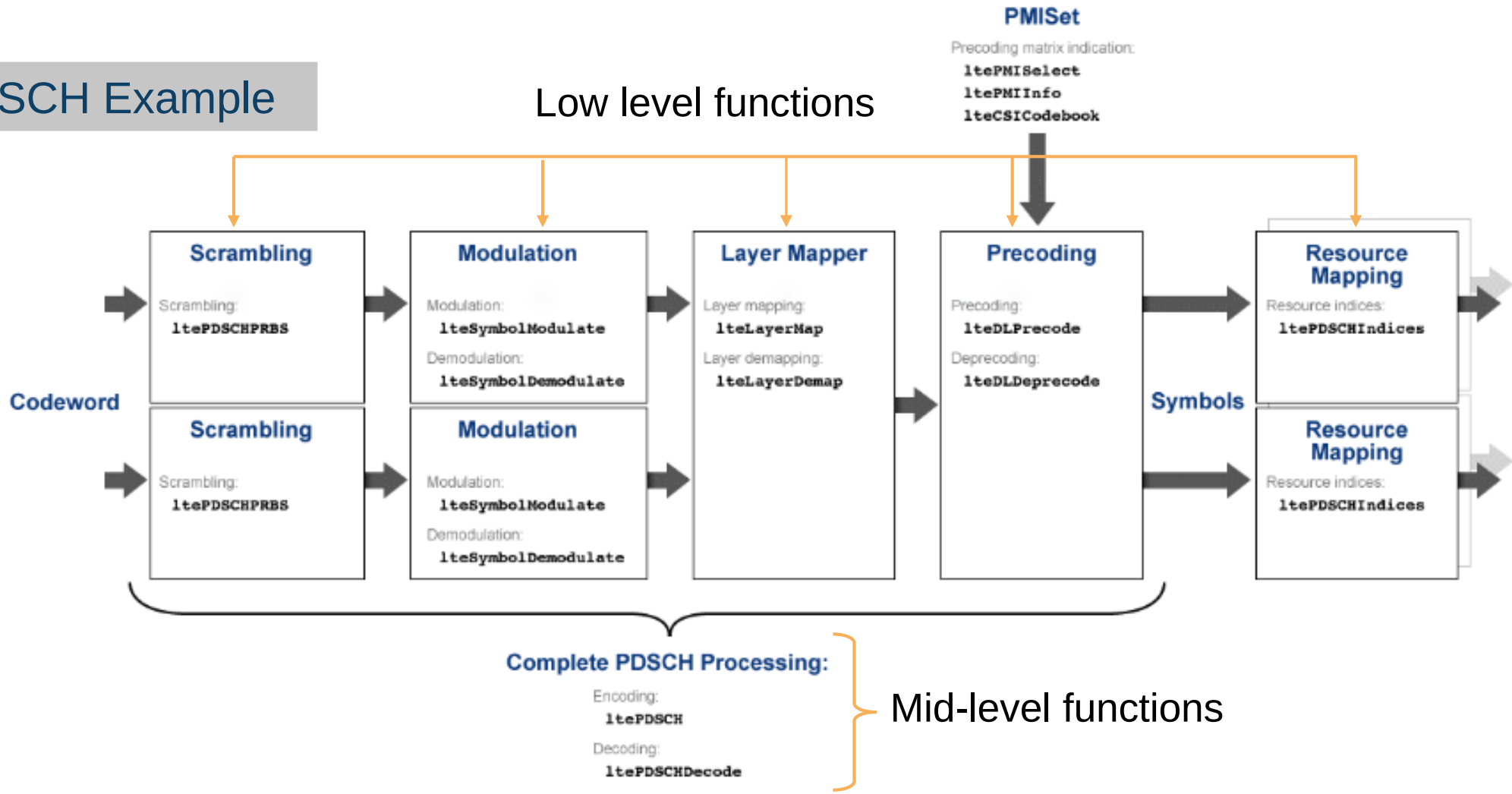
DMG – Directional Multigigabit
60 GHz,
short range
high throughput wireless video

LTE System Toolbox

Granularity

PDSCH Example

Low level functions

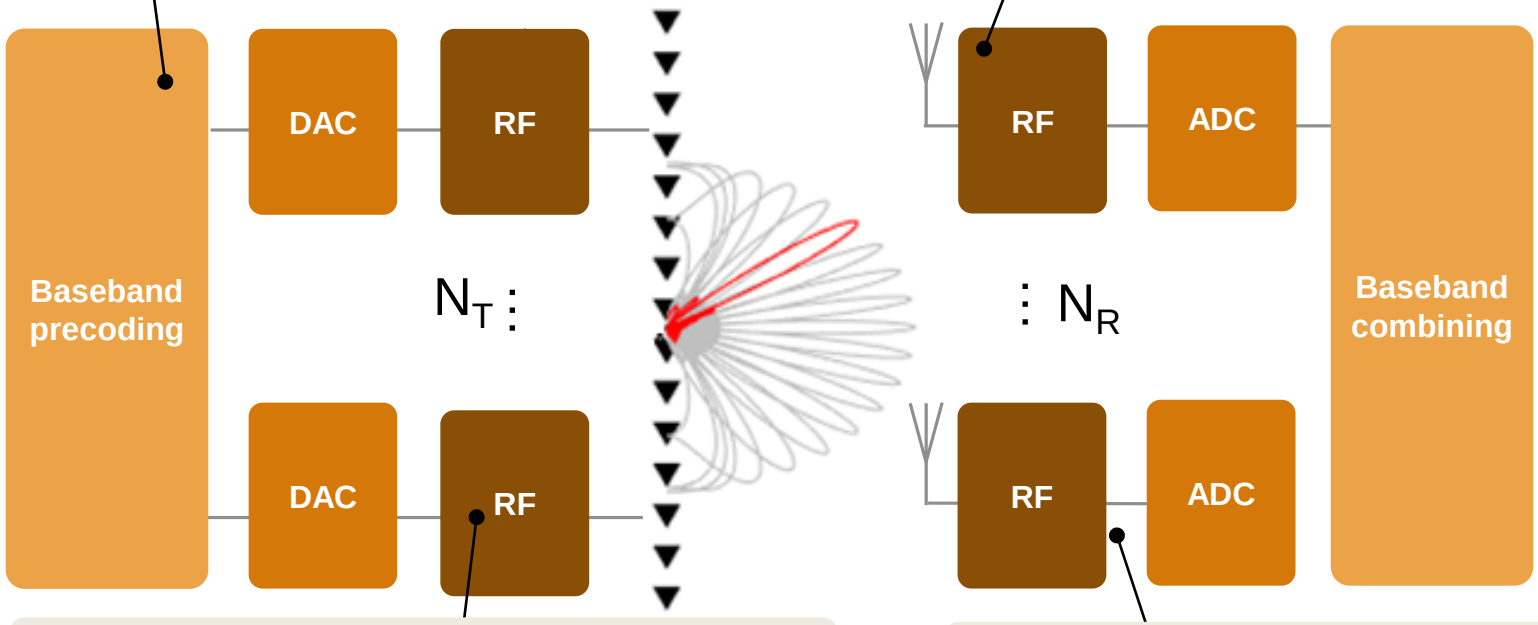


Mid-level functions

Wireless Modeling Challenges

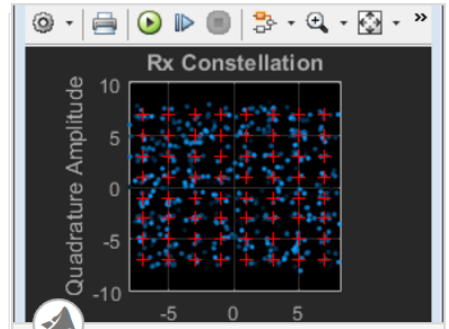
Baseband DSP development
- Is my implementation correct?
- Evaluate link performance (algorithm)?

Antenna array design and evaluation
- Element coupling
- Edge effects



Explore beamforming trade-offs
- Baseband, analogue or hybrid
- Simulate capabilities and limitations
- Trade-off ADCs vs RF components

Impact of RF impairments
- Frequency dependency
- Non-linearities
- Mismatches and coupling



Wireless Digital Video Broadcasting with RF Beamforming

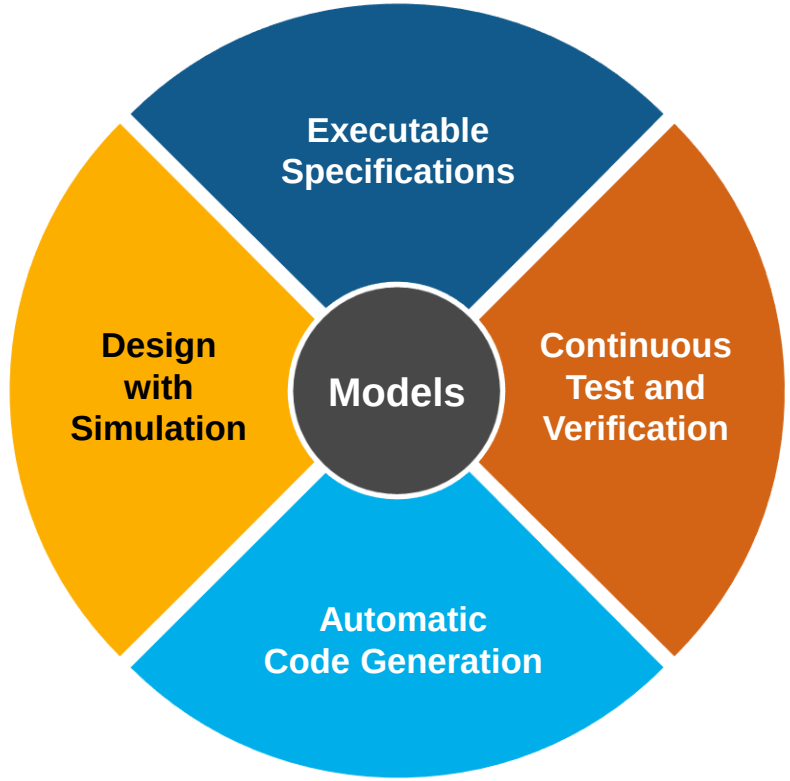
Model a digital video broadcasting system which includes phased array antennas. The baseband transmitter, receiver and channel are realized

Open Script

Wireless design challenges

The Model Based Design Advantage

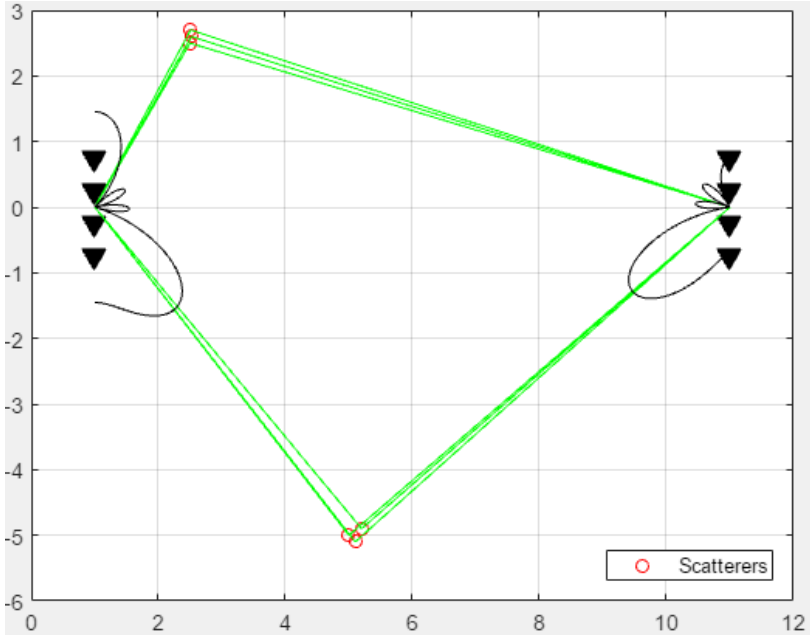
- System Architecture
- Mixed-Signal Hardware
- Antenna Design
- DSP Algorithms
- Digital Hardware
- Software Development
- RF Design



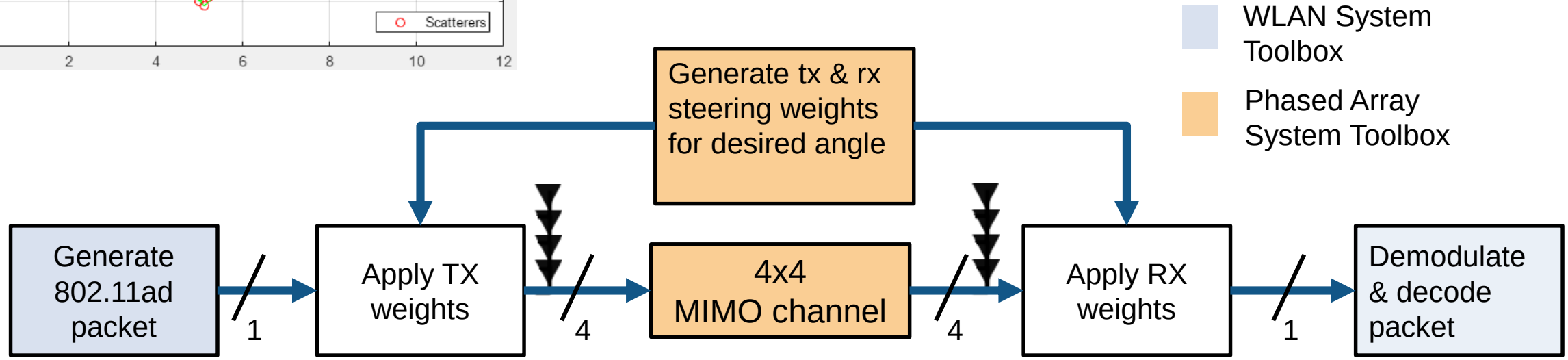
Requires 7 different skills to be successful!

at least

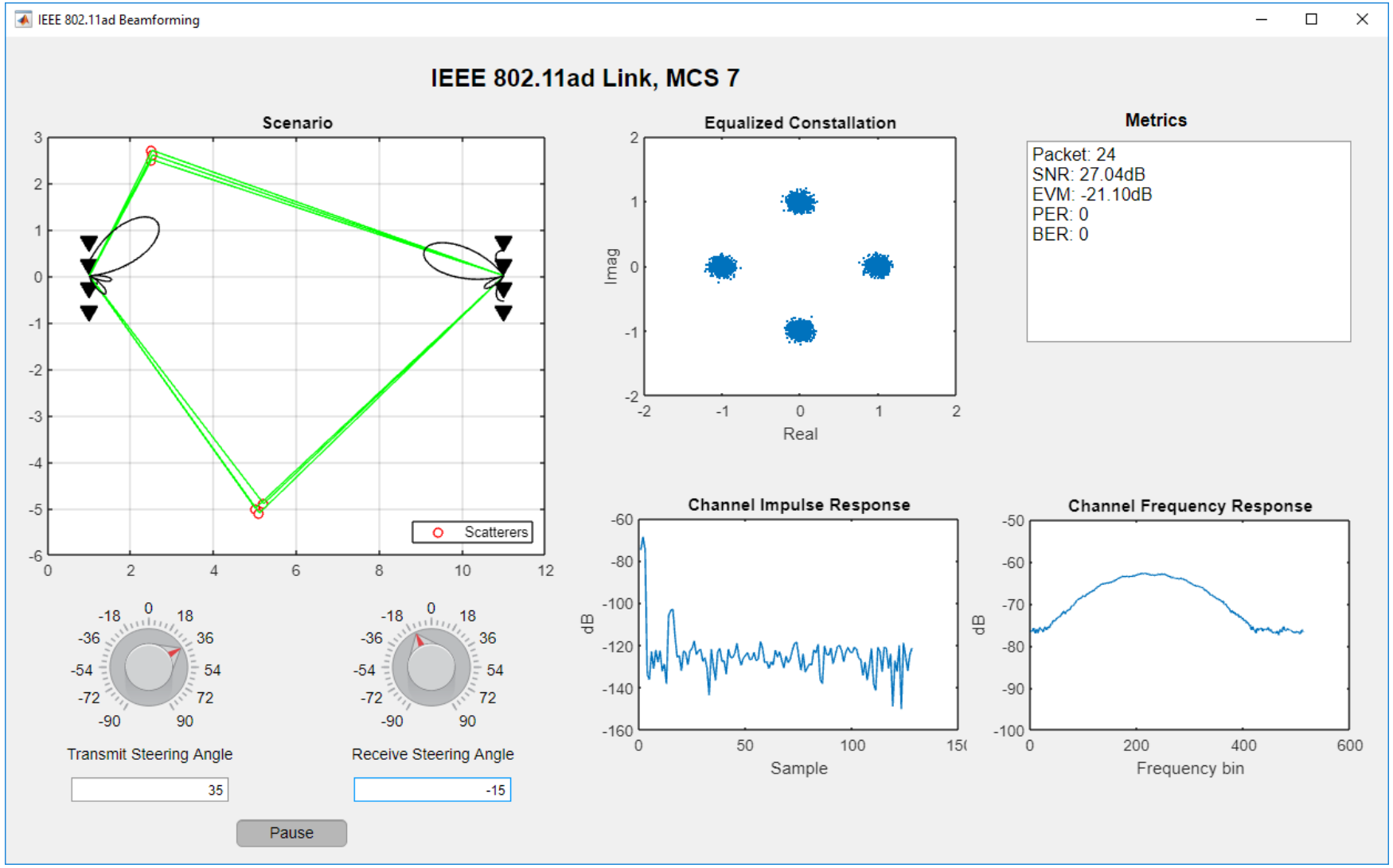
DEMO Modeling 802.11ad – Including Beamforming



- Uniform linear array of 4 elements (TX & RX)
- MIMO channel with 6 scatterers
- PER and EVM for 802.11ad link

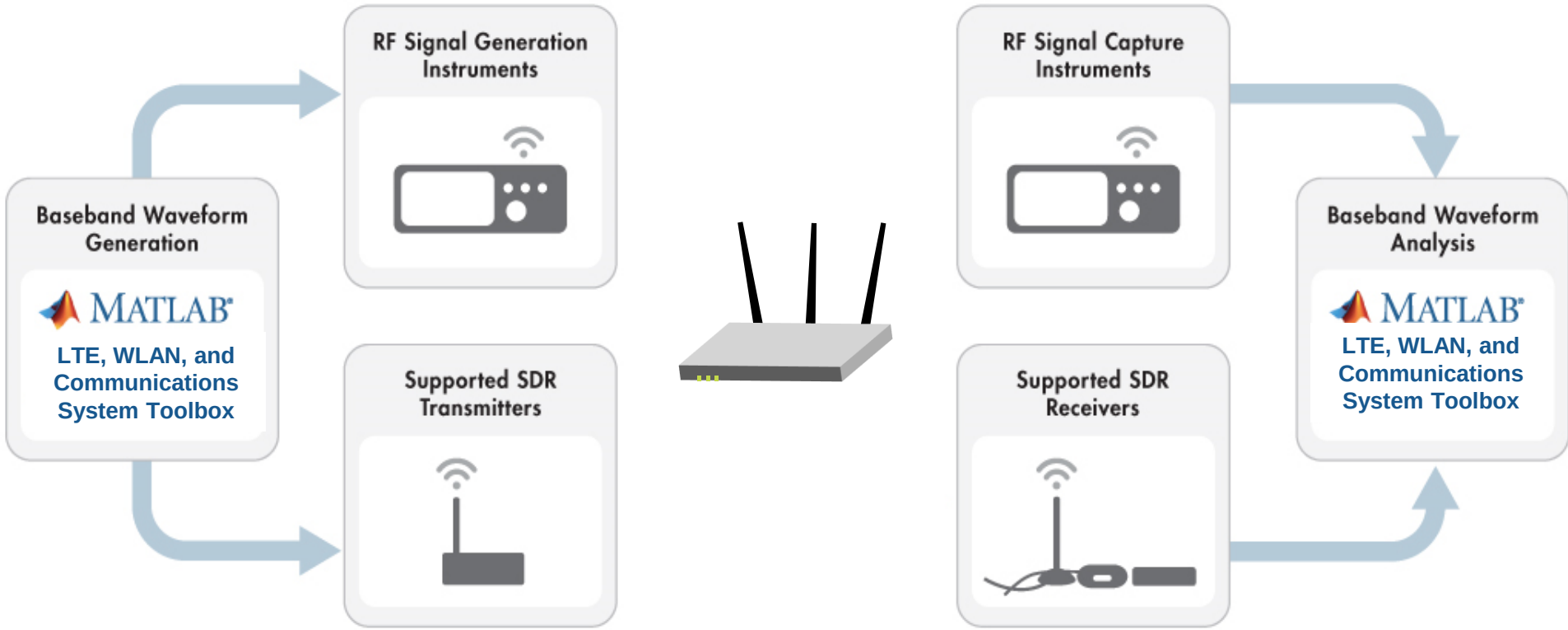


Modelling 802.11ad Beamforming



Working with Real Signals

Going beyond simulation



Supported Hardware for Radio Connectivity

Decreasing Cost

Signal Generator and Analyser

Keysight, R&S, NI, Tektronix, …
High quality RF front end
Wide frequency range, high bandwidth

SDR

USRP, PLUTO, Zynq, …
Customizable RF front end
Sizable FPGA for targeting designs

Ultra low-cost SDR

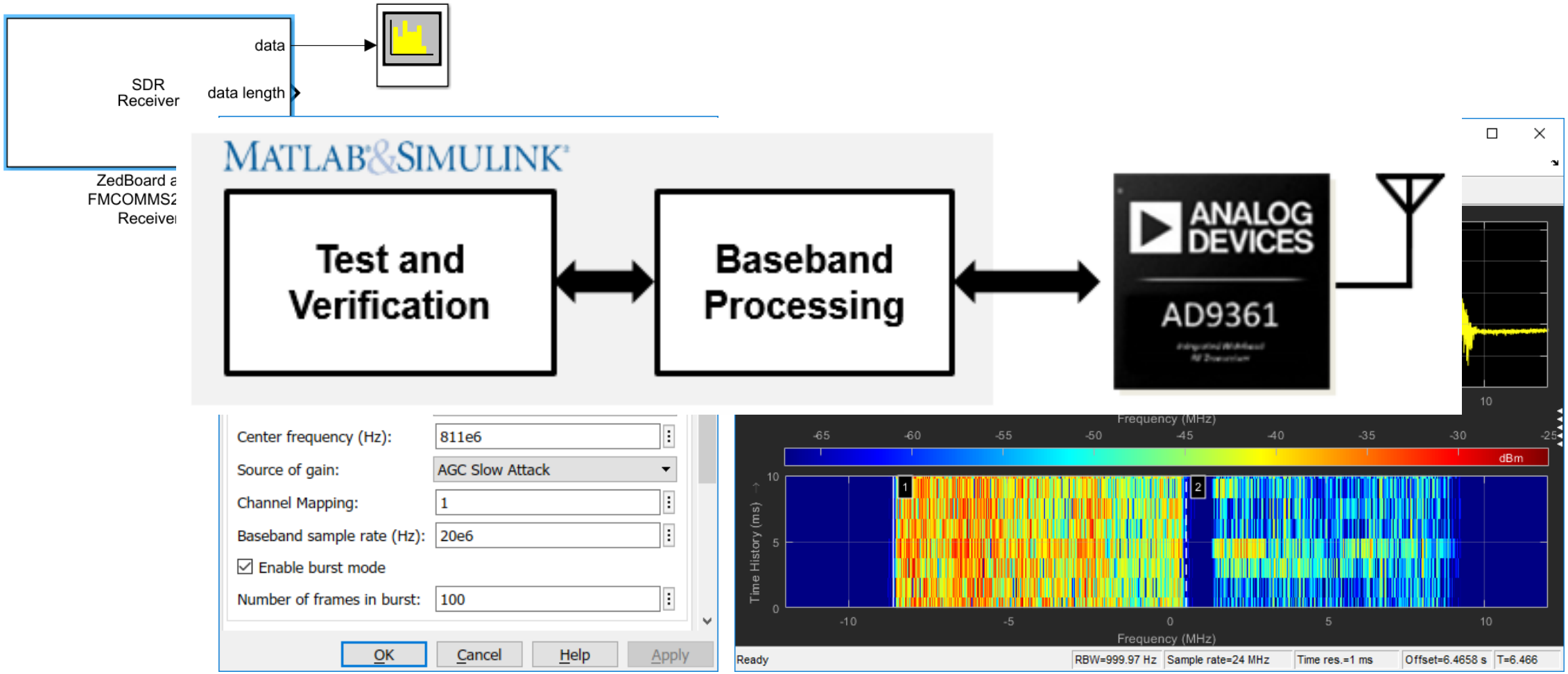
RTL-SDR, …
Low bandwidth
Receive only

Instrument Control Toolbox

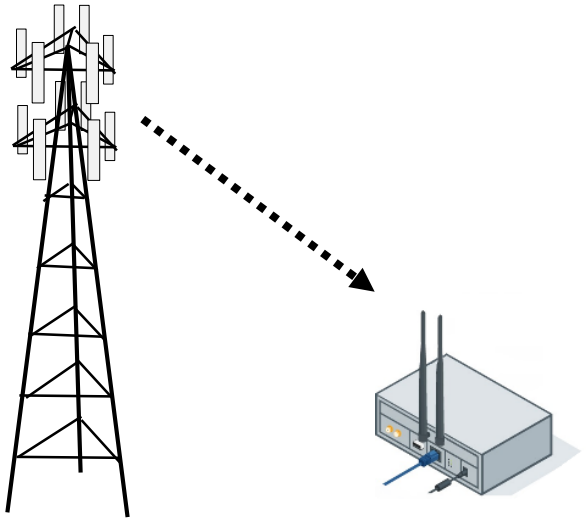
SDR Hardware Support Package

DEMO Radio I/O

Stream Over the Air signals – Explore spectrum



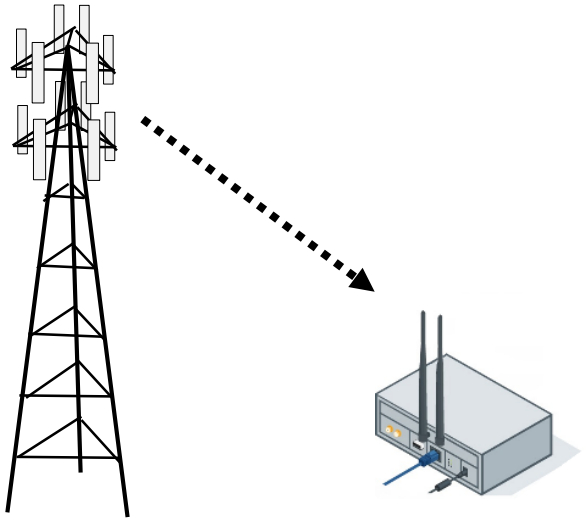
Highlights Modelling MIB Decoding



- Emulate the User Equipment using a SDR
- Implement LTE Cell Search procedure
- Physical layer processing:
  - Cell search
  - Time and frequency offset estimation and correction
  - OFDM demodulation
  - Channel estimation and equalization
  - PBCH Demodulation
  - BCH Decoding
  - MIB Parsing

3GPP TS36.331 Section 6.2.2

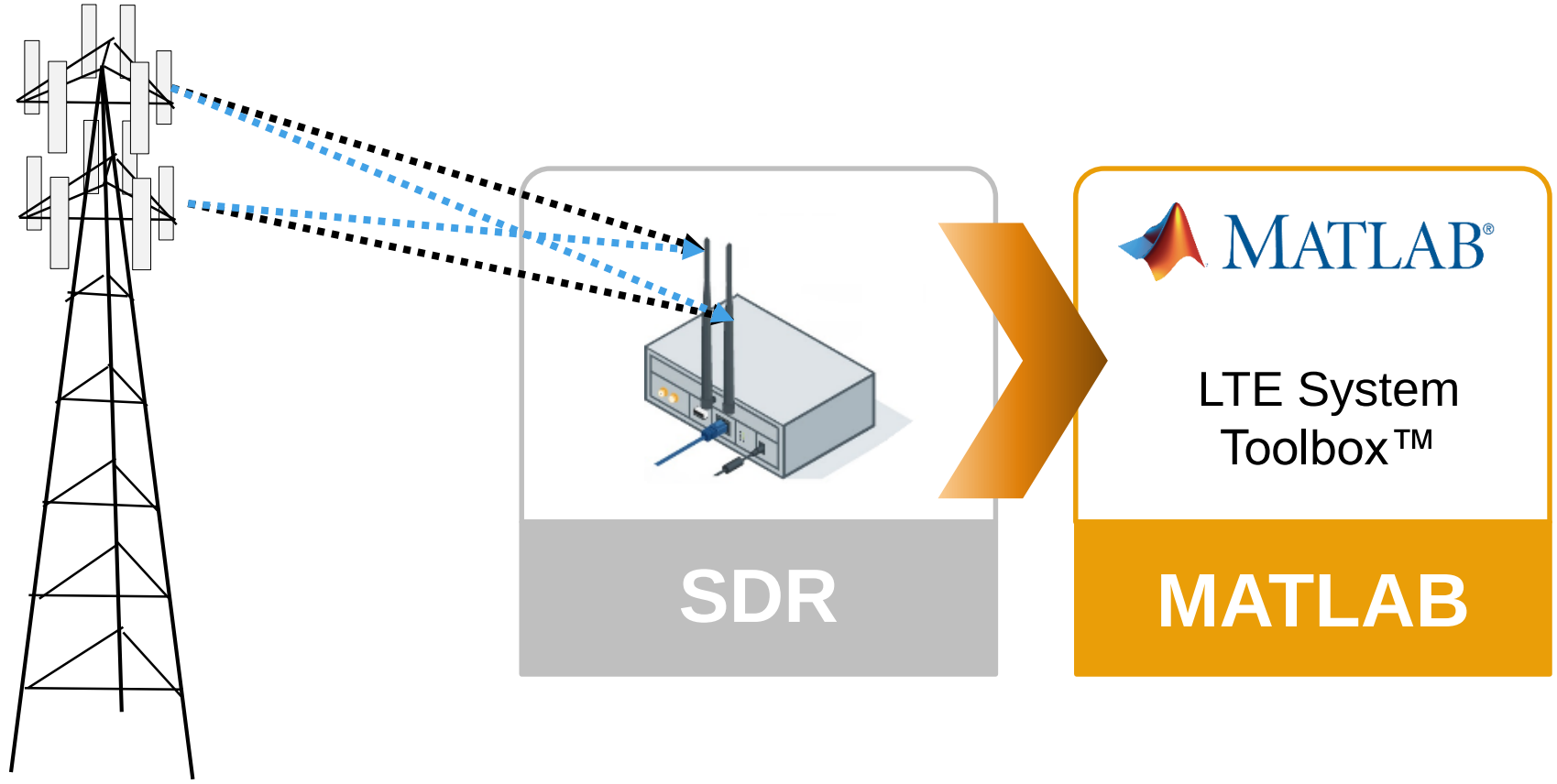
Highlights Modelling MIB Decoding



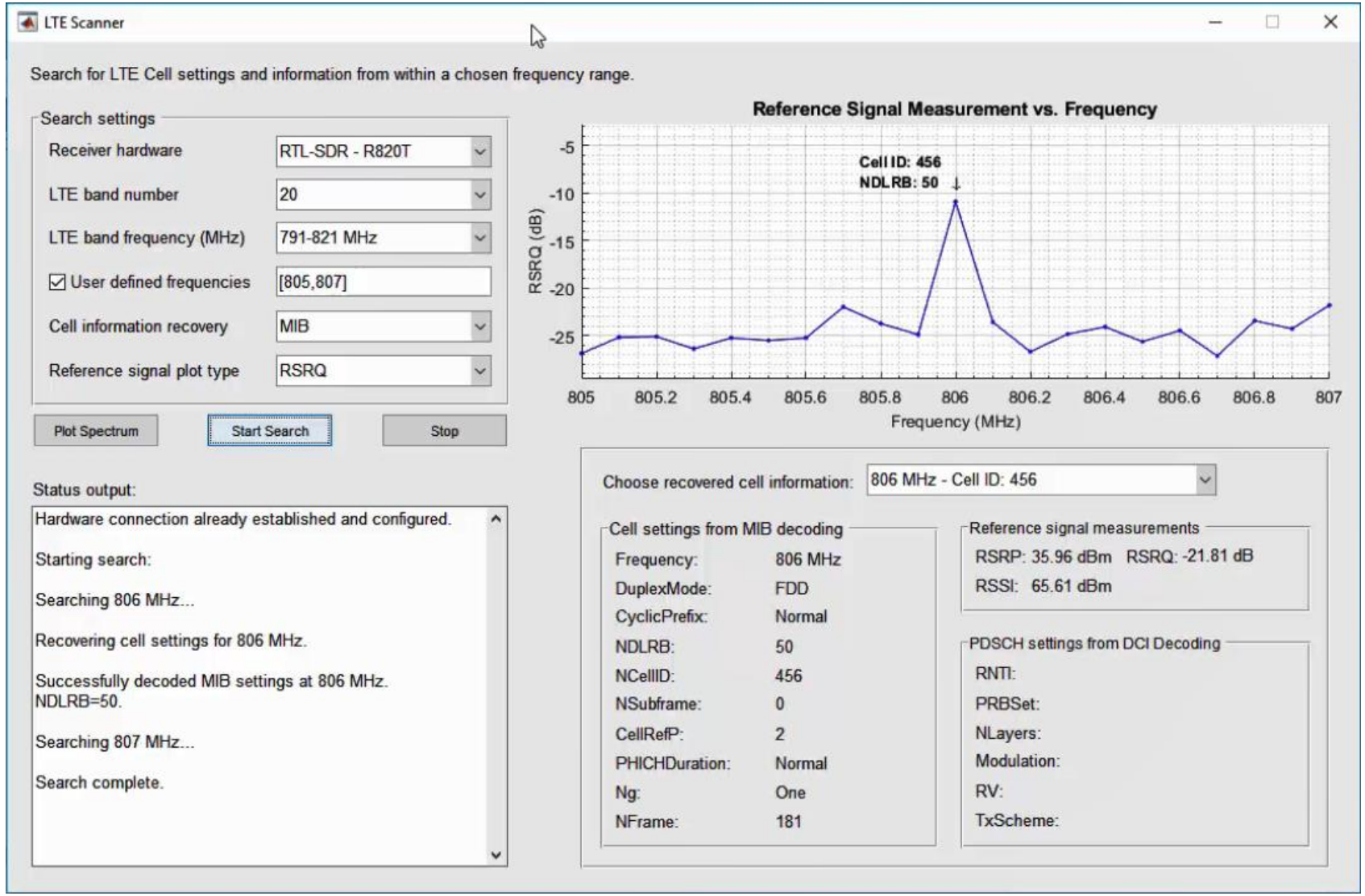
- **Golden reference**
  - Ensure my implementation is correct
  - E.g. PSS/SSS sequence for cell search
- **Algorithm development**
  - Link-level simulation to analyse receiver IP performance
  - E.g. channel estimation
- **Verification**
  - Capture and decode over-the-air waveforms offline
  - Verify behaviour before moving to HW

3GPP TS36.331 Section 6.2.2

DEMO LTE Scanner



LTE Cell Scanner

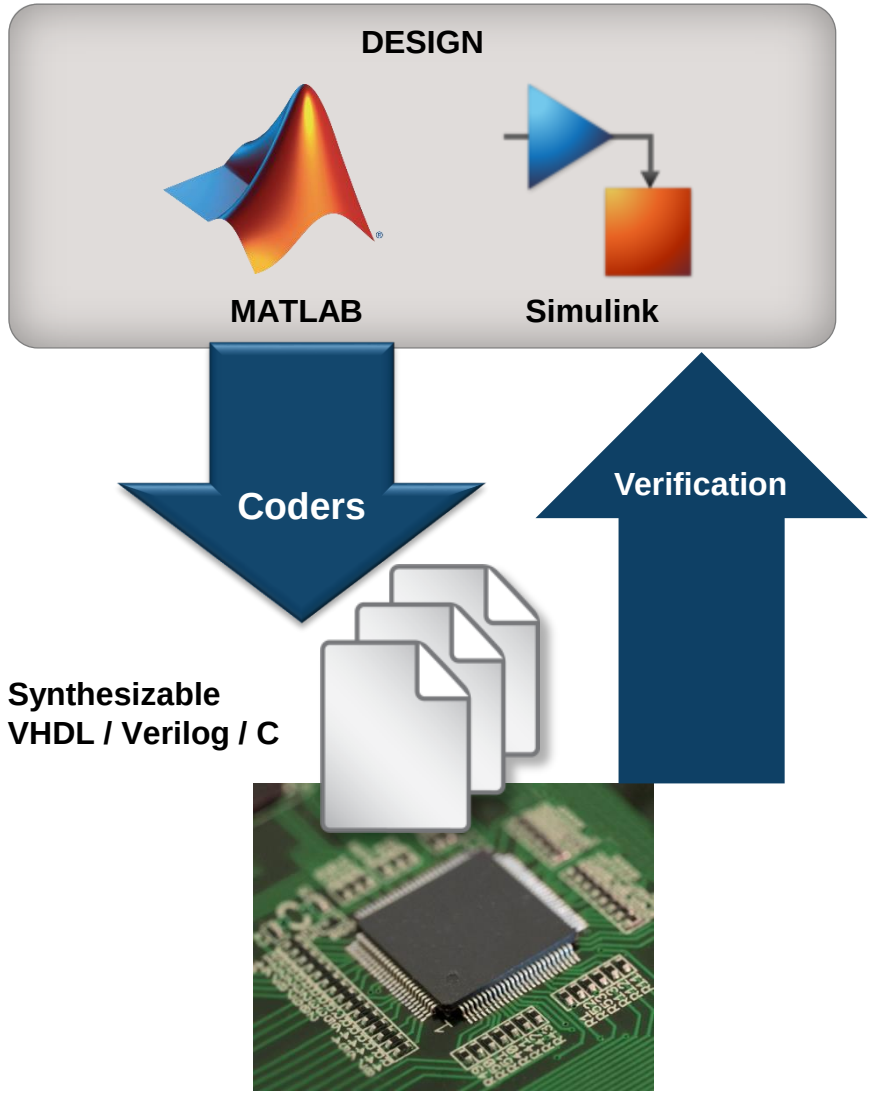


From Design To Hardware

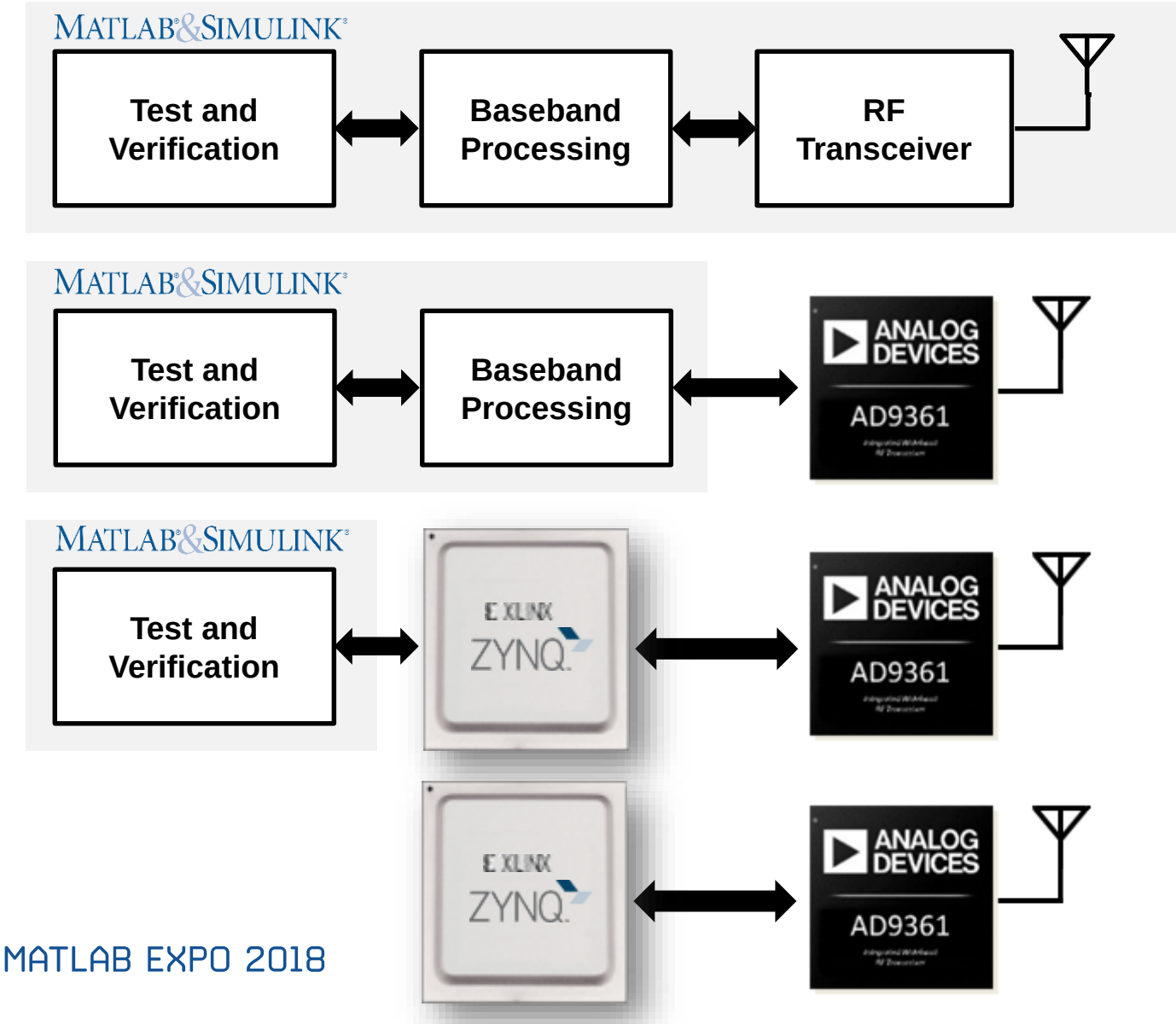
MATLAB
- Large data sets
- Explore mathematics
- Data visualization

Simulink
- Model HW Parallel architectures
- Simulation
- Code Generation Capabilities

Targeting FPGA and ASIC
- Streaming design
- Implementation detail
- Architectural specification
- Verification



Typical Workflow



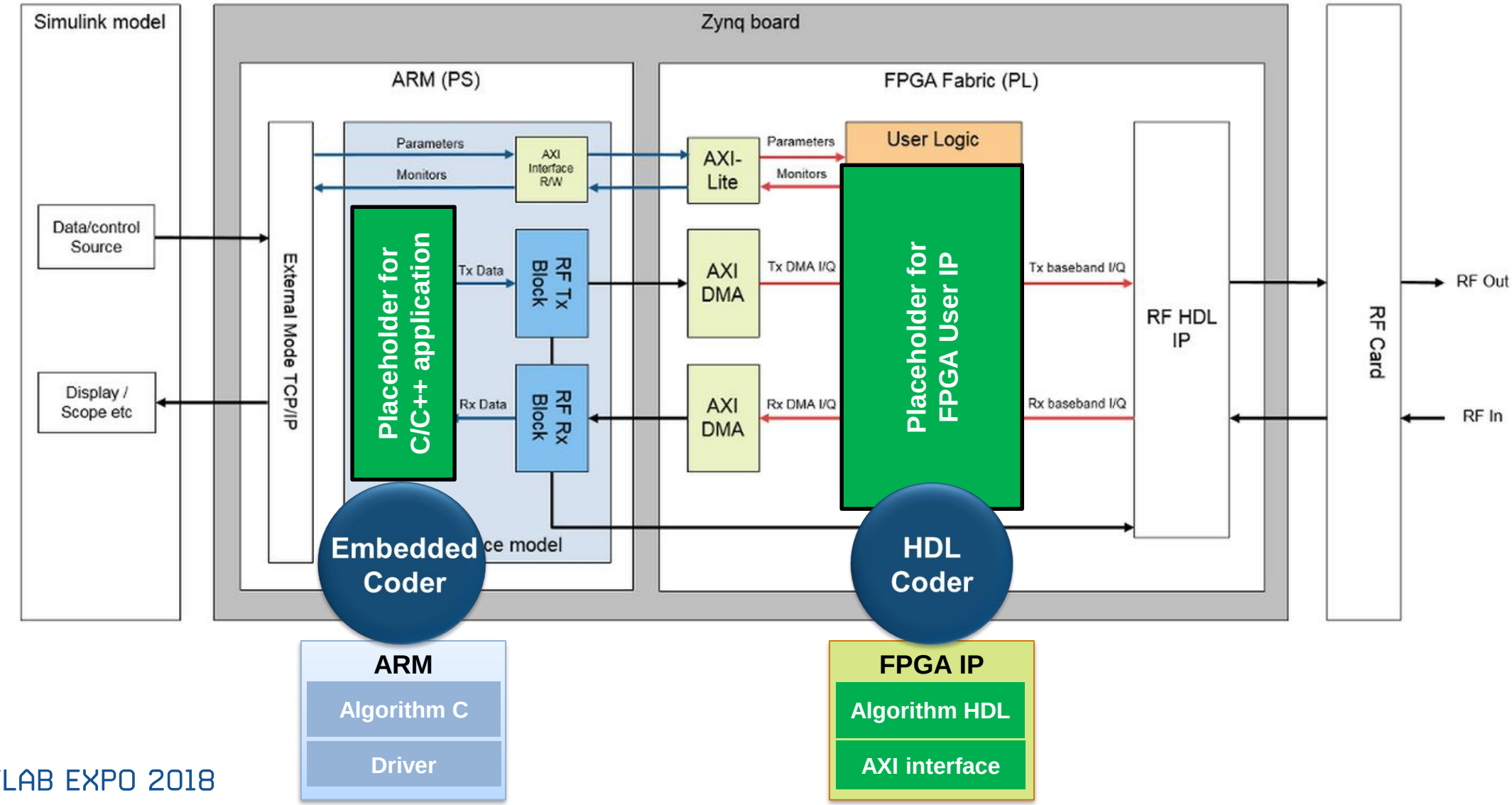
Modeling & Simulation

Radio I/O
Streaming real-world data

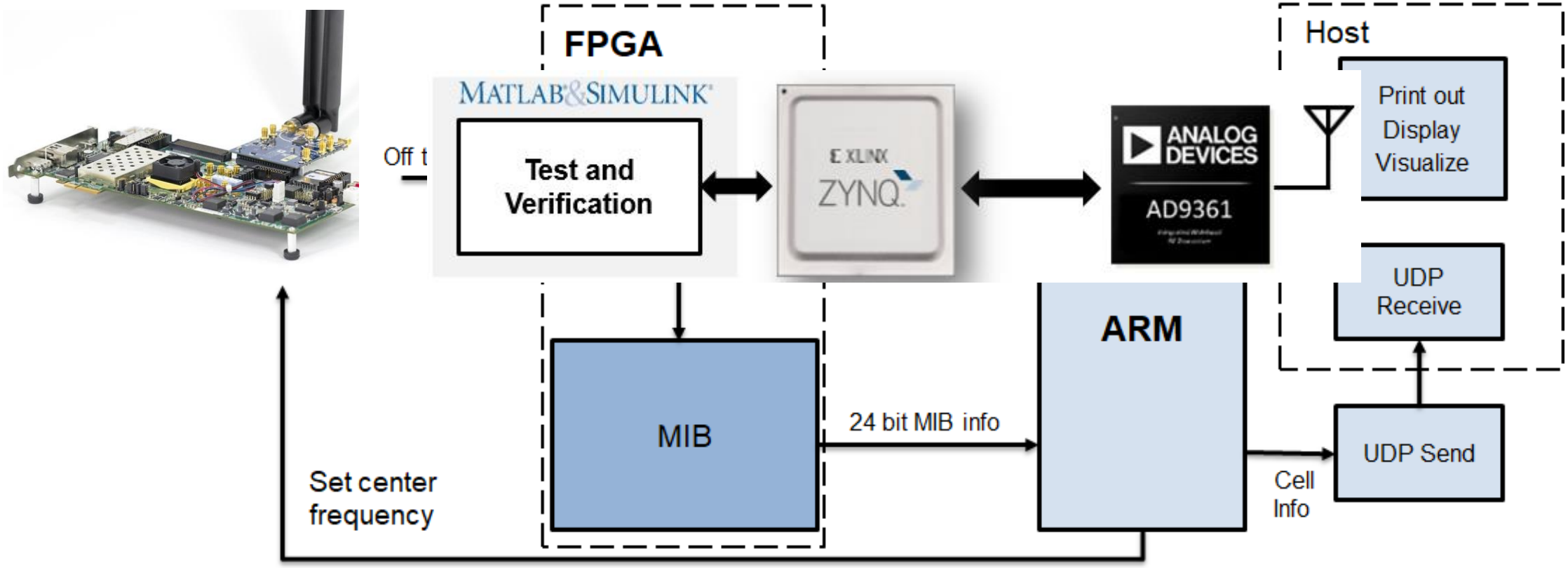
Deploy on hardware

Standalone operation

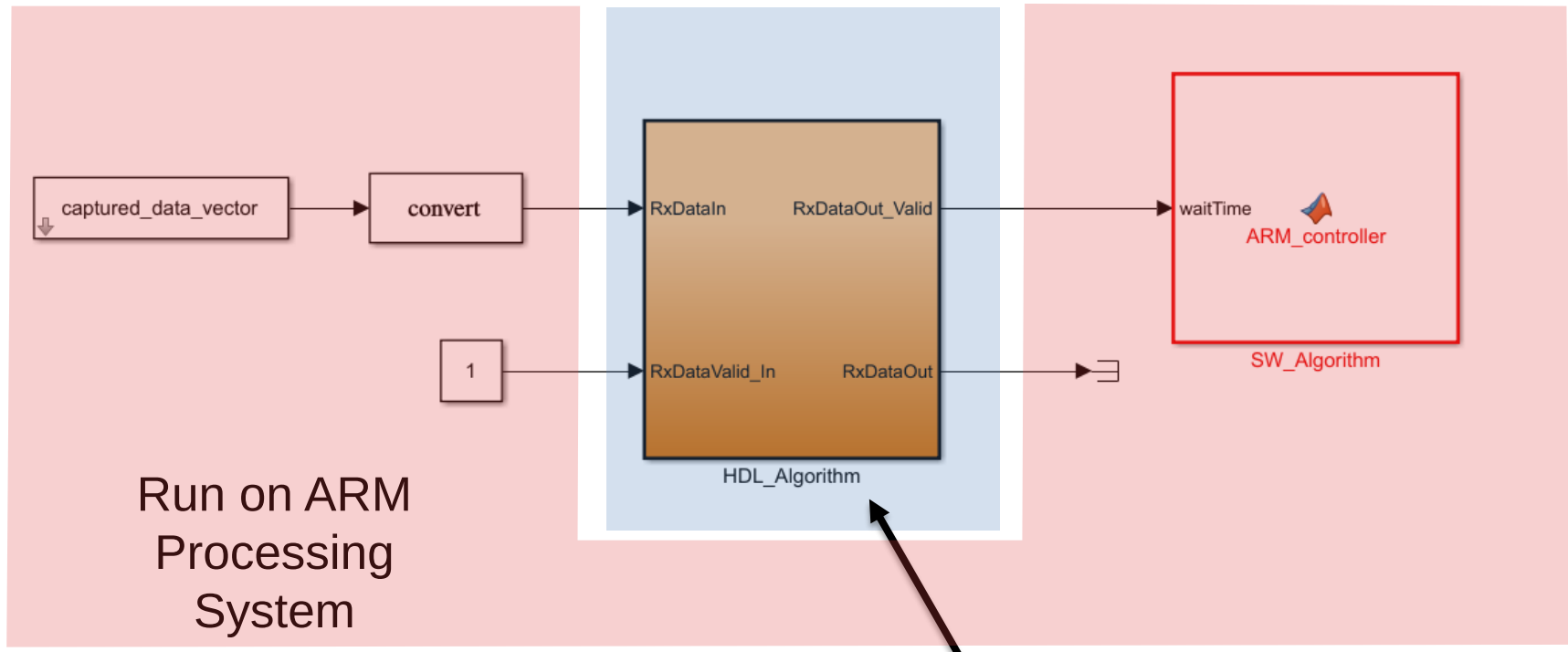
Zynq SDR - Hardware Support Package



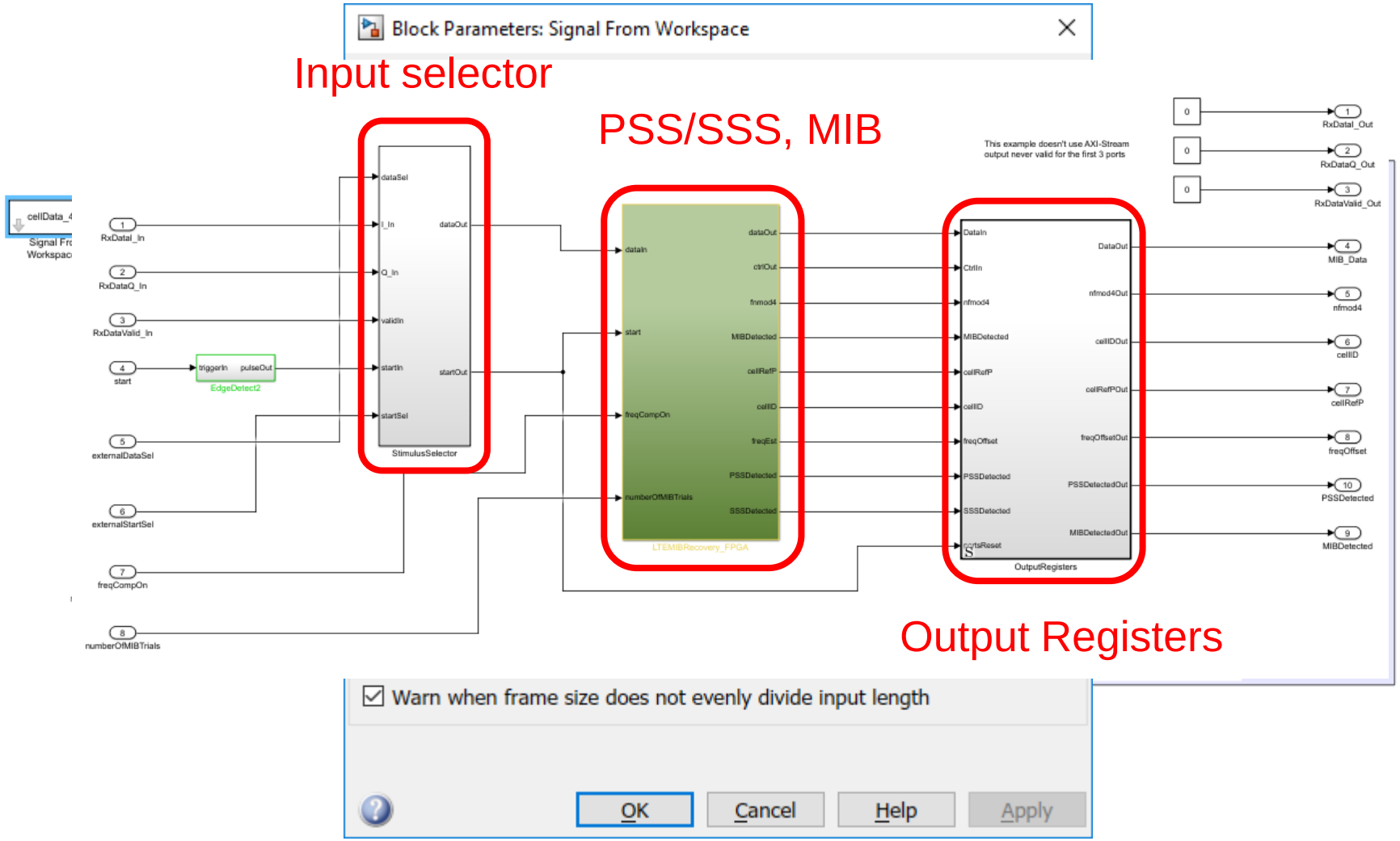
Real Time LTE Frequency Scanner



Targeting an algorithm to the FPGA and ARM

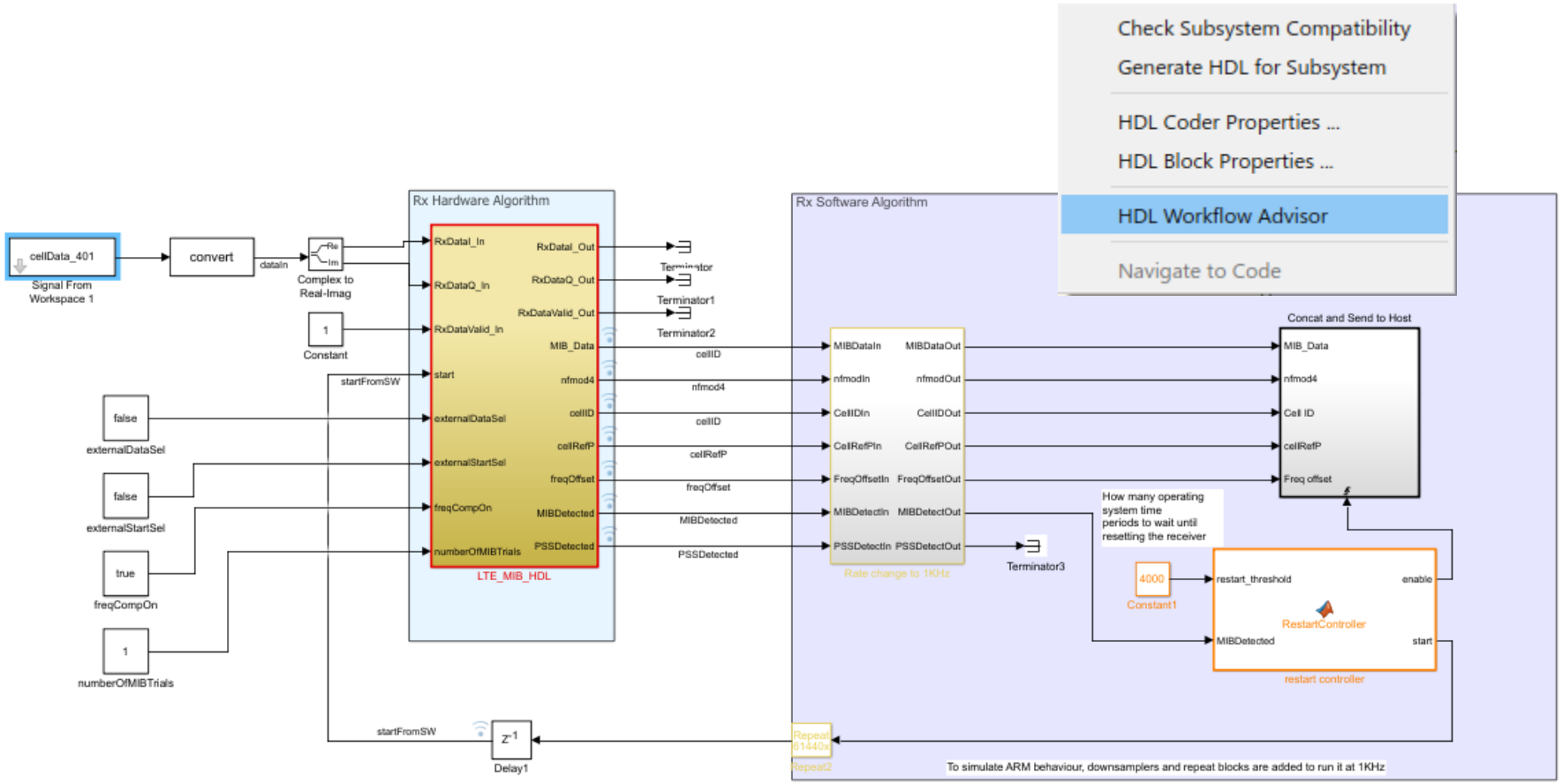


LTE Cell Scanner Example: Algorithm



- **Model Algorithm**
- Generate Bitstream
- SW Interface Model
- Run on Hardware

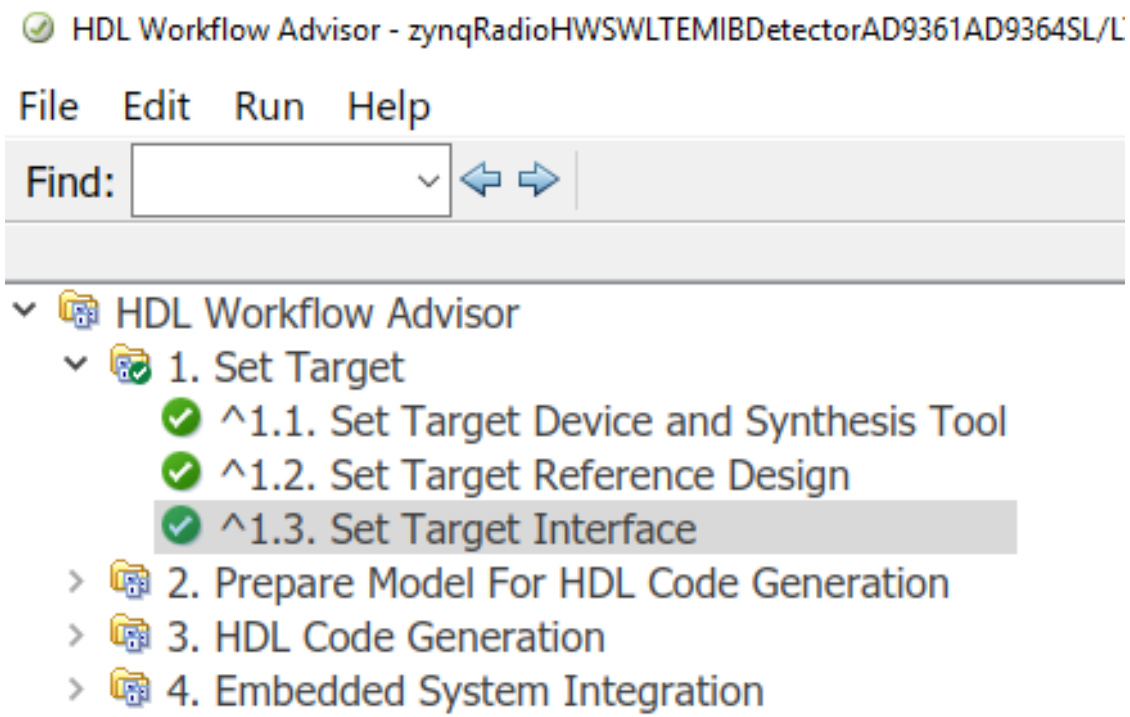
LTE Cell Scanner Example: Generation



- Model Algorithm
- **Generate Bitstream**
- SW Interface Model
- Run on Hardware

HDL Advisor

Step by Step Assistant: Set Target



1.3. Set Target Interface

Analysis (^Triggers Update Diagram)

Set target interface for HDL code generation

Input Parameters

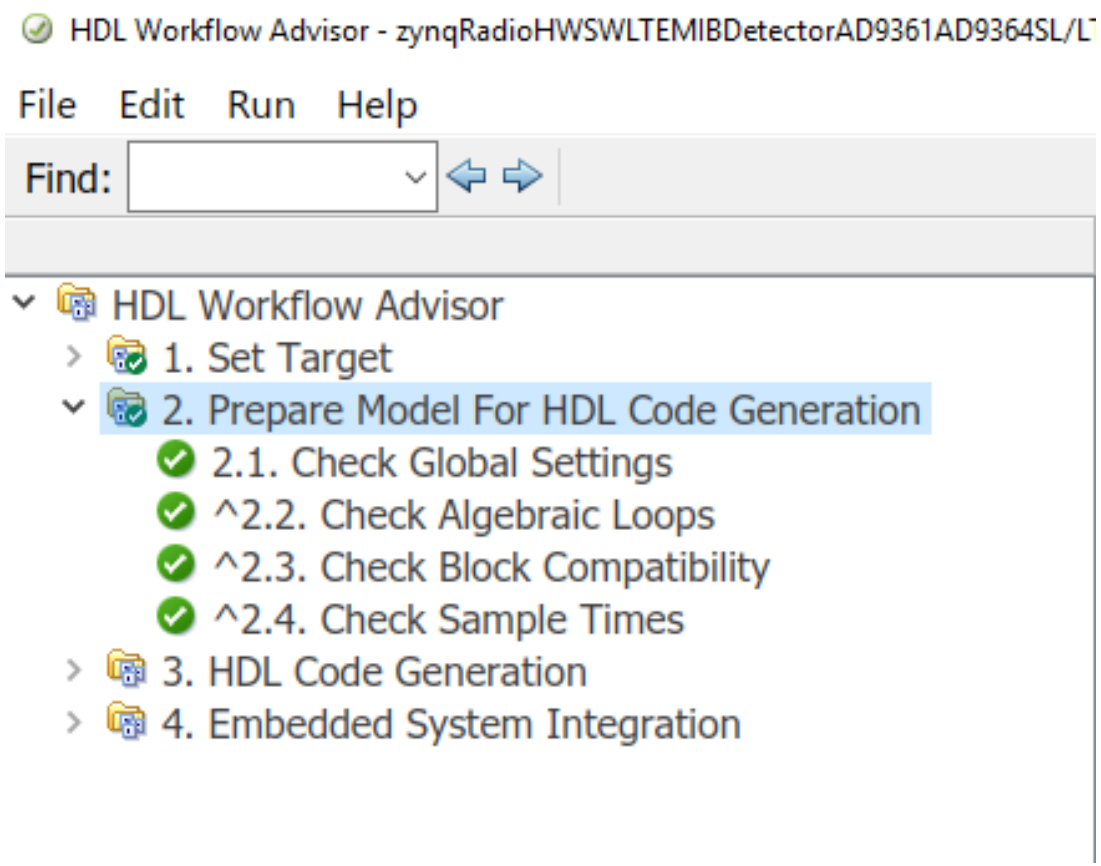
Processor/FPGA synchronization: Free running

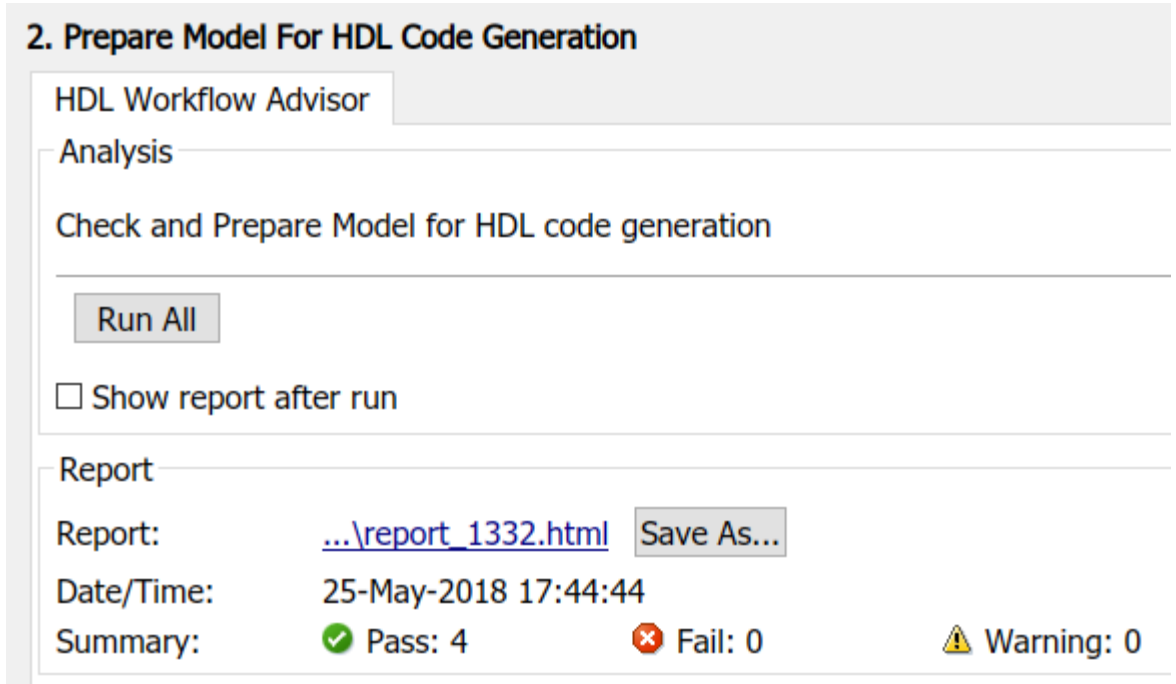
Target platform interface table

Port Name	Port Type	Data Type	Target Platform Interfaces	Bit Range
RxDataI_In	Inport	sfix16_E...	Rx data I1 In [0:15]	[0:15]
RxDataQ_In	Inport	sfix16_E...	Rx data Q1 In [0:15]	[0:15]
RxDataValid_In	Inport	boolean	Rx data Valid In	[0]
start	Inport	boolean	AXI4-Lite	x"104"
externalDataSel	Inport	boolean	AXI4-Lite	x"108"
RxDataI_Out	Outport	int16	Rx data I1 Out [0:15]	[0:15]
RxDataQ_Out	Outport	int16	Rx data Q1 Out [0:15]	[0:15]

HDL Advisor

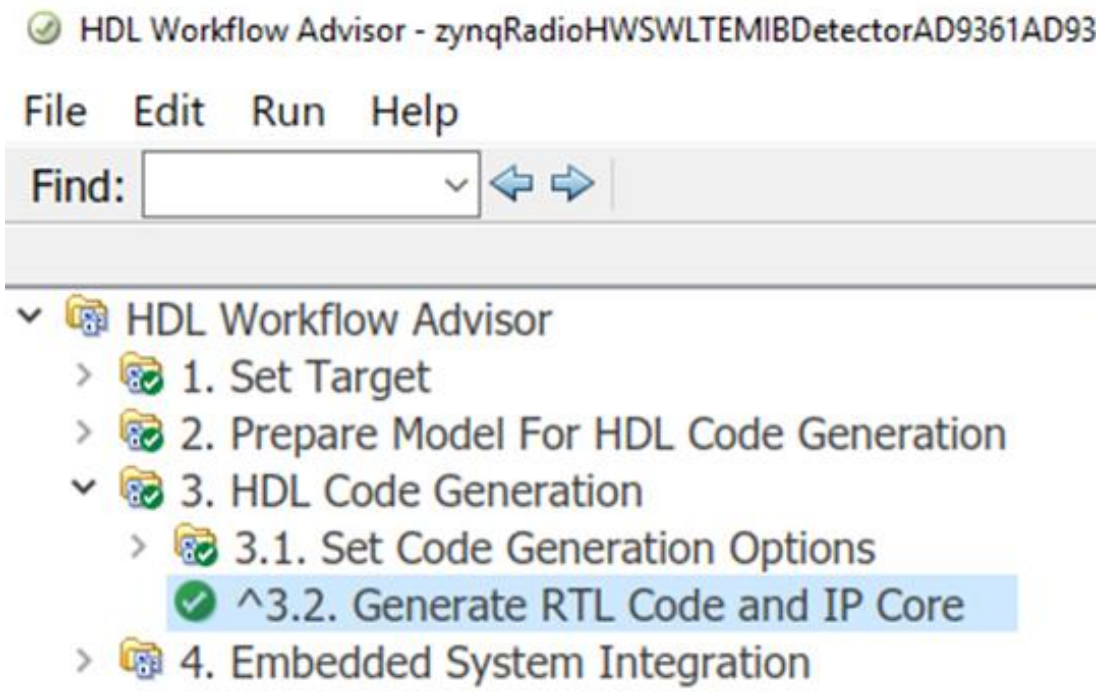
Step by Step Assistant: Check Model

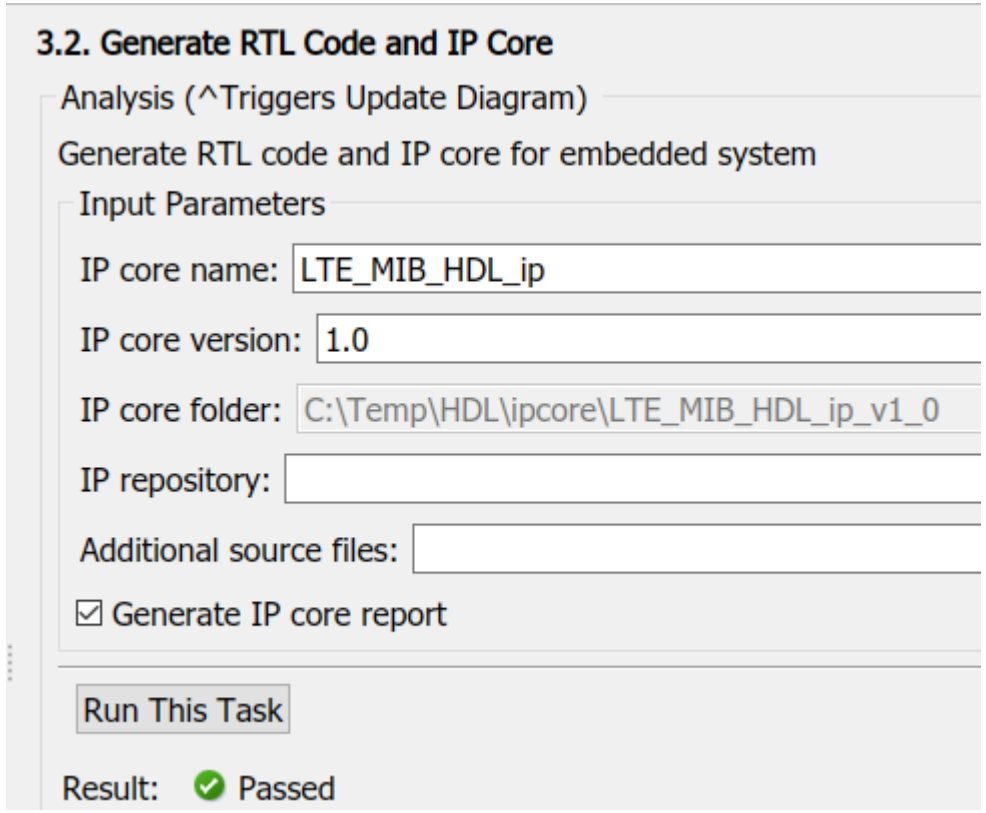




HDL Advisor

Step by Step Assistant: Generate HDL

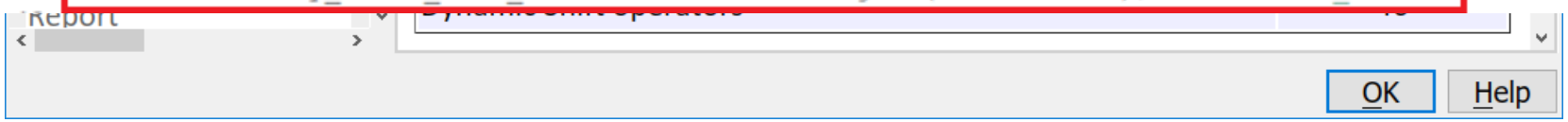




Generated HDL Code

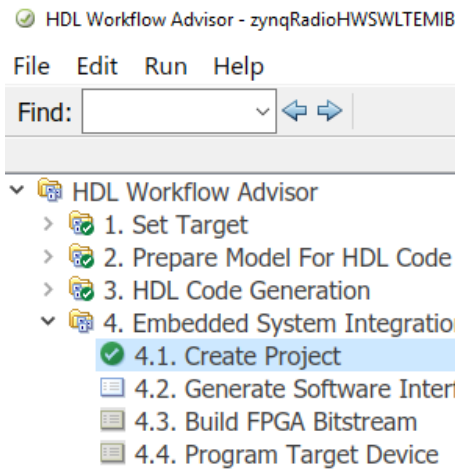
Navigating Code and Viewing Reports

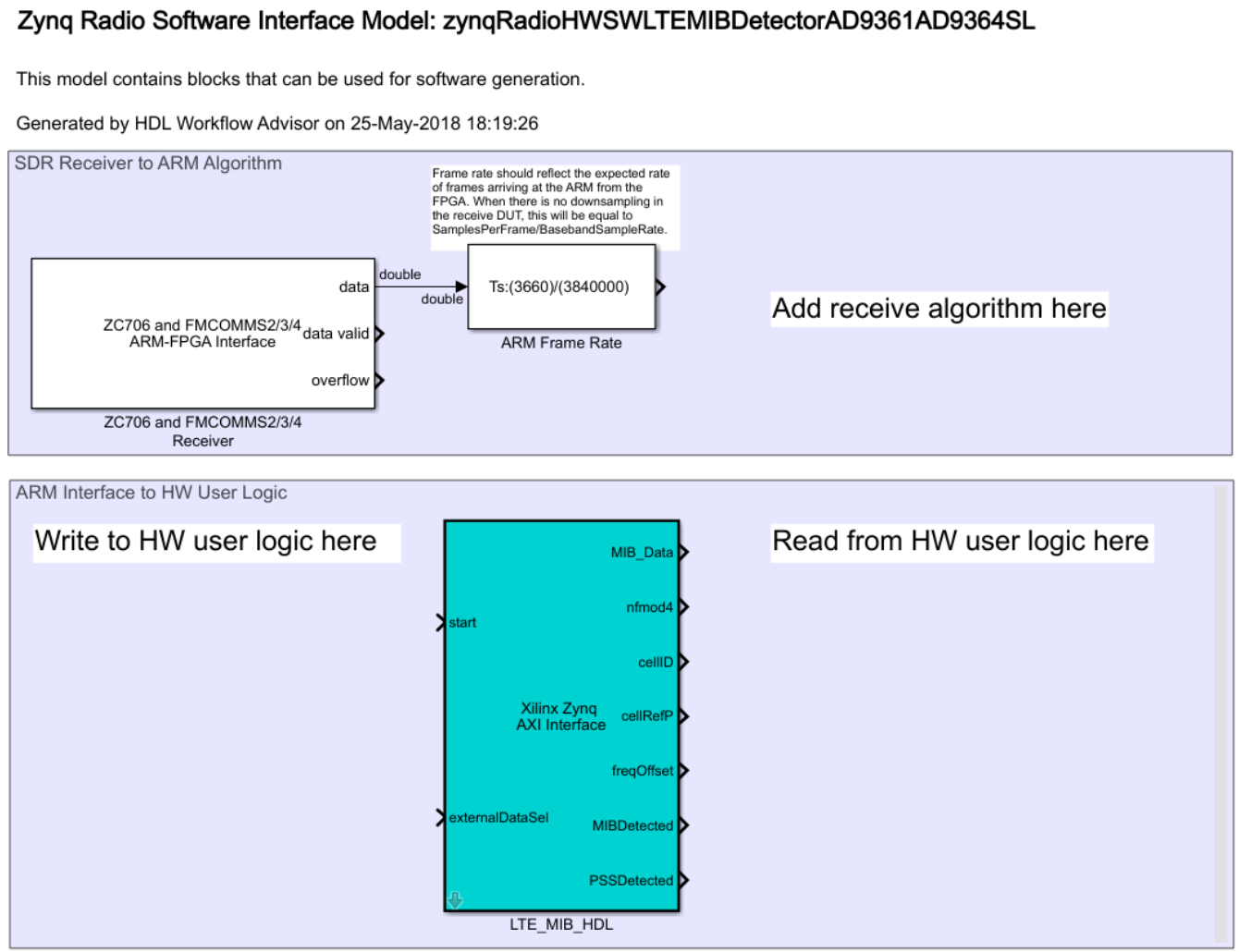
```
18  -- -------------------------------------------------------------
19  LIBRARY IEEE;
20  USE IEEE.std_logic_1164.ALL;
21  USE IEEE.numeric_std.ALL;
22
23  ENTITY LTE_MIB_HDL_ip_src_QPSK_Demod IS
24    PORT( In1_re                          :   IN    std_logic_vector(18 DOWNTO 0);  -- sfix19_En7
25          In1_im                          :   IN    std_logic_vector(18 DOWNTO 0);  -- sfix19_En7
26          bit0                            :   OUT   std_logic_vector(18 DOWNTO 0);  -- sfix19_En7
27          bit1                            :   OUT   std_logic_vector(18 DOWNTO 0)   -- sfix19_En7
28          );
29  END LTE_MIB_HDL_ip_src_QPSK_Demod;
30
31
32  ARCHITECTURE rtl OF LTE_MIB_HDL_ip_src_QPSK_Demod IS
33
34    -- Signals
35    SIGNAL In1_re_signed                  : signed(18 DOWNTO 0);  -- sfix19_En7
36    SIGNAL In1_im_signed                  : signed(18 DOWNTO 0);  -- sfix19_En7
37    SIGNAL Unary_Minus_cast               : signed(19 DOWNTO 0);  -- sfix20_En7
38    SIGNAL Unary_Minus_cast_1             : signed(19 DOWNTO 0);  -- sfix20_En7
39    SIGNAL Unary_Minus_cast_2             : signed(19 DOWNTO 0);  -- sfix20_En7
40    SIGNAL Unary_Minus_cast_3             : signed(19 DOWNTO 0);  -- sfix20_En7
41    SIGNAL Unary_Minus_out1_re            : signed(18 DOWNTO 0);  -- sfix19_En7
42    SIGNAL Unary_Minus_out1_im            : signed(18 DOWNTO 0);  -- sfix19_En7
```



HDL Advisor

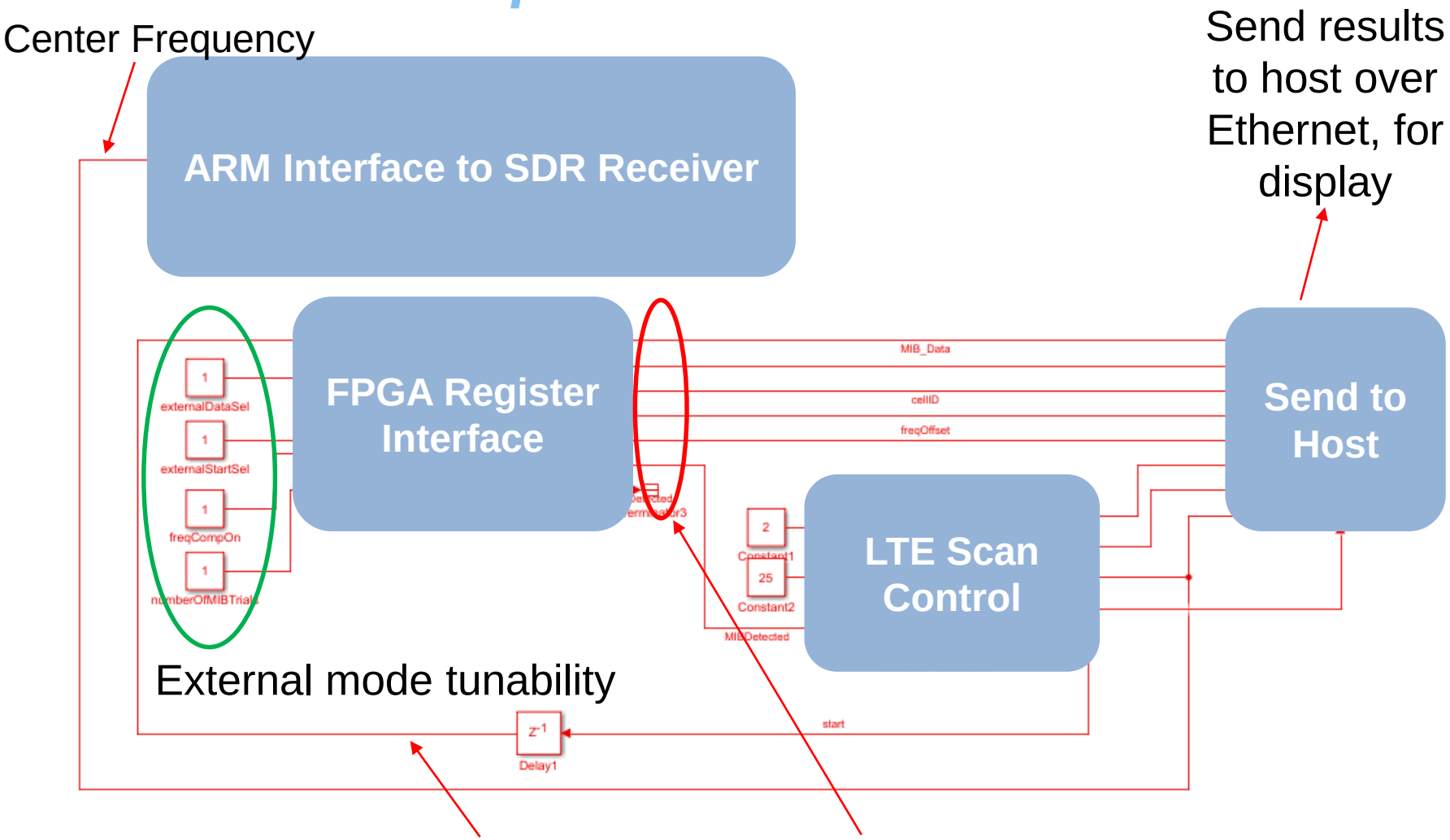
Step by Step Assistant: SW Model & Bitstream





Software Interface

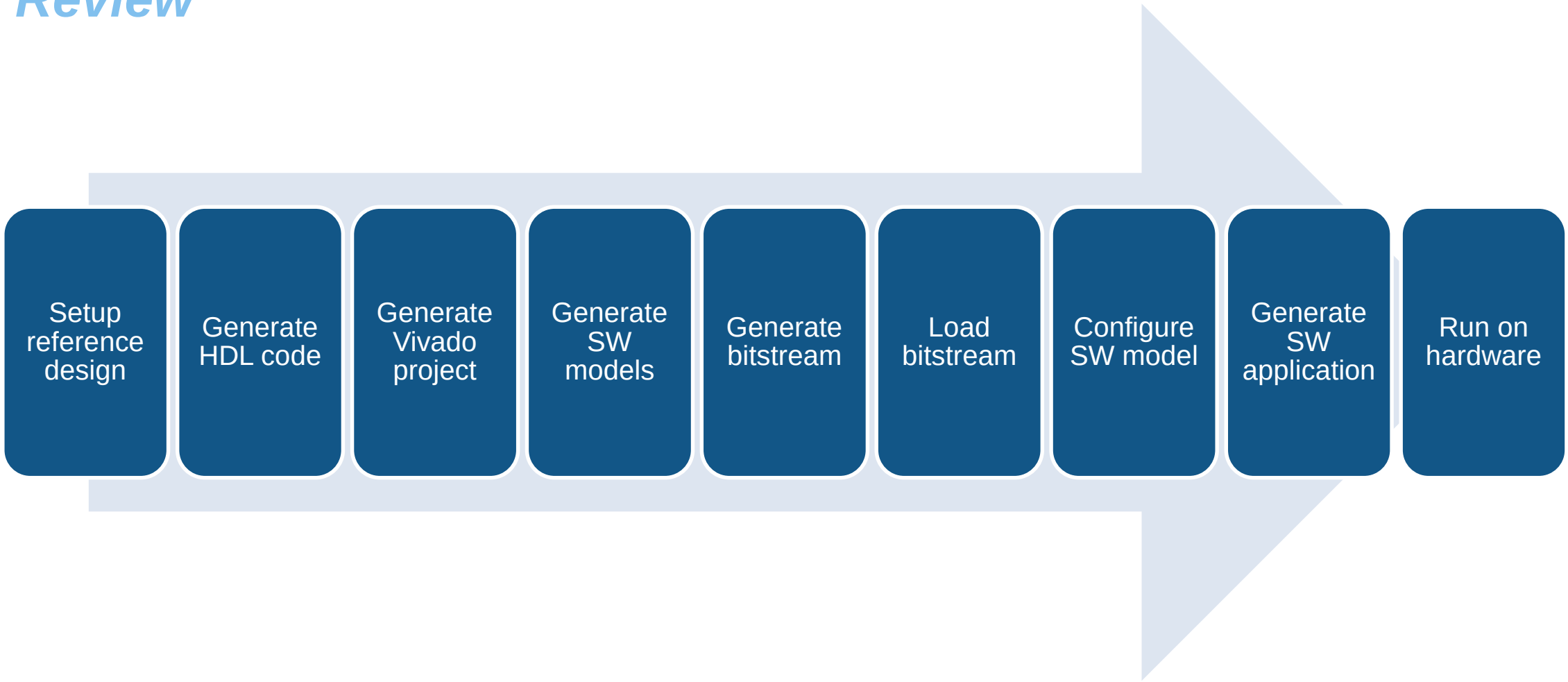
Runs on ARM processor



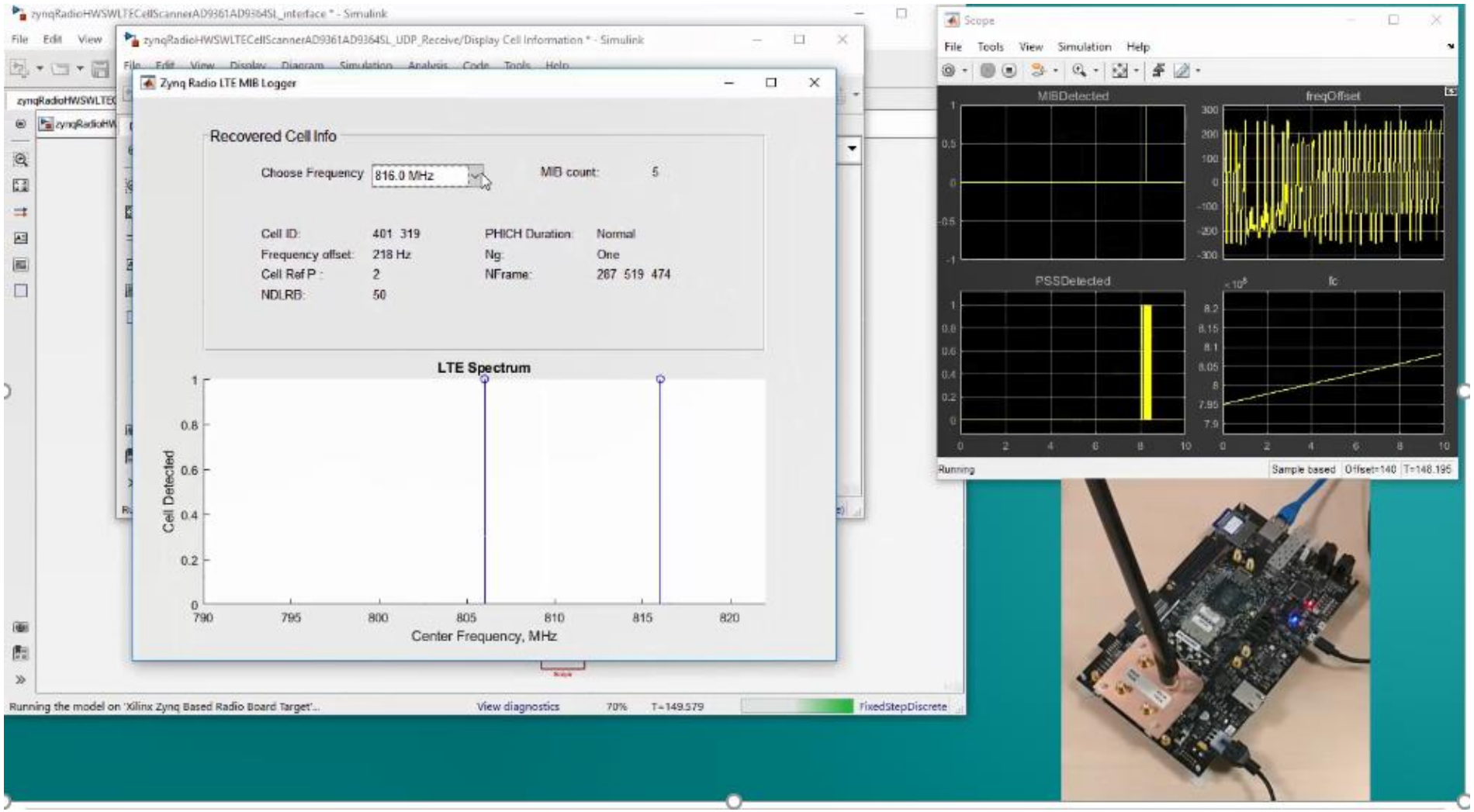
- Model Algorithm
- Generate Bitstream
- **SW Interface Model**
- Run on Hardware

Targeting Workflow

Review

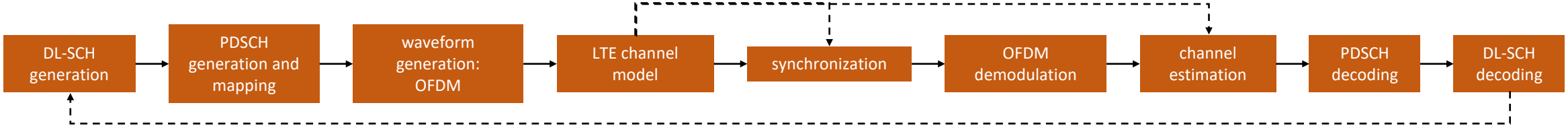


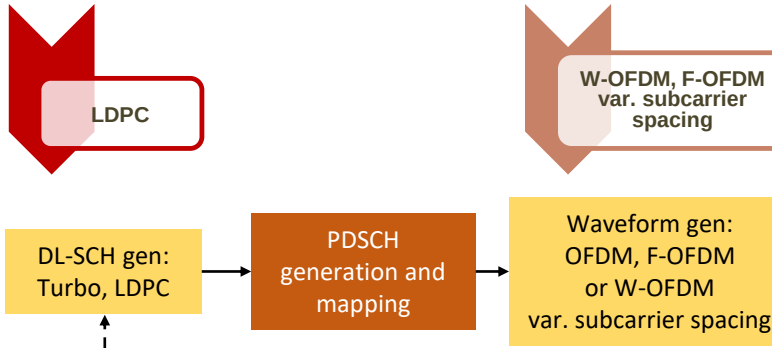
Run on Hardware

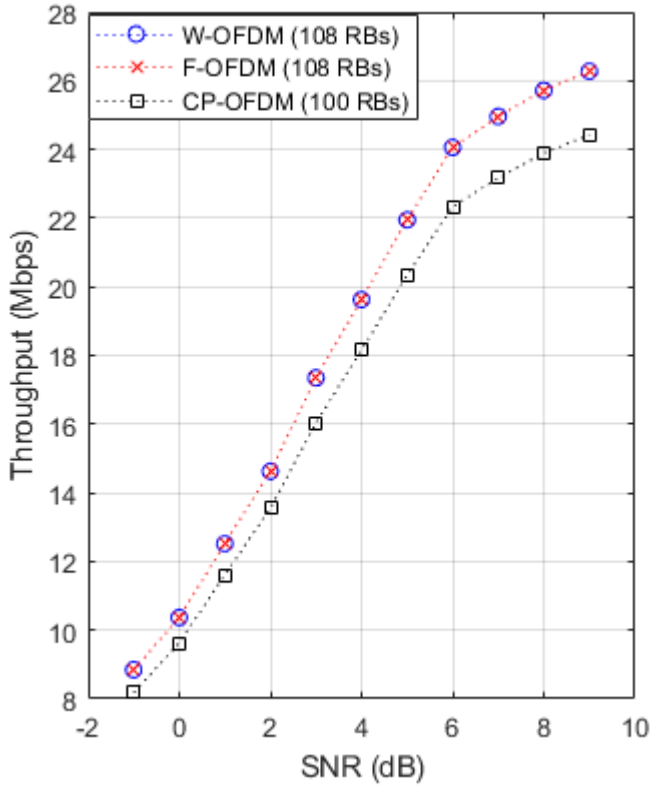


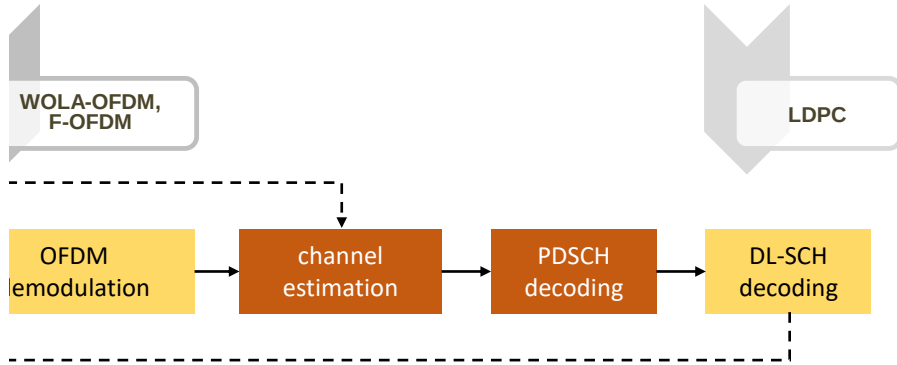
Extending Standards

LTE to 5G



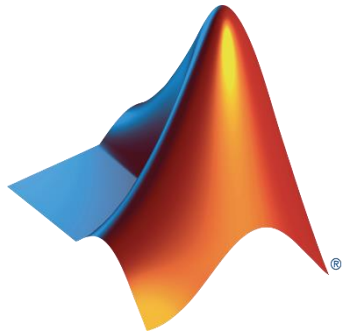






Conclusions

- **Wireless Designs starts with MATLAB**
  - Prove algorithm and design with **simulation** and **over-the-air signals**
  - Generate customizable waveforms to verify conformance to the latest **5G, LTE, and WLAN standards**
  - **Automatically generate HDL or C** code for prototyping and implementation without hand-coding



Thank you!