

AUTOMATED INTEGRATION OF SIMULINK MODELS INTO VIRTUAL PLATFORMS

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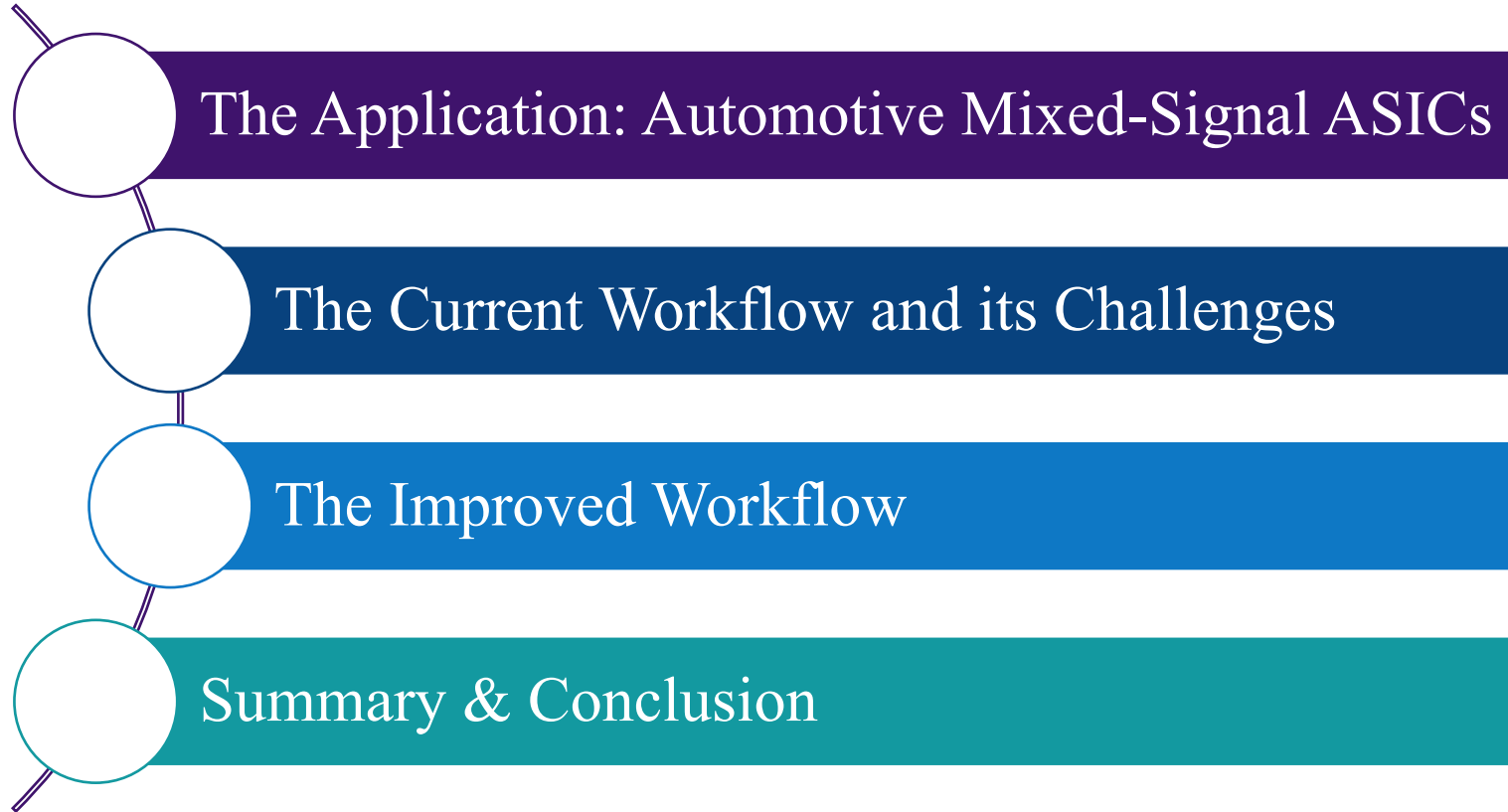
MATLAB EXPO
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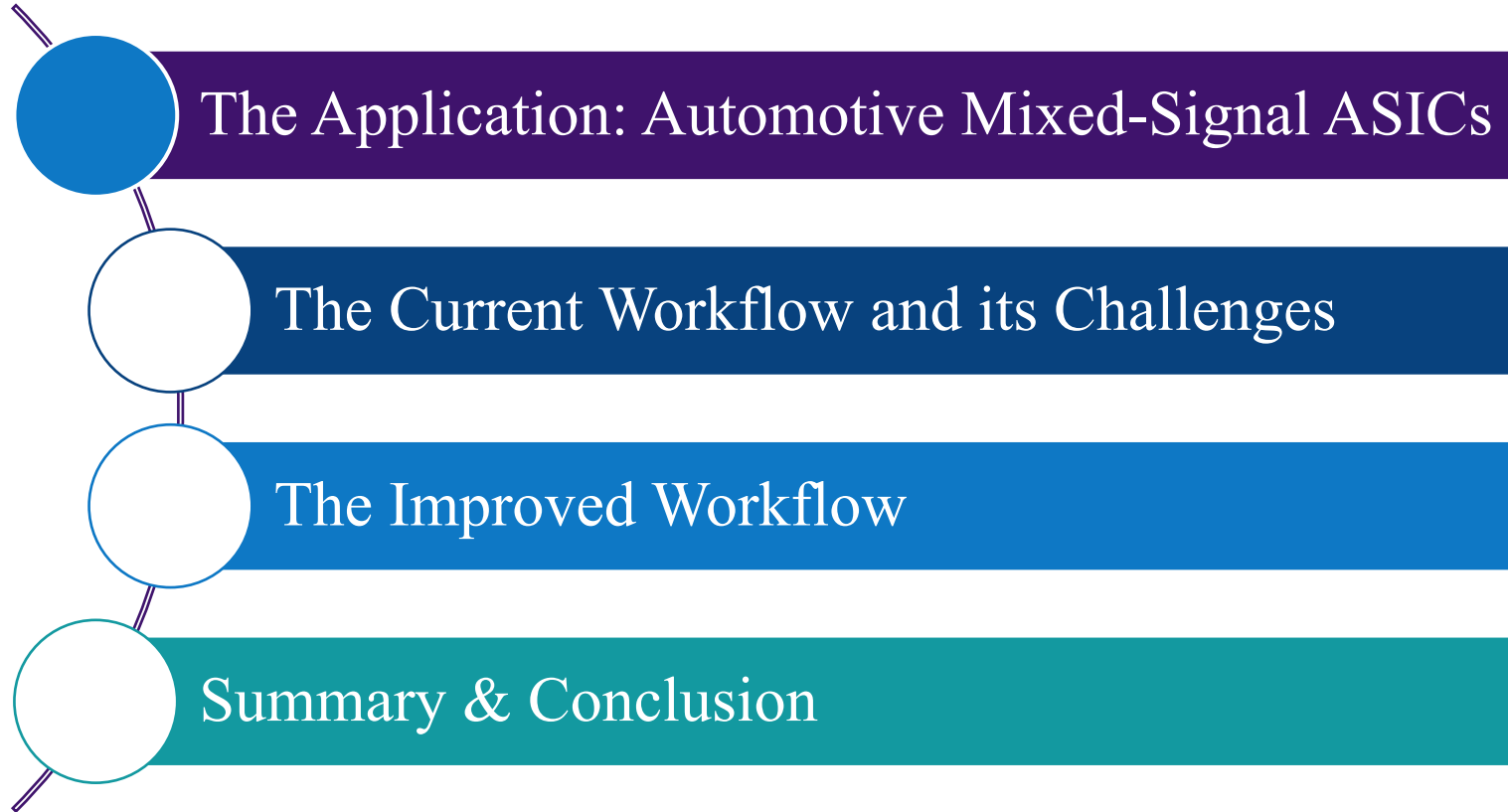
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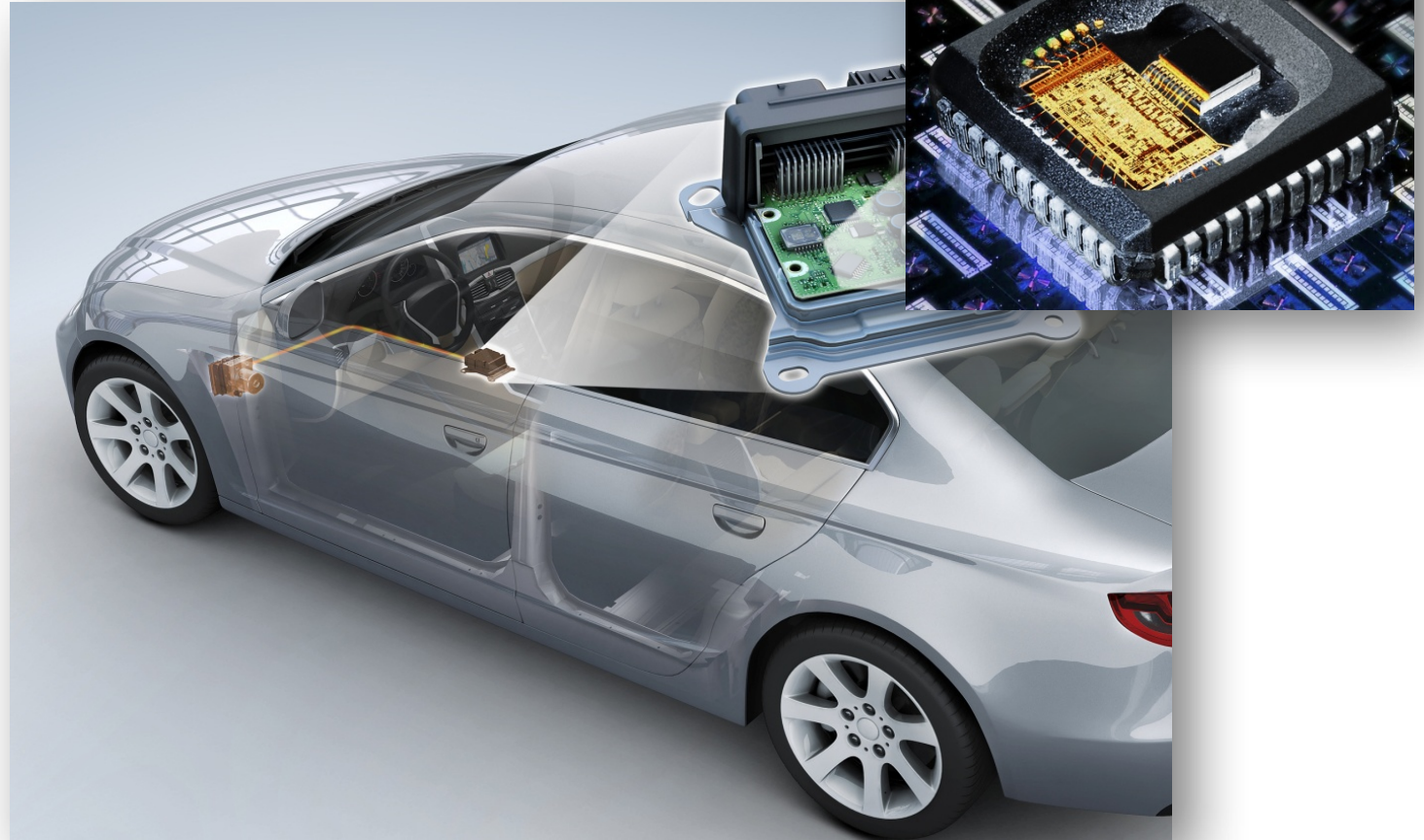
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Integration of Simulink Models into Virtual Platforms

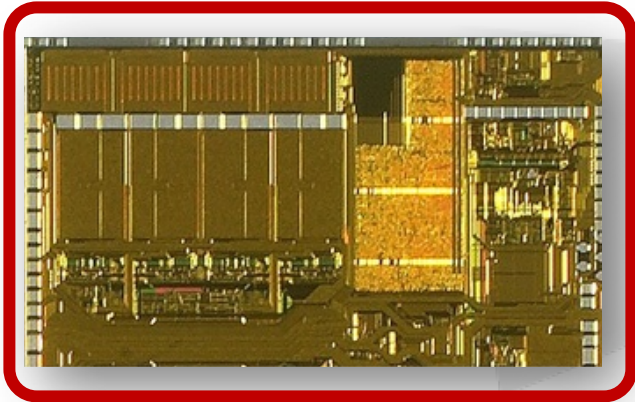
Automotive Mixed-Signal ASICs

- ▶ Bosch accelerates progress of automotive technology with continued innovations like ESP or autonomous driving solutions
- ▶ Integral part for these solutions are automotive sensors
- ▶ Example: Inertial sensor system for ESP

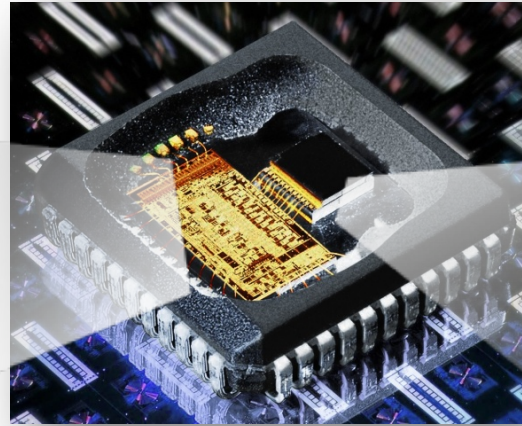


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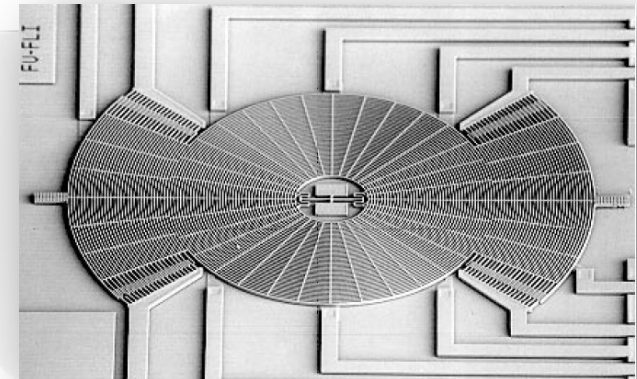
Automotive Mixed-Signal ASICs



- ▶ Heterogeneous SoC:
 - ▶ Analog Hardware
 - ▶ Digital Non-Programmable Hardware
 - ▶ Processors



- ▶ System-in-Package (SiP)



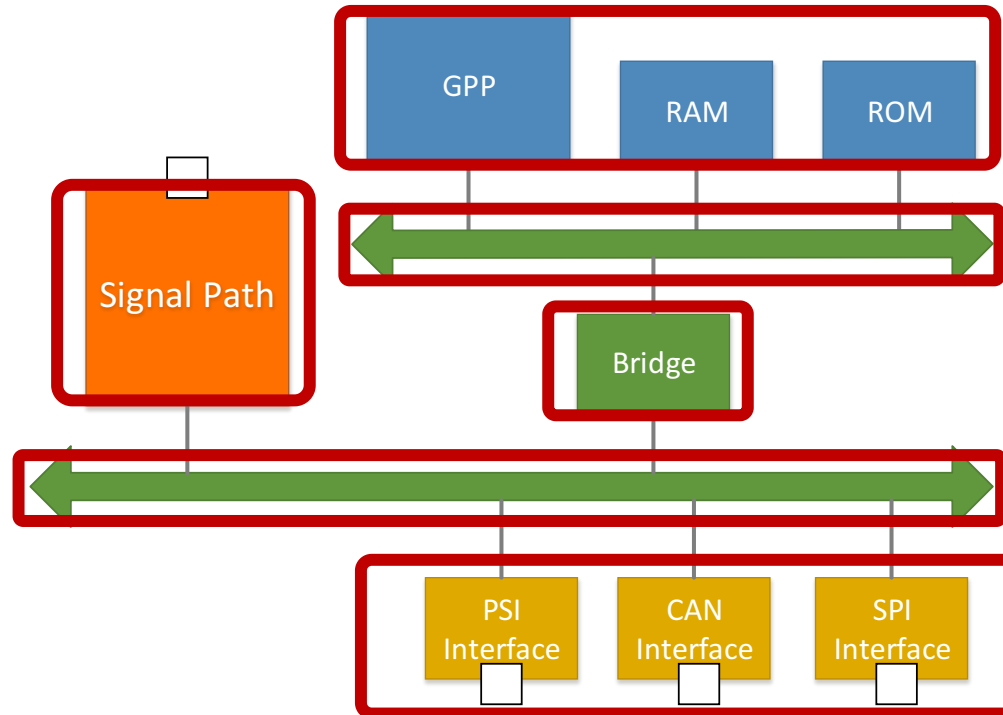
Source: Karsten Funk

- ▶ Sensor

Integration of Simulink Models into Virtual Platforms

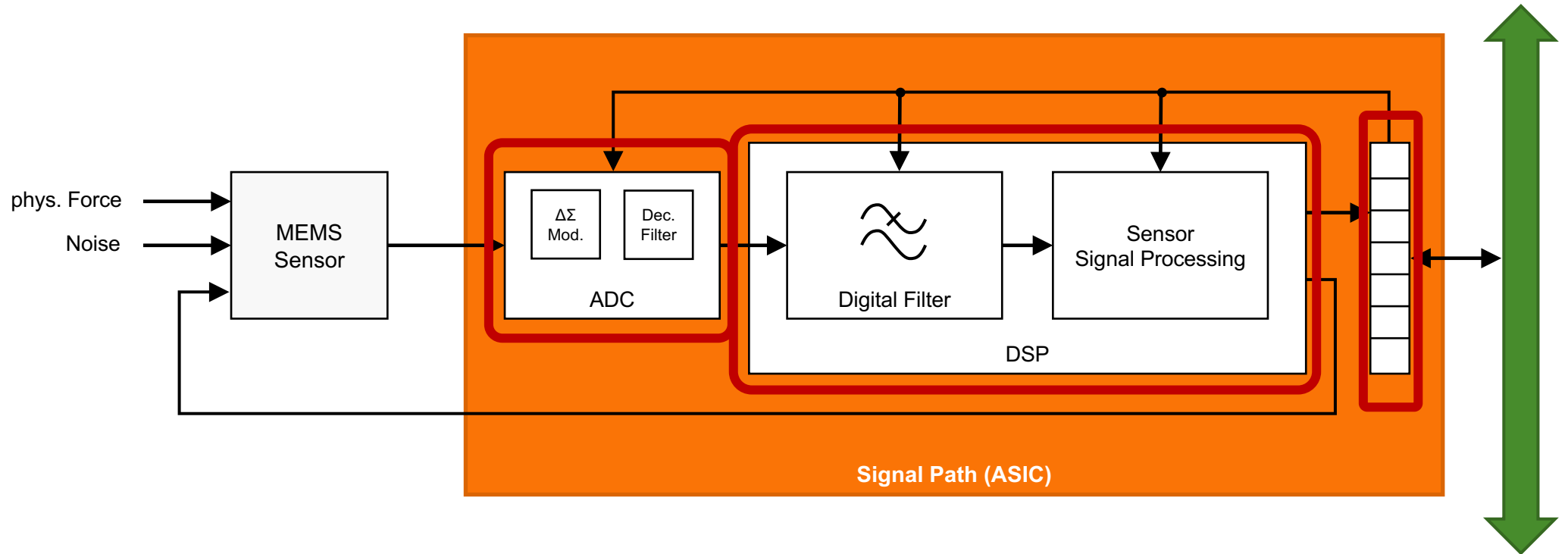
Sensor ASIC – Architecture Example

- ▶ Signal path for sensor signal processing
- ▶ General Purpose Processor (GPP) subsystem for
 - ▶ safety monitoring
 - ▶ communication protocols
 - ▶ etc.
- ▶ Several interfaces
- ▶ On-Chip Architecture

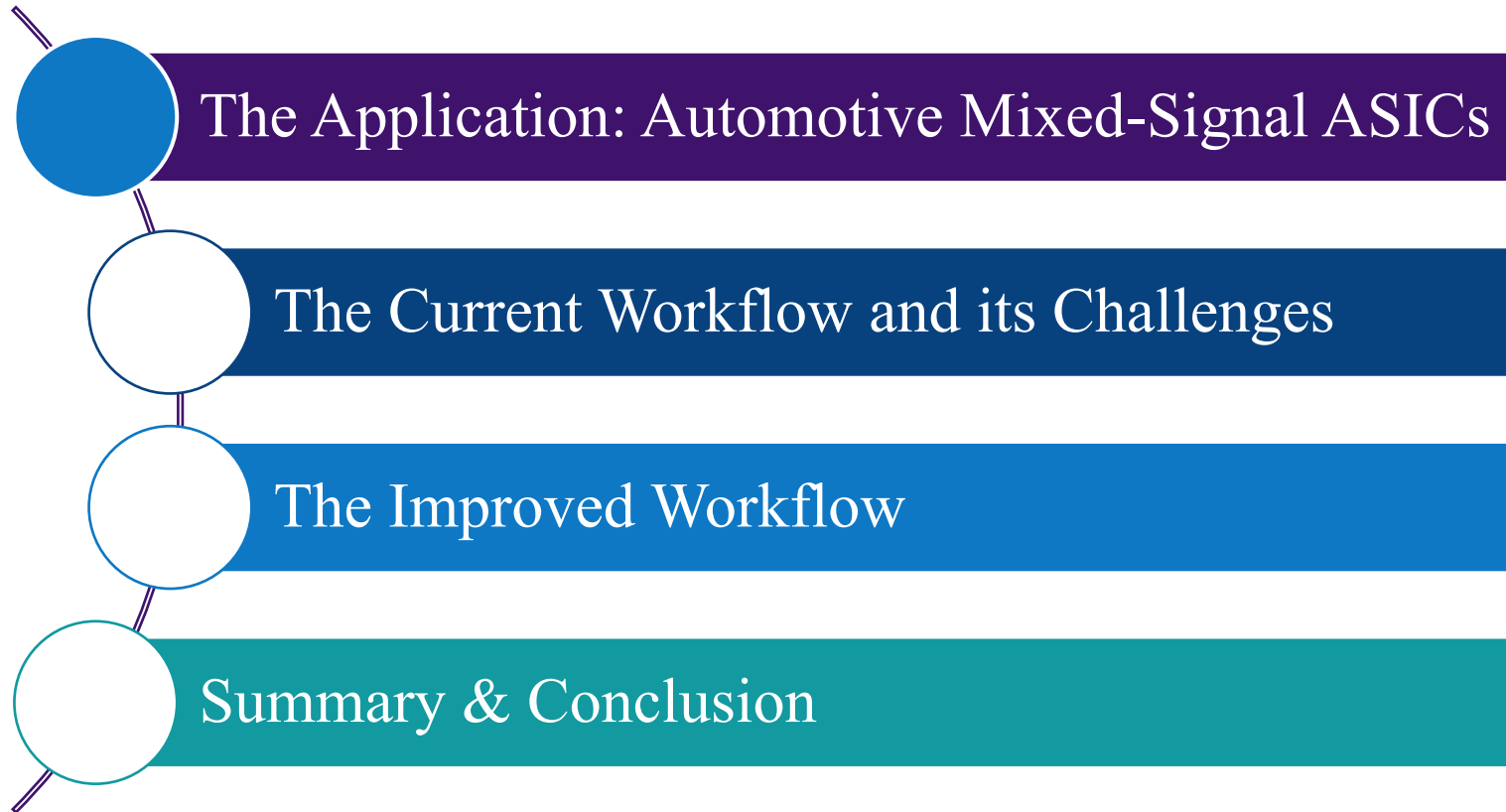


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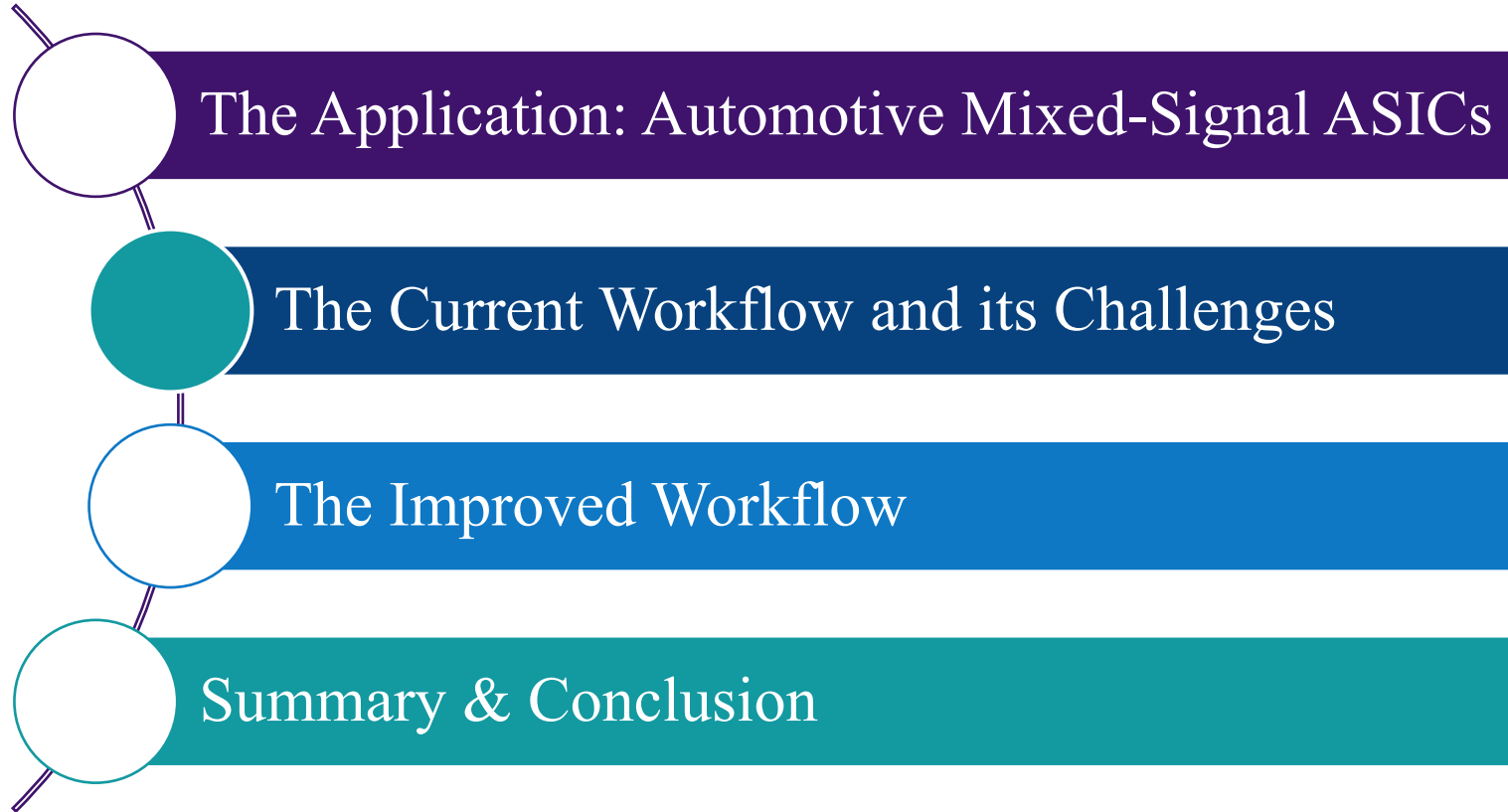
Sensor ASIC – Signal Path Example



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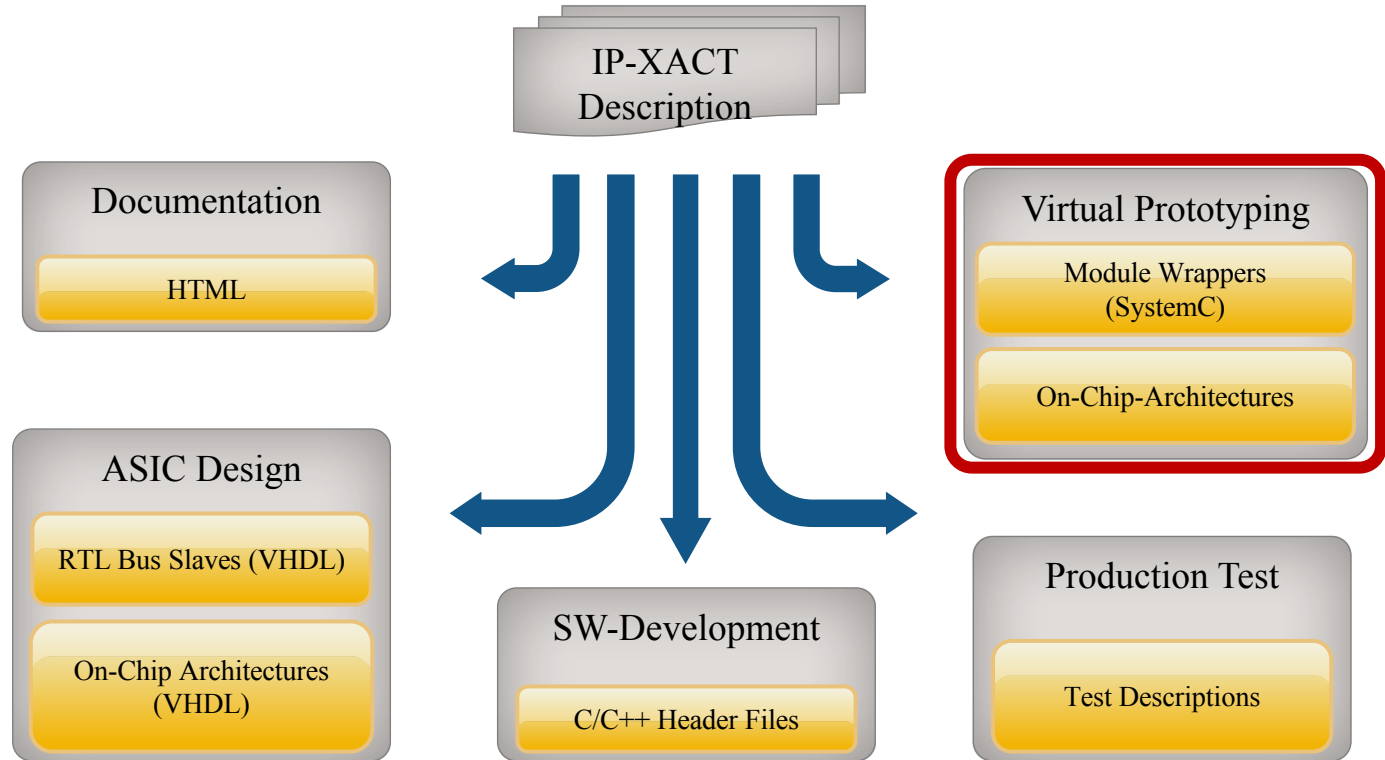
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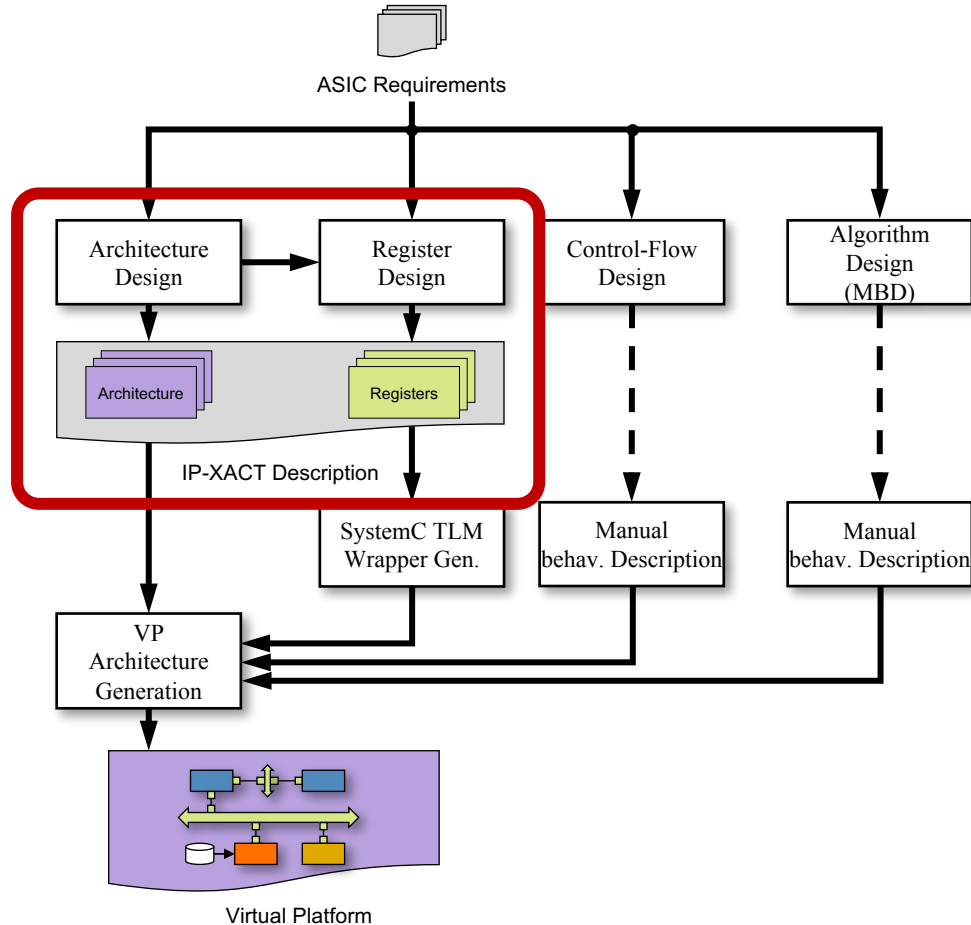
Current Workflow - IP-XACT-Centric Tool Environment

- ▶ IP-XACT description as single source
- ▶ Generation of various design, test and documentation outputs
- ▶ Ensures consistency throughout the whole design flow



Integration of Simulink Models into Virtual Platforms

Current Workflow - IP-XACT-Centric VP Generation

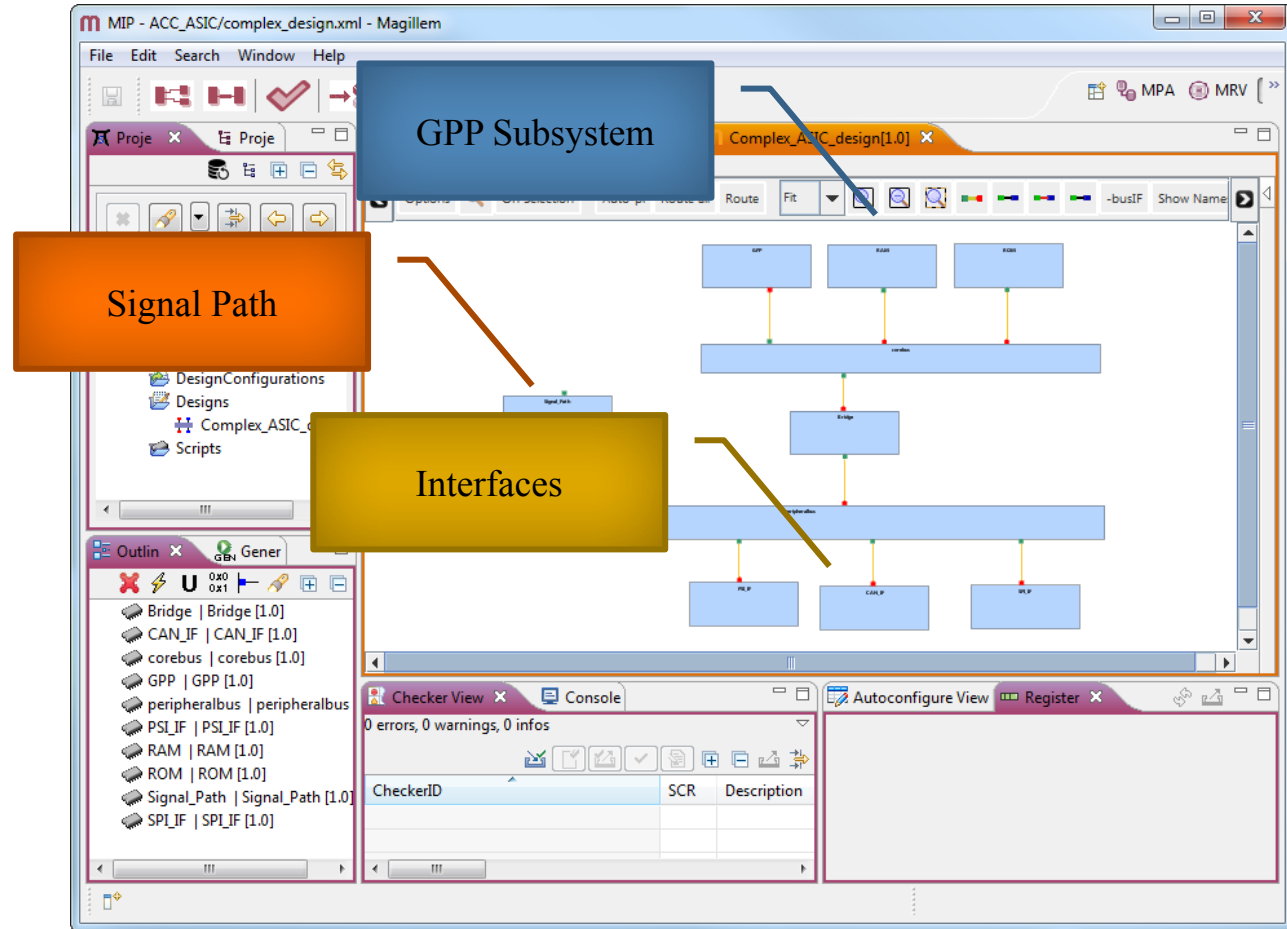


- Description of architecture and register interfaces in IP-XACT
- Automated generation of VP architectures and TLM register interfaces
- Signal processing algorithm design using Model-Based Design
- Manual behavioural description of control- and signal-flow oriented designs

Integration of Simulink Models into Virtual Platforms

Architecture Design - Magillem[®] IP-XACT Packager (MIP)

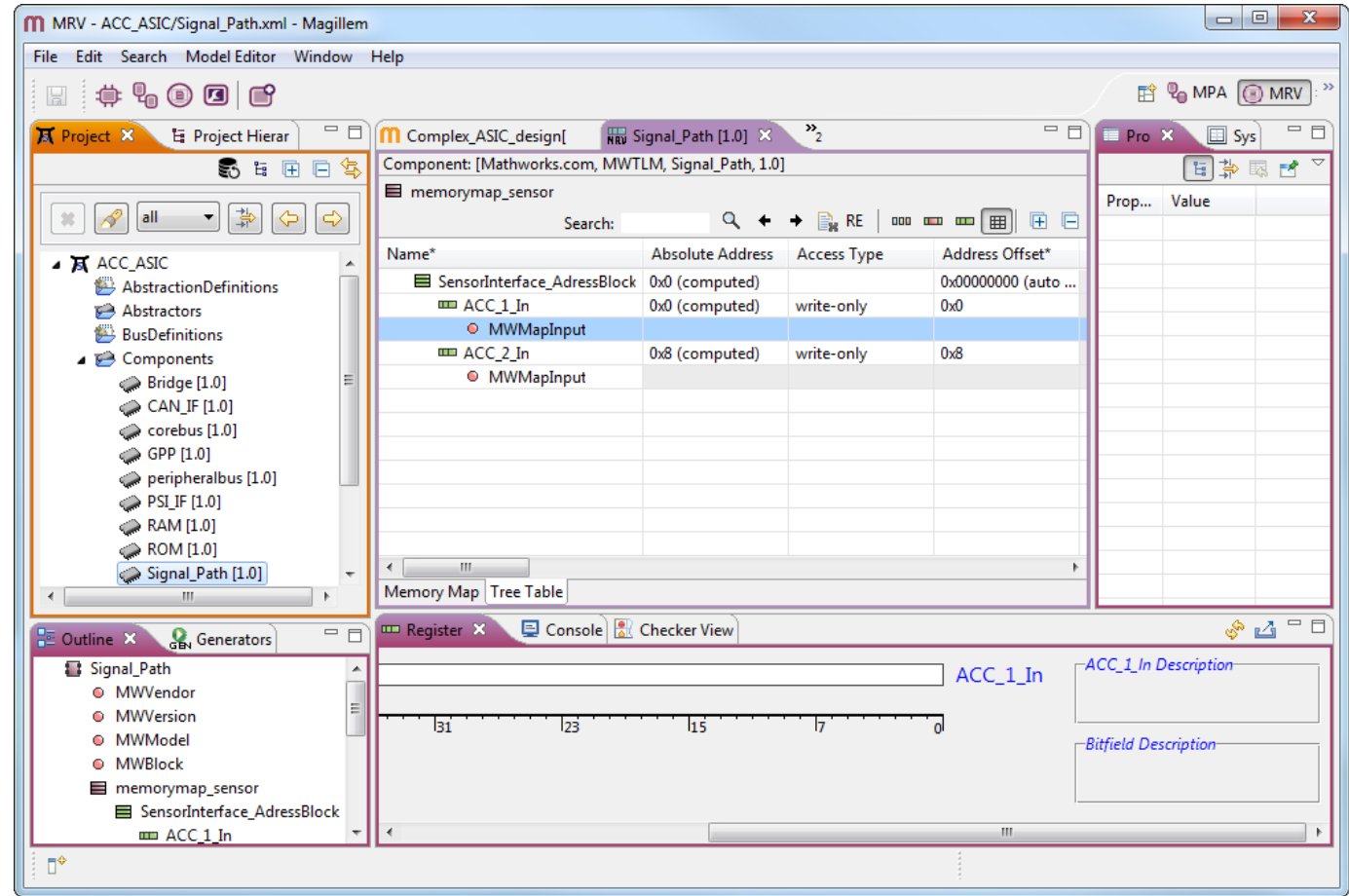
- Design of On-Chip Architecture in Magillem[®] IP-XACT Packager
- Saved as IP-XACT Design description



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Register Interface Design - Magillem[®] Register View (MRV)

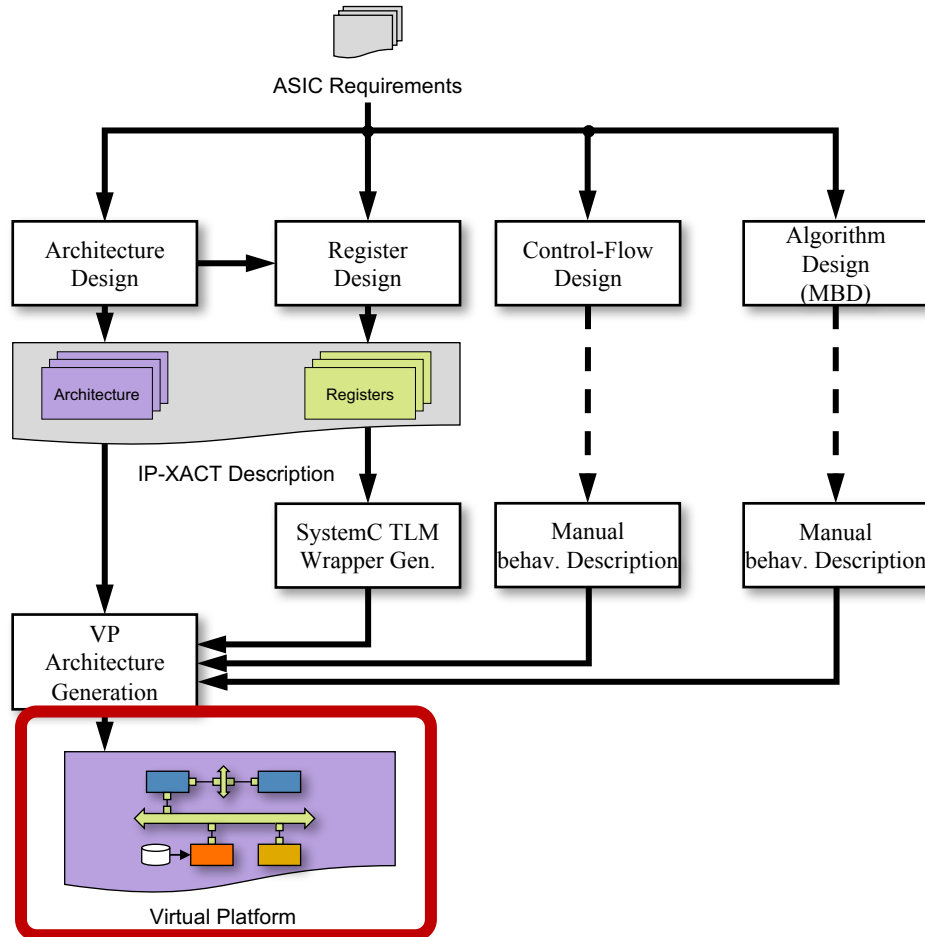
- Design of register interfaces in Magillem[®] Register View
- Saved as IP-XACT Component description



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Current Workflow - IP-XACT-Centric VP Generation

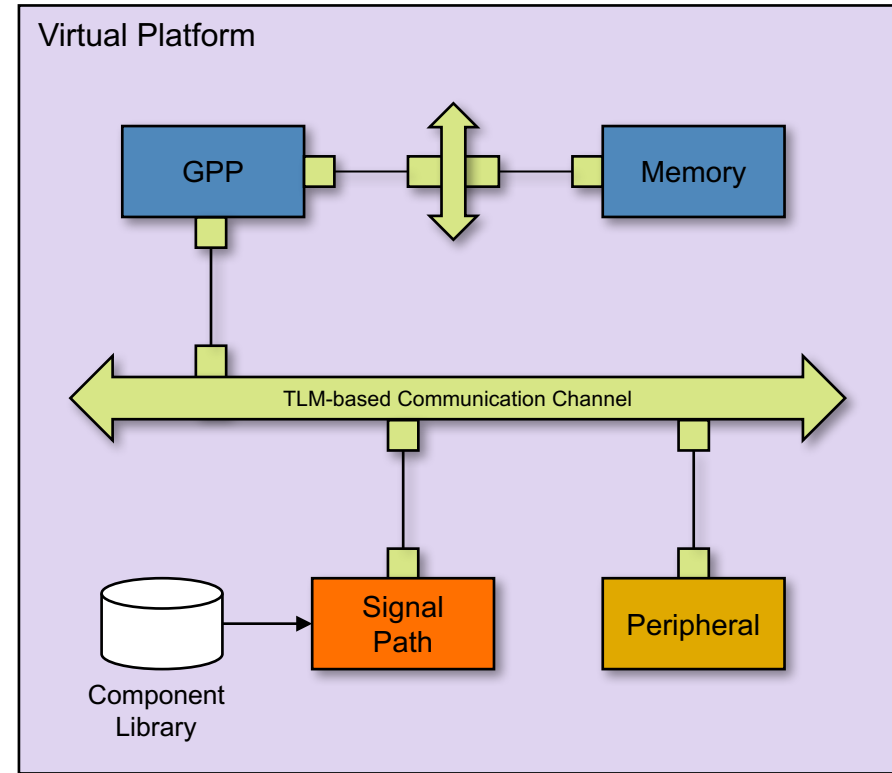
- Automated generation of VP architectures and TLM register interfaces



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Virtual Platforms (VP)

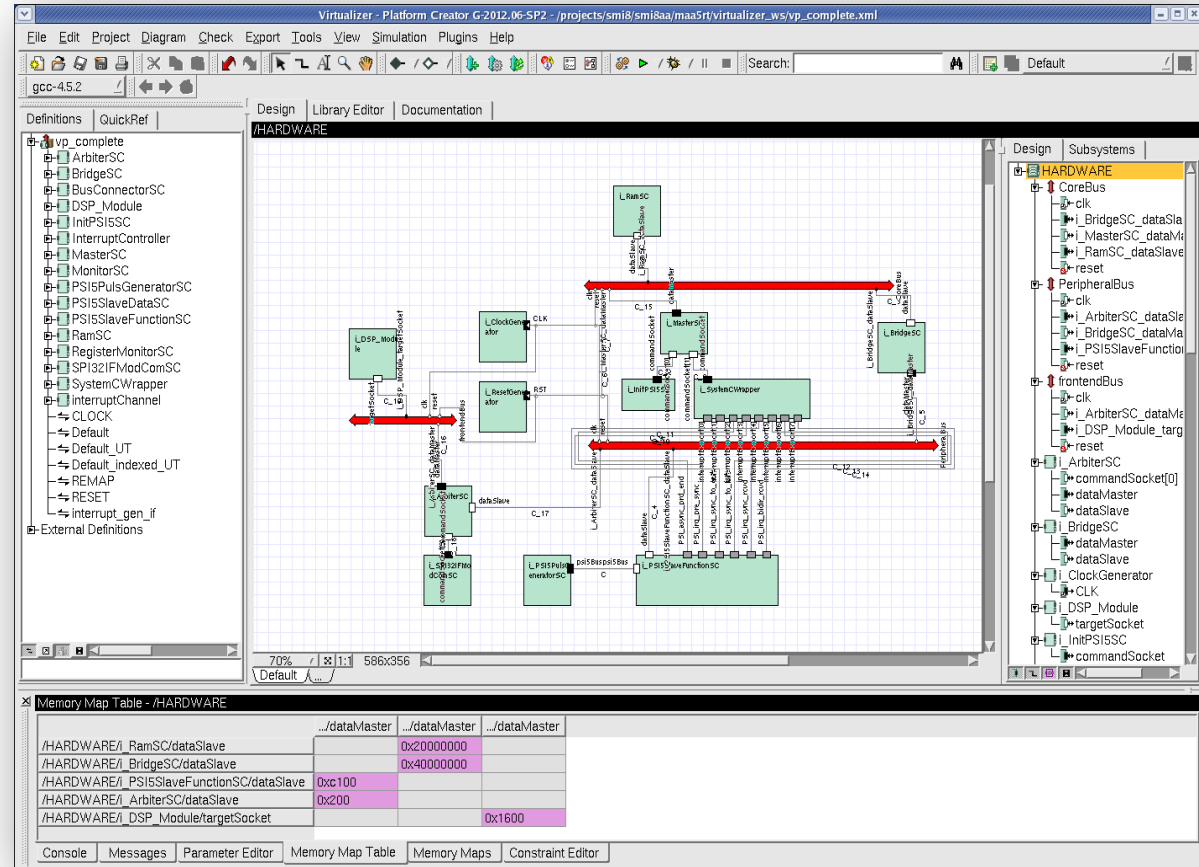
- ▶ SoC architecture-centric
- ▶ Highspeed pre-silicon development environment
- ▶ Abstracting communication interfaces through Transaction Level Modelling (TLM)
- ▶ Benefits
 - ▶ SoC concept validation and architectural exploration
 - ▶ Concurrent SW and HW development
 - ▶ Validation of HW/SW interfaces
 - ▶ Optimization of SW



Integration of Simulink Models into Virtual Platforms

System Simulation and SW Dev. in Synopsys® Virtualizer™

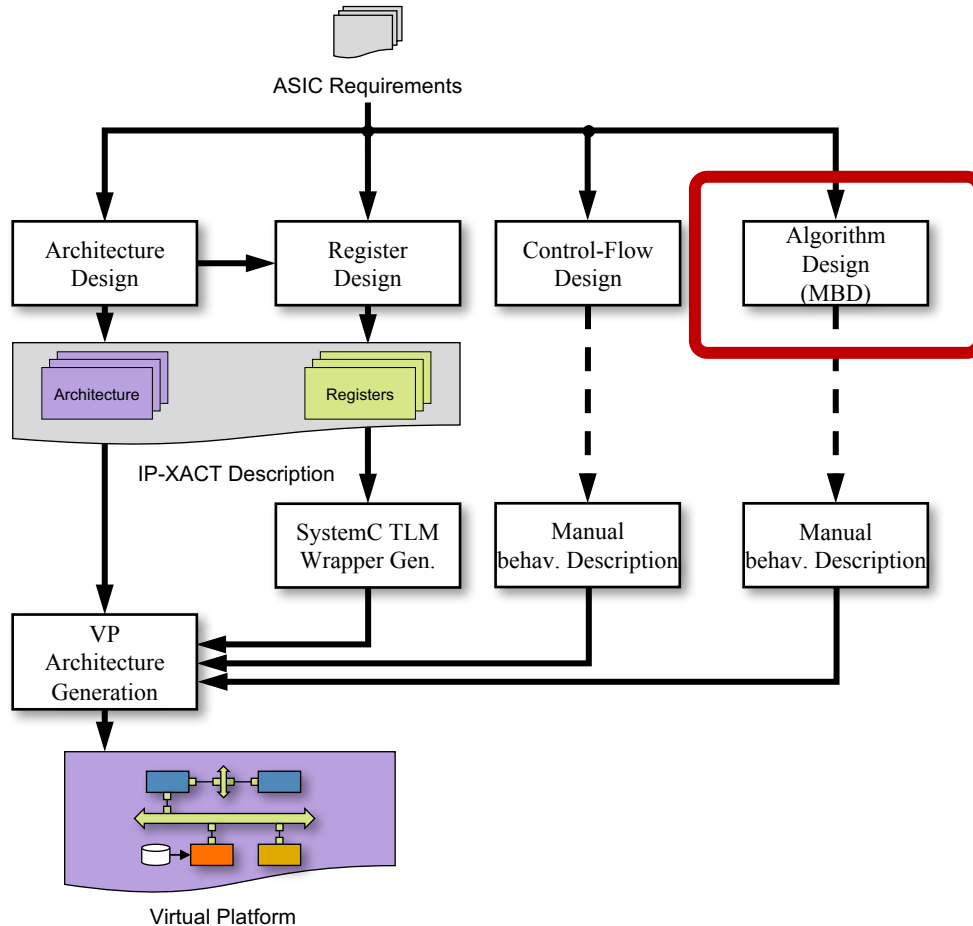
- ▶ Tool for construction and simulation of Virtual Prototypes
- ▶ Large module library
- ▶ Comprehensive debugging capabilities
- ▶ Export of development kits for SW development



Integration of Simulink Models into Virtual Platforms

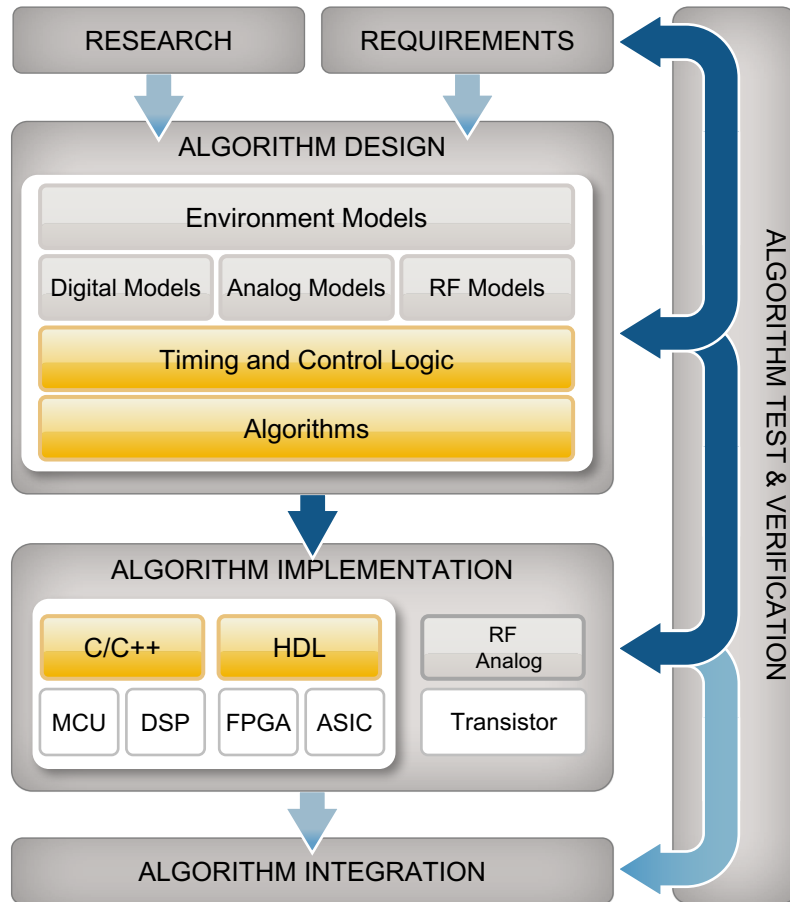
Current Workflow - IP-XACT-Centric VP Generation

- Signal processing algorithm design using Model-Based Design



Integration of Simulink Models into Virtual Platforms

Model-Based Design (MBD)



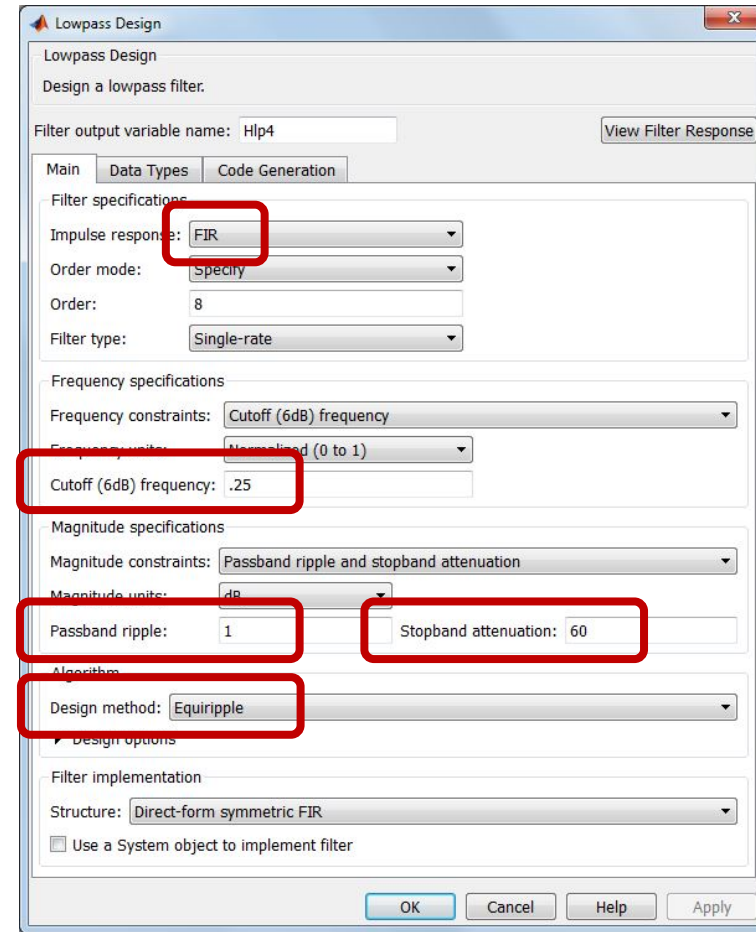
- ▶ Algorithm-centric
- ▶ Signal flow-oriented multi-domain simulation
 - ▶ Differential equation, transfer function, physical network level
 - ▶ Time-continuous, time-discrete
 - ▶ Value-continuous, value-discrete
- ▶ Benefits
 - ▶ Mathematical algorithm design
 - ▶ Early verification of its functional correctness and performance in its environment
 - ▶ Implementation through automatic code generation

Integration of Simulink Models into Virtual Platforms

Example: Lowpass Filter Design with DSP System Toolbox™

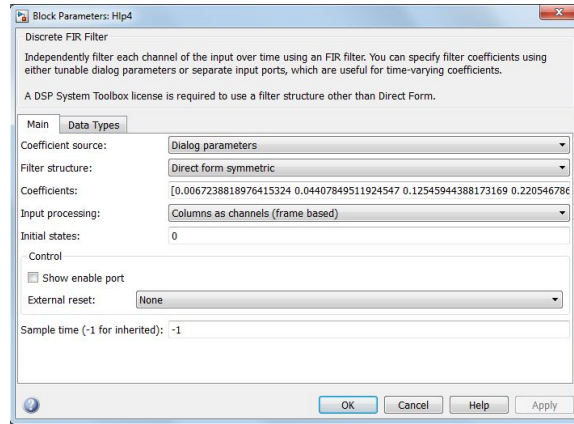
Specification:

- Filter response: FIR
- Design Method: Equiripple
- 6dB-cutoff frequency: 0.25
- Stopband attenuation: 60 dB
- Passband ripple: 1 dB

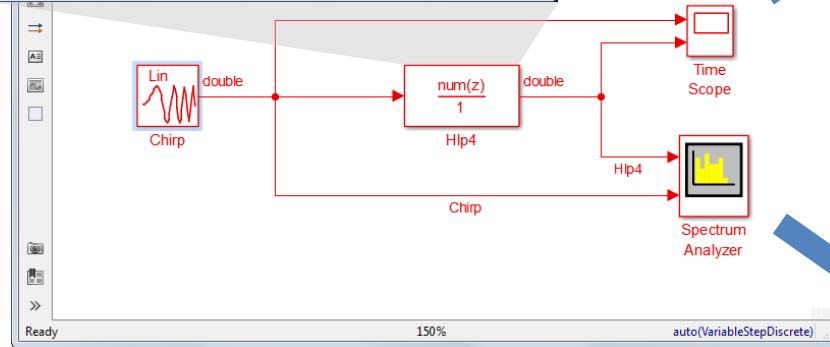
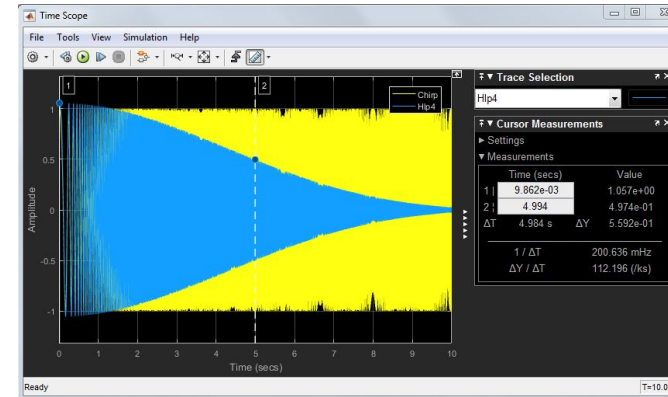


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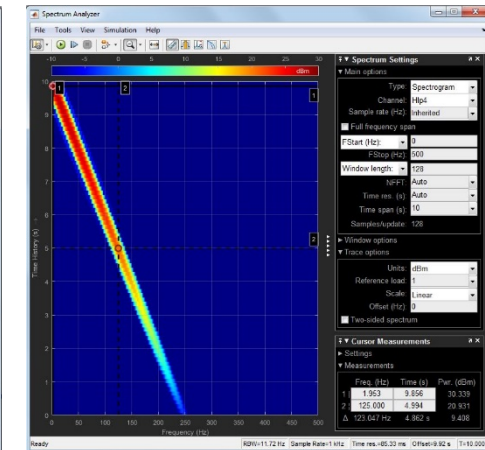
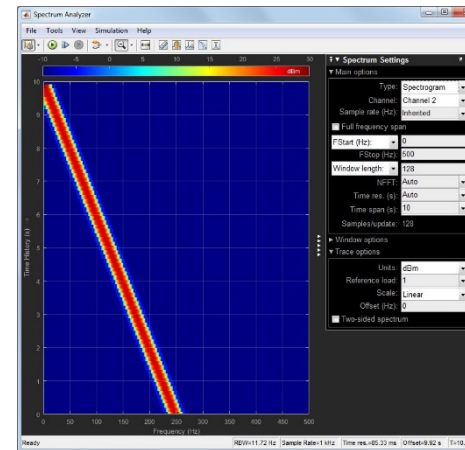
Signal-Flow-based Simulation with Simulink®



Time domain:

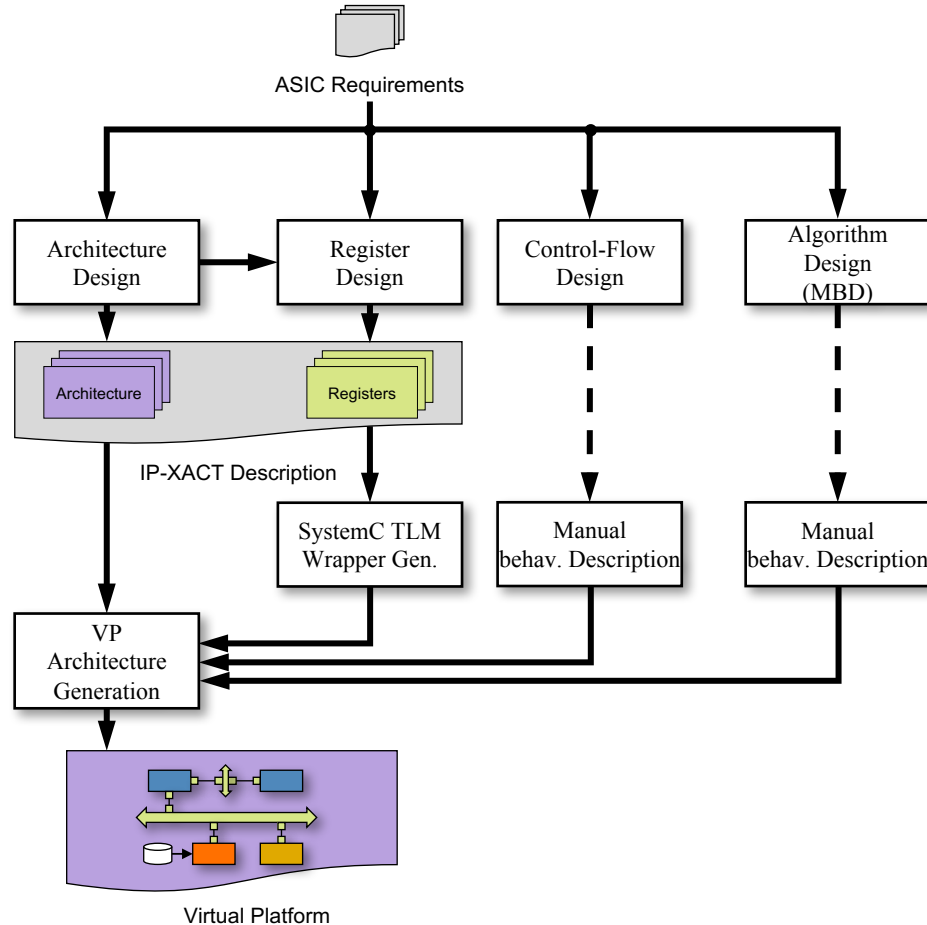


Frequency domain:



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Gap Analysis



► Benefits of Model-Based Design

- Verified algorithm meeting signal processing characteristics

► Workflow Gap

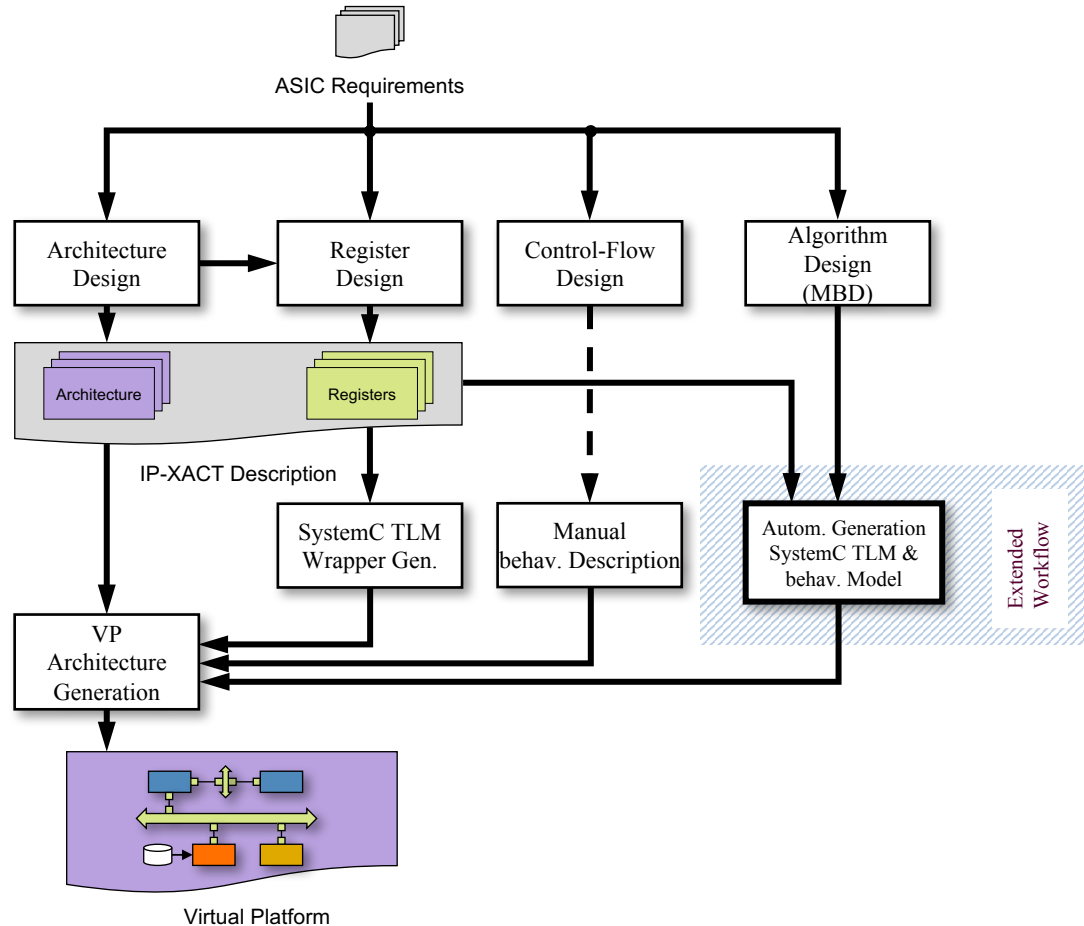
- Manual behavioural description of algorithm
- Manual integration into SystemC TLM wrapper

► Potential Issue

- Mismatch between manual behavioural description and implementation

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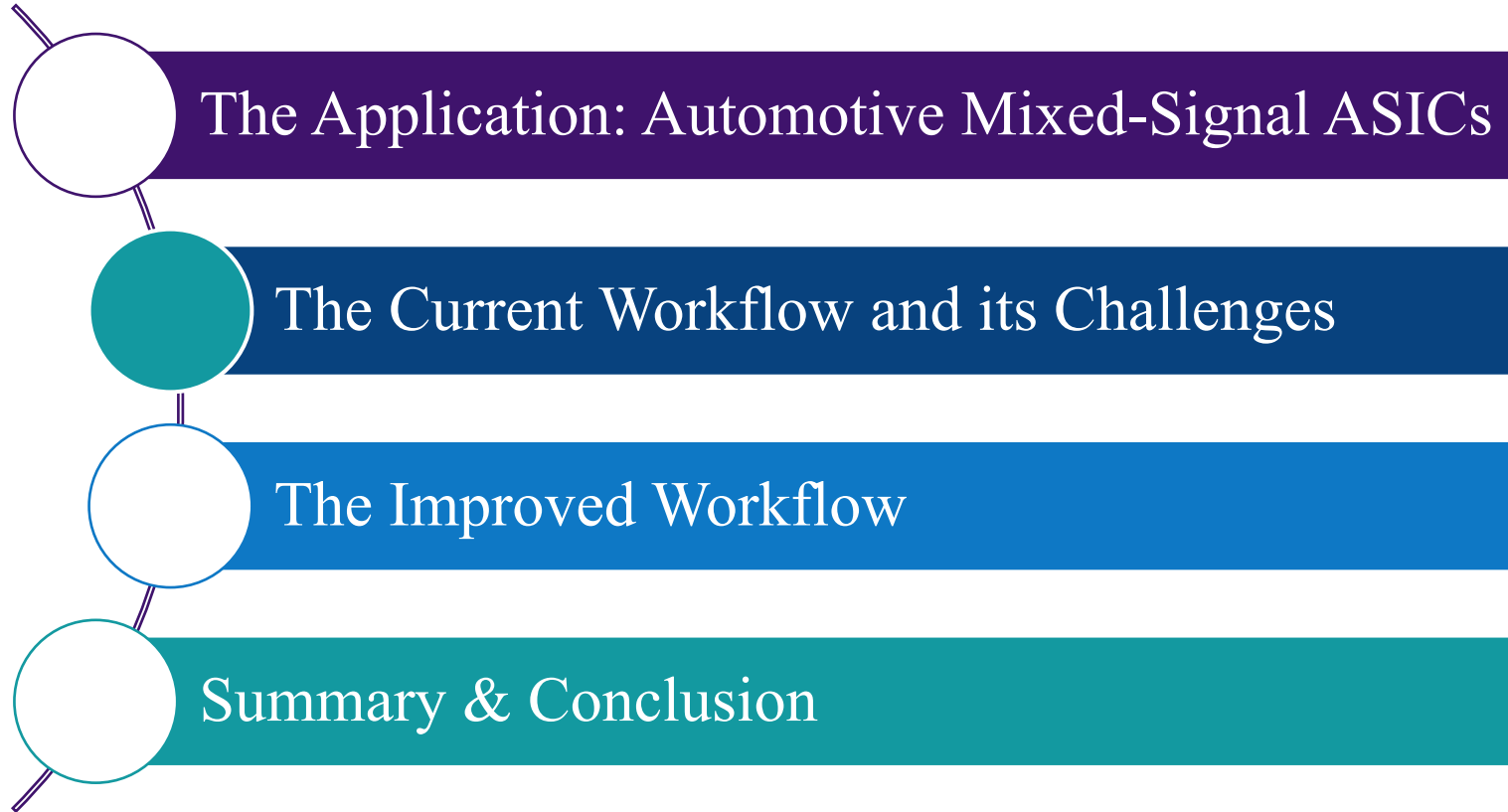
Gap Analysis



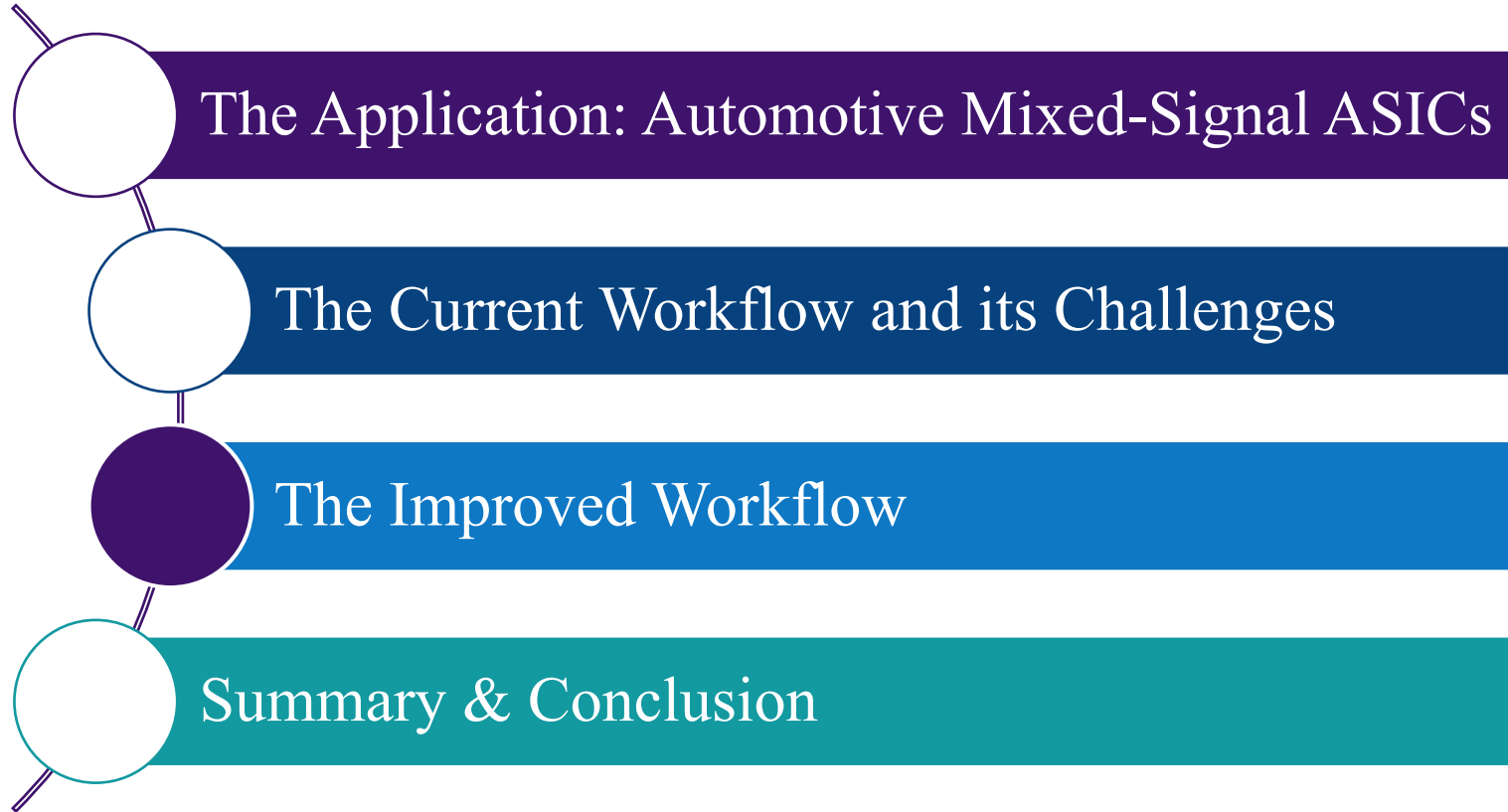
Solution:

- ▶ Automatic generation of SystemC TLM component
 - ▶ Behavioural algorithmic model
 - ▶ Integration in SystemC TLM wrapper
- ▶ IP-XACT register definition as input
- ▶ Support of SCML register

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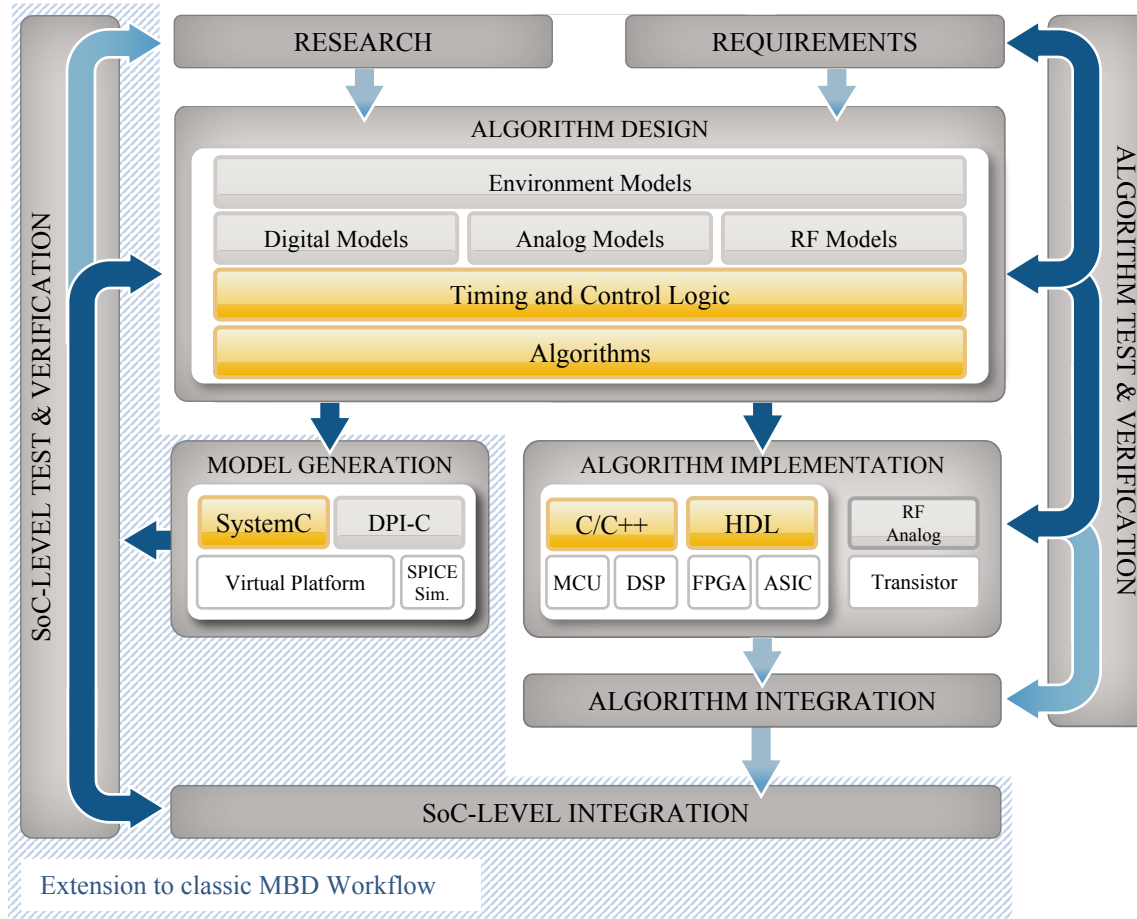


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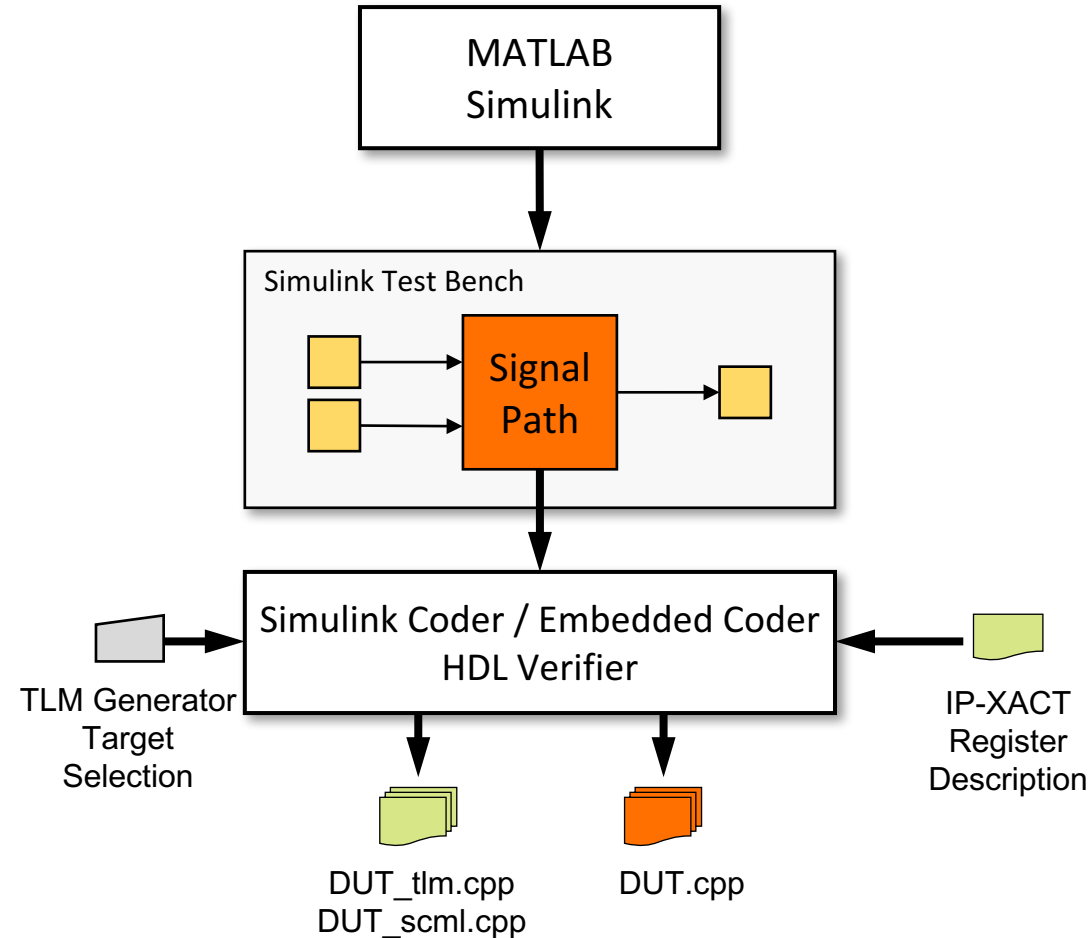
Algorithm Design & Model Generation



- ▶ Extended Model-Based Design Workflow
 - ▶ Model Generation
- ▶ Additional code generation targets
 - ▶ Virtual platforms (e.g. SystemC TLM 2.0)
 - ▶ Verification environments (e.g. SystemVerilog DPI-C)
- ▶ Benefits
 - ▶ Integrated, automated workflow
 - ▶ Functional equivalence between ..
 - Algorithm design
 - Virtual Platform model
 - Algorithm implementation

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Algorithm Design & Model Generation



► Algorithm Design

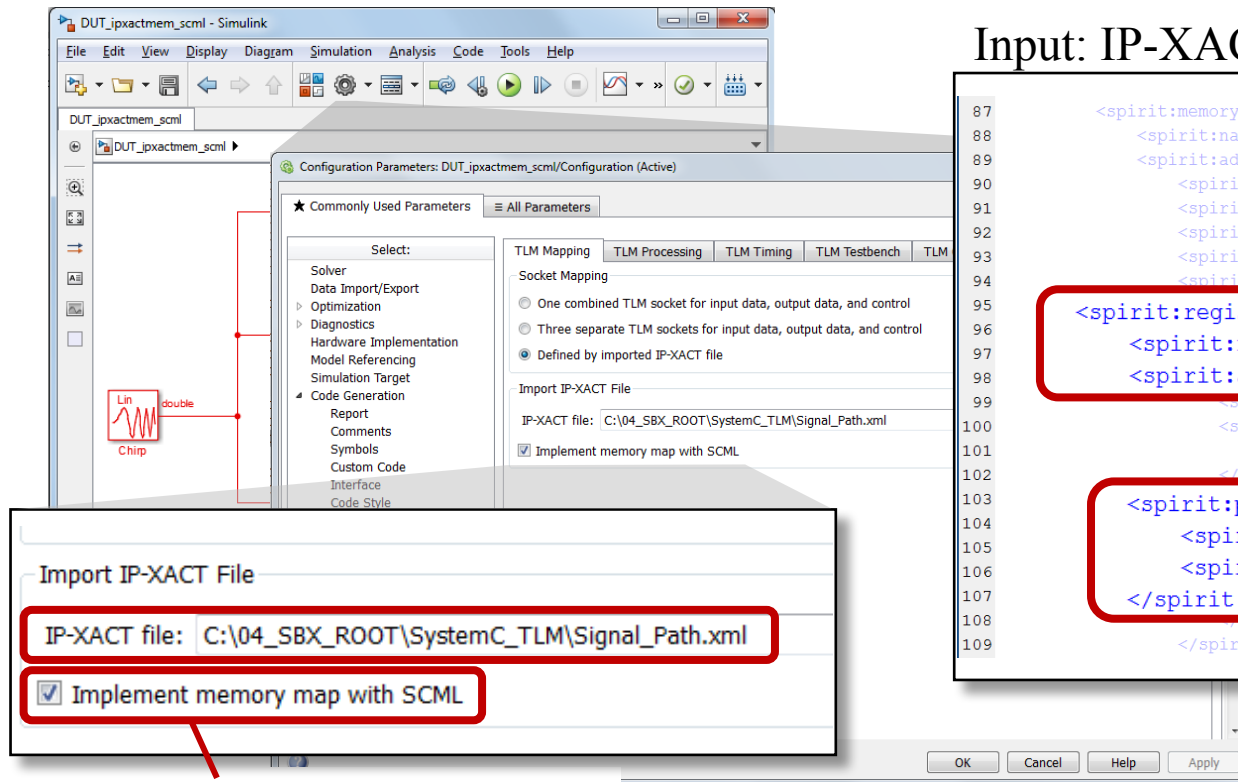
- Mathematical representation
- Multi-domain simulation environment
 - Early algorithm verification within its environment

► Model Generation

- Automatic code generation (SystemC TLM)
- IP-XACT register description as input
- Behavioural description integrated in SystemC TLM wrapper
- Self-testing SystemC TLM testbench
- IP-XACT register description as output

Integration of Simulink Models into Virtual Platforms

Model Generation - IP-XACT Register Mapping (I/O, Parameters)



SCML Register Support

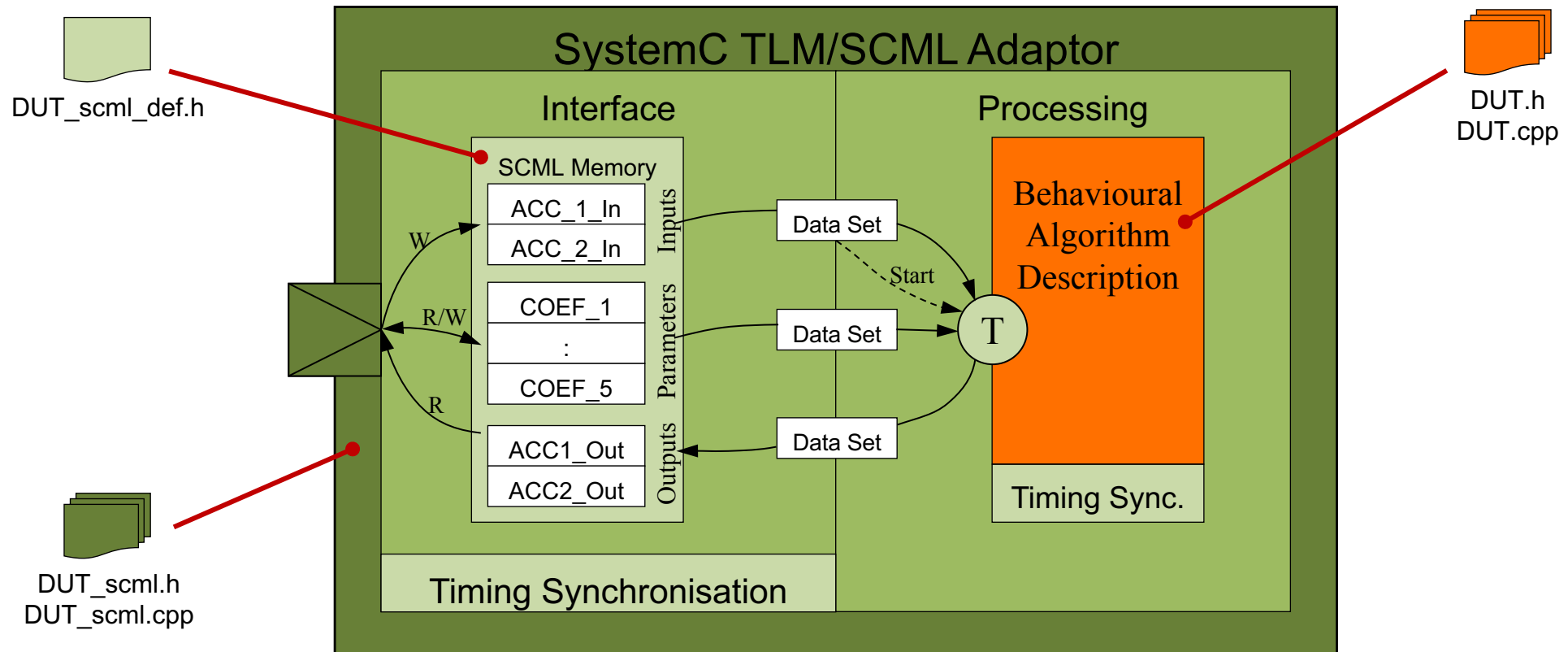
Input: IP-XACT Register Mapping

```
87 <spirit:memoryMap>
88 <spirit:name>memorymap_bus</spirit:name>
89 <spirit:addressBlock>
90 <spirit:name>BusInterface_AddressBlock</spirit:name>
91 <spirit:baseAddress spirit:id="subsystem_tlm_base_address_output"
92 <spirit:range spirit:resolve="immediate">0x100</spirit:range>
93 <spirit:width>64</spirit:width>
94 <spirit:usage>register</spirit:usage>
95 <spirit:register>
96 <spirit:name>ACC1_Out</spirit:name>
97 <spirit:addressOffset>0x00</spirit:addressOffset>
98
99 <spirit:access>read-only</spirit:access>
100 <spirit:reset>
101 <spirit:value>0x00</spirit:value>
102 </spirit:reset>
103 <spirit:parameter>
104 <spirit:name>MwMapOutput</spirit:name>
105 <spirit:value>sym_Hlp4</spirit:value>
106 </spirit:parameter>
107 </spirit:register>
108
109 </spirit:memoryMap>
```

Interface mapping between
IP-XACT and Simulink

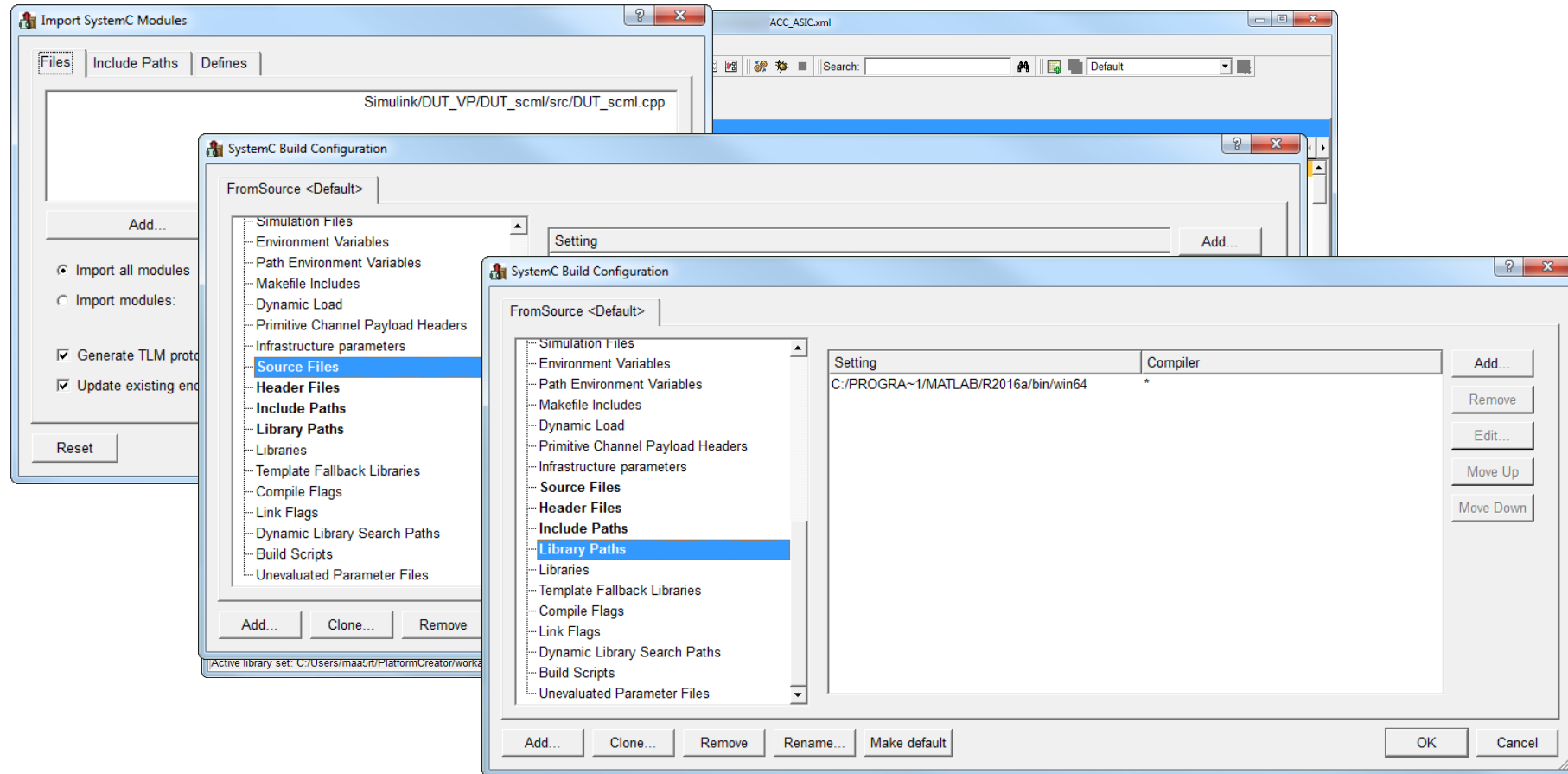
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Model Generation - SystemC TLM/SCML Adaptor Architecture



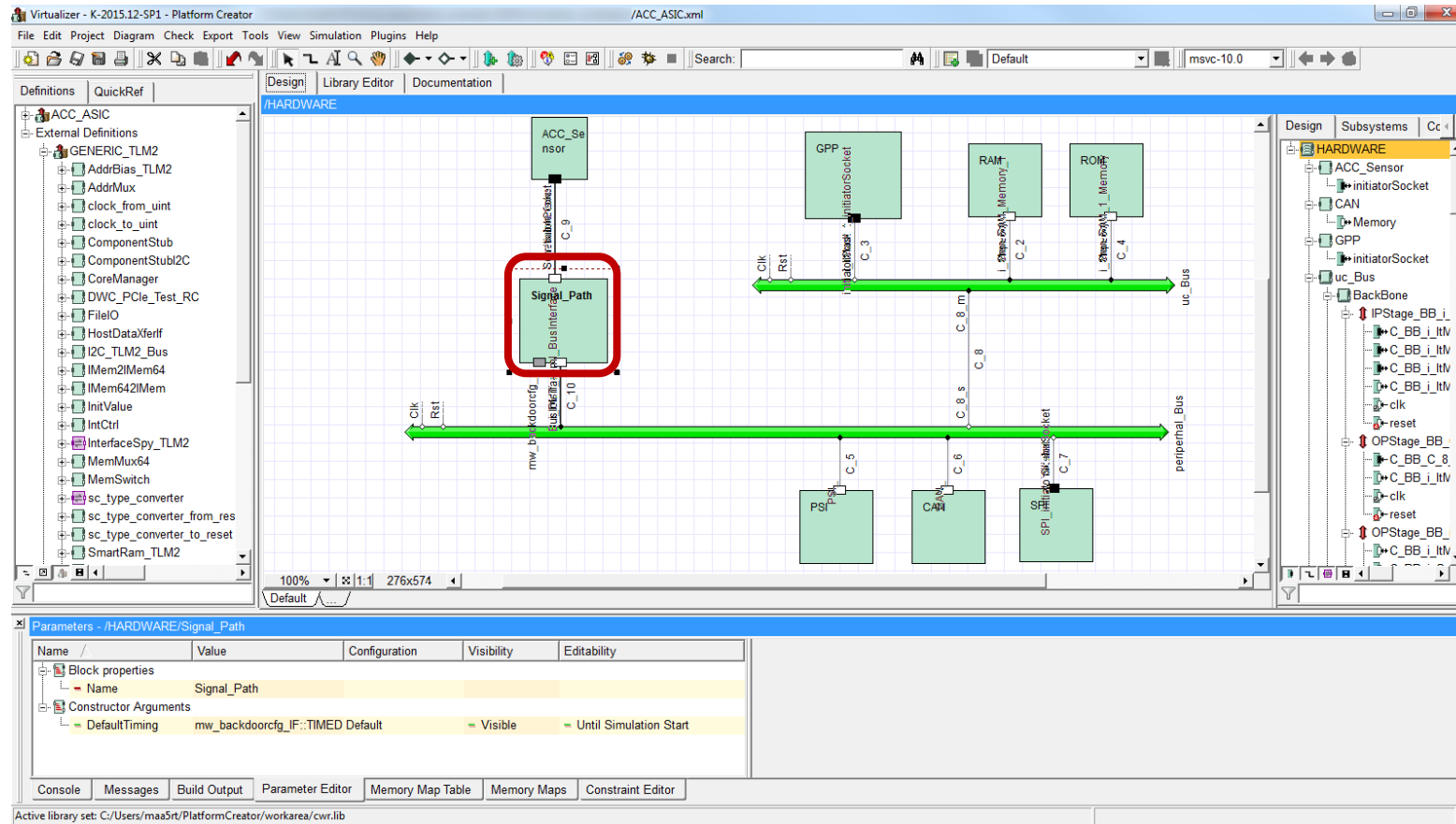
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Integration and Simulation - Manual Import of SystemC Module



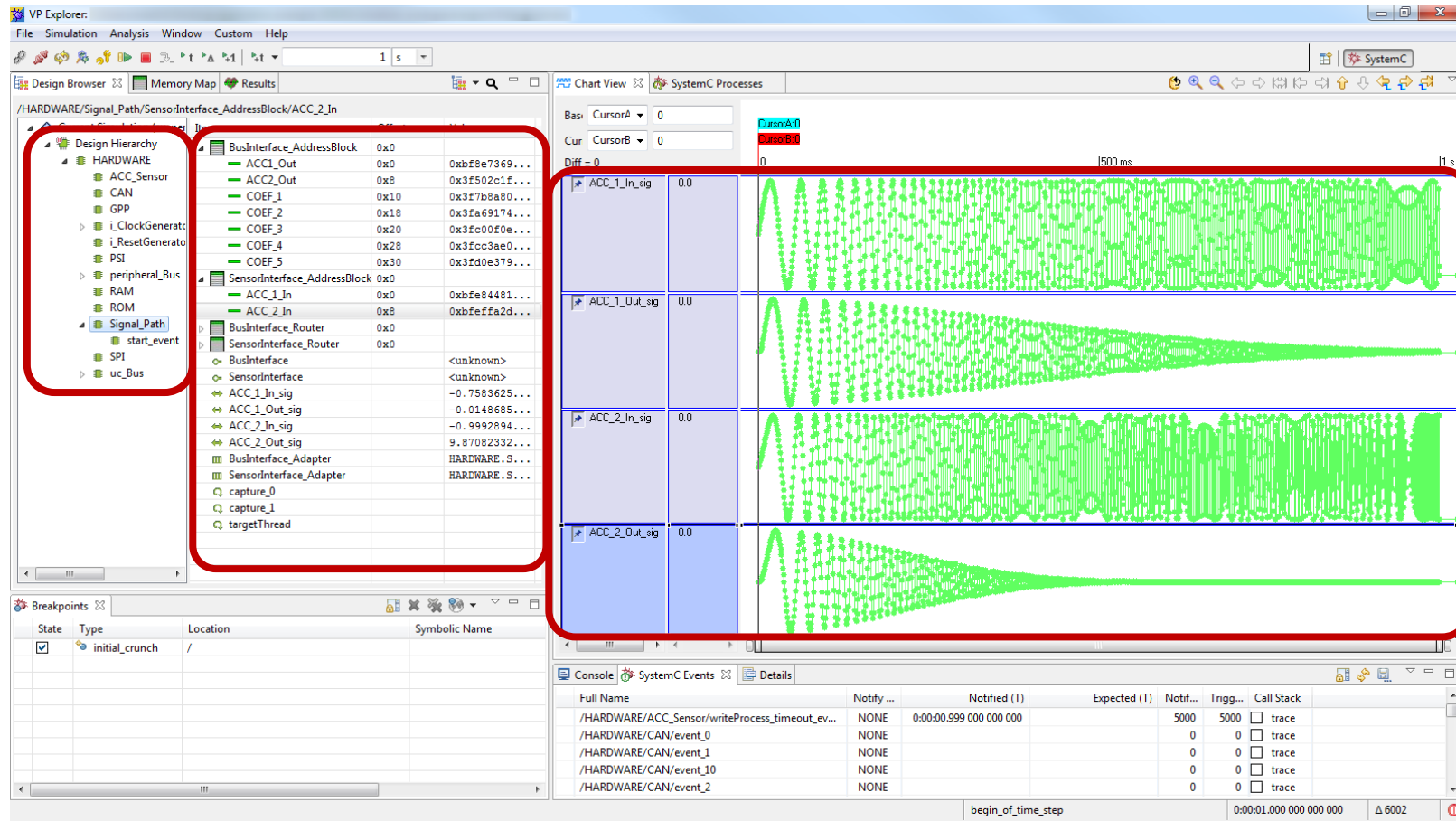
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Integration and Simulation - SystemC Module in Synopsys® Virtualizer™

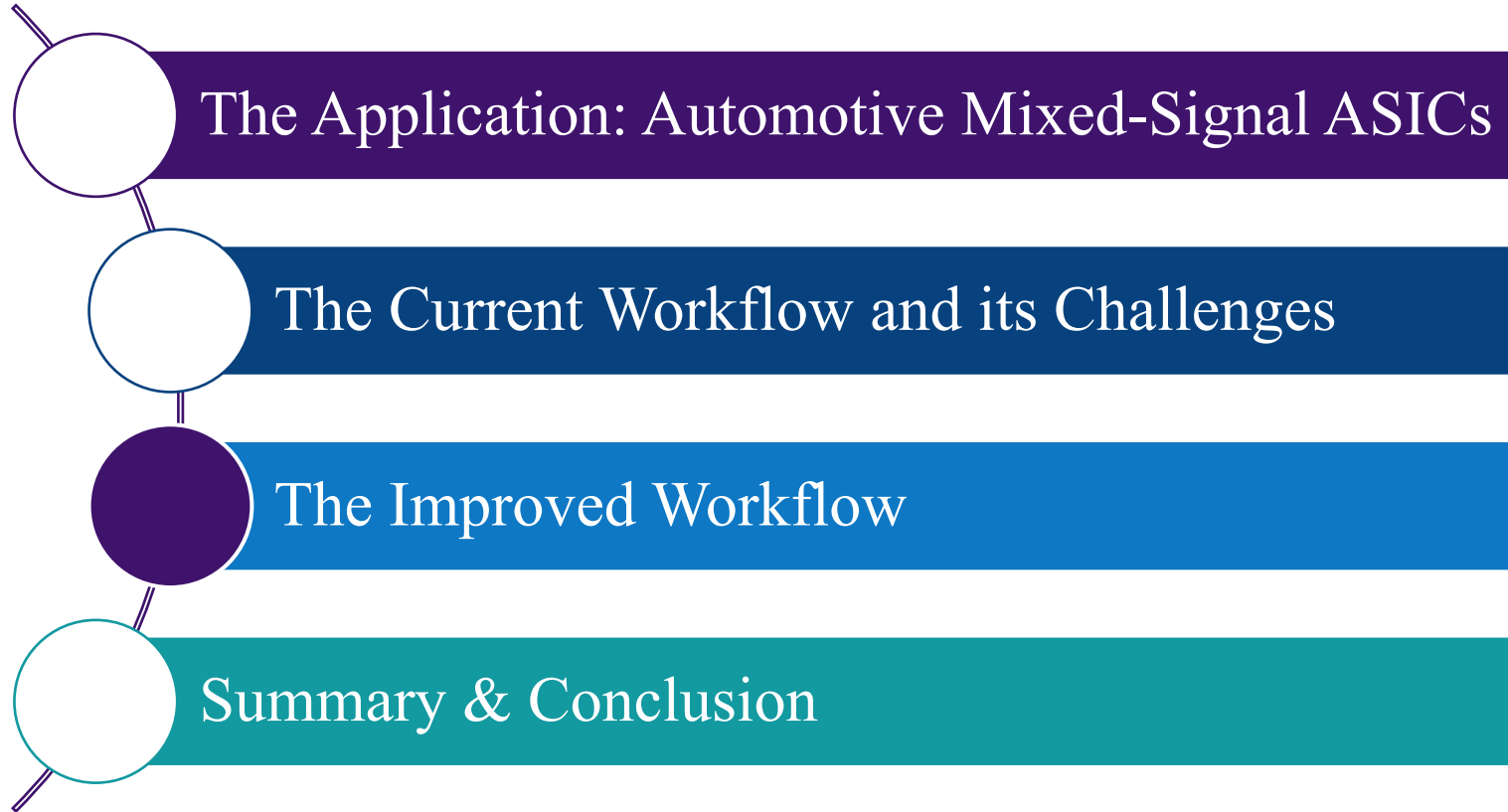


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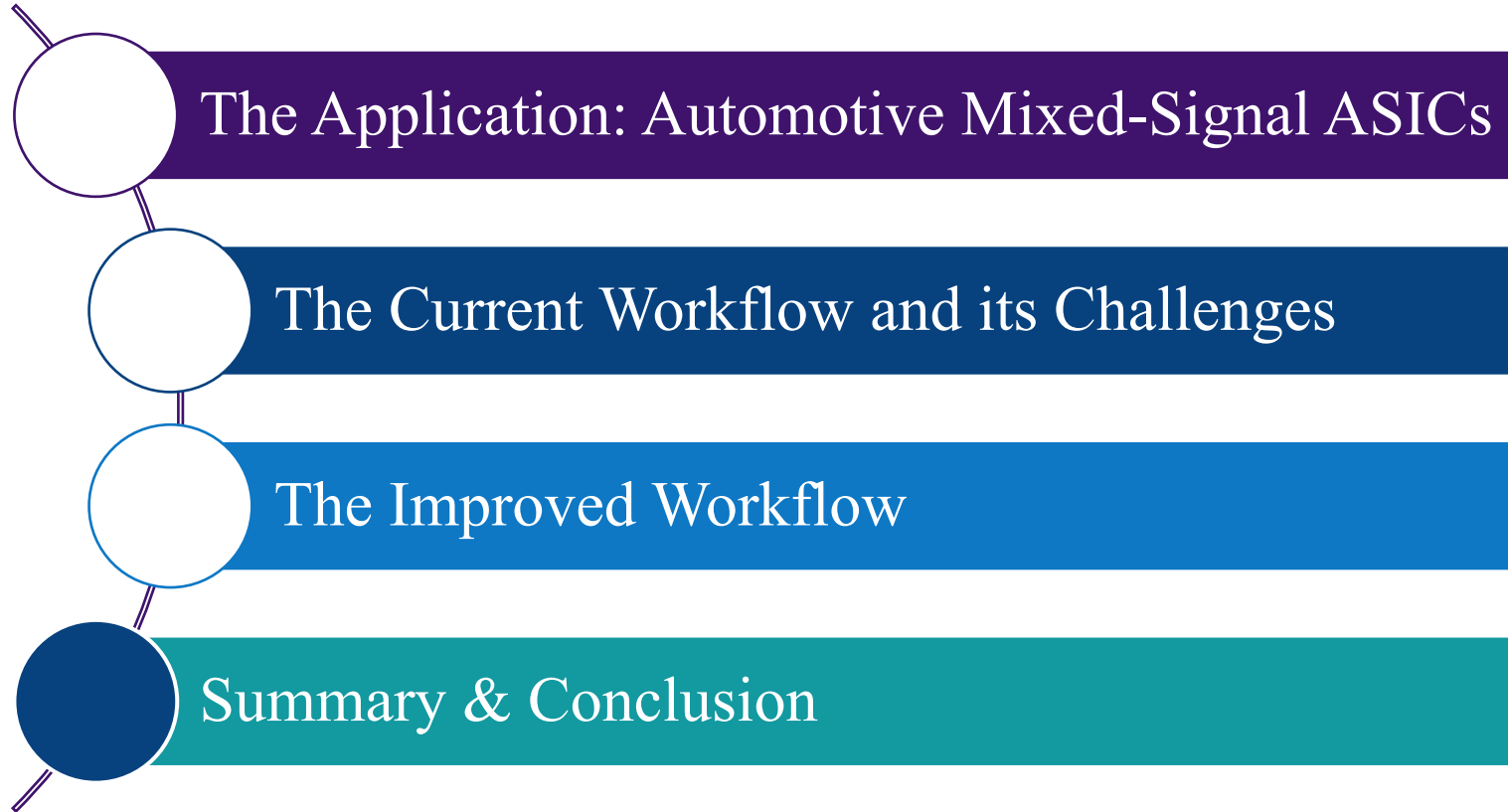
Integration and Simulation – Simulation in Synopsys® VPEXplorer



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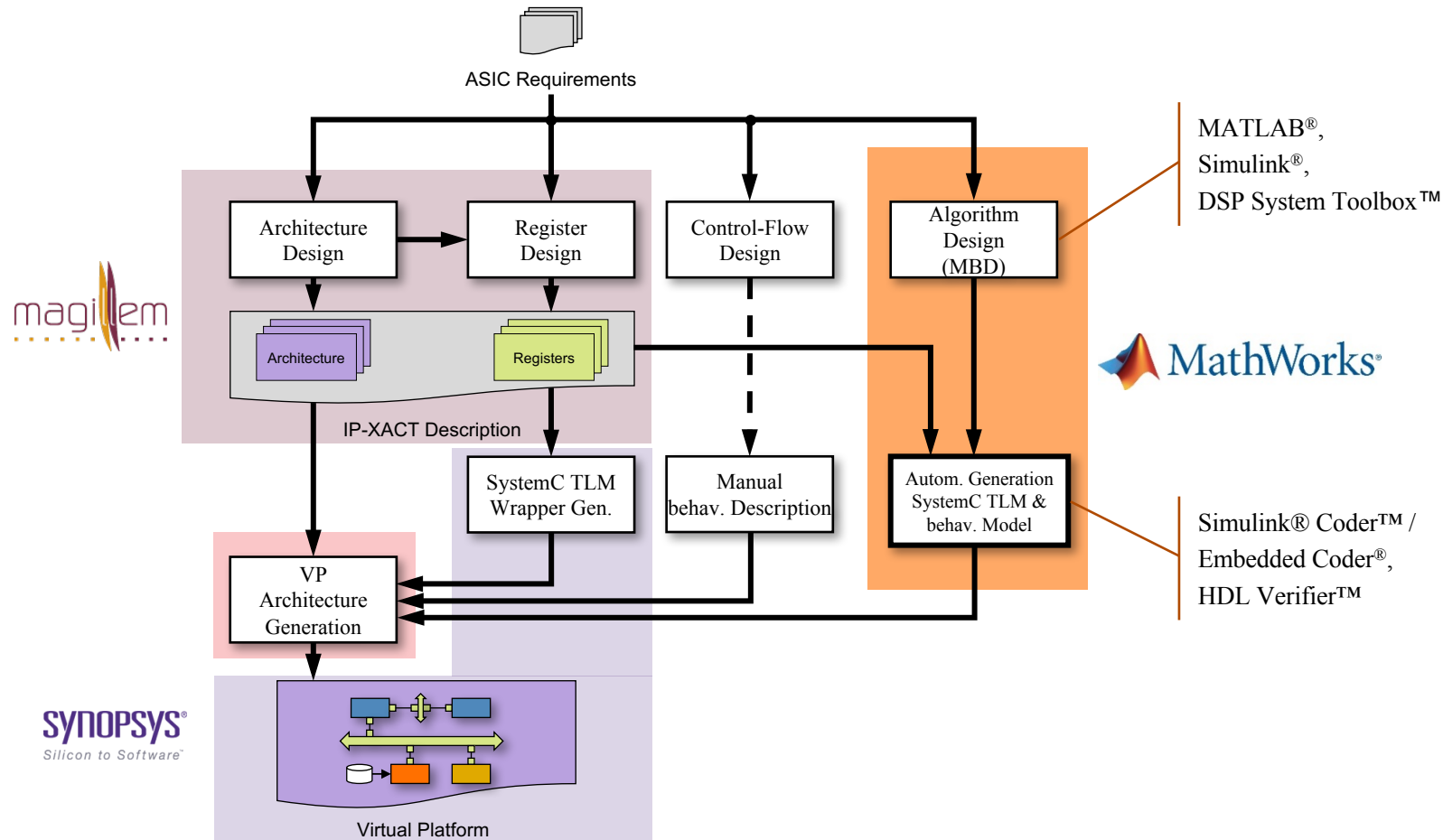


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Integration of Simulink Models into Virtual Platforms

Summary – Bosch Workflow



Integration of Simulink Models into Virtual Platforms

Summary & Conclusion

- ▶ Developed method:
Automated integration of Simulink signal processing behaviour modules into Virtual Platforms
- ▶ Generated artefacts:
 - ▶ Functional core
 - ▶ SystemC TLM2.0 Wrapper with SCML registers based on IP-XACT description
 - ▶ Code connecting wrapper and functional core
- ▶ Benefits:
 - ▶ Increase of efficiency for integration signal processing behaviour into VPs
 - ▶ Earlier availability of functional VPs of signal processing ASICs
 - ▶ Inherent consistency between Simulink model and VP

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