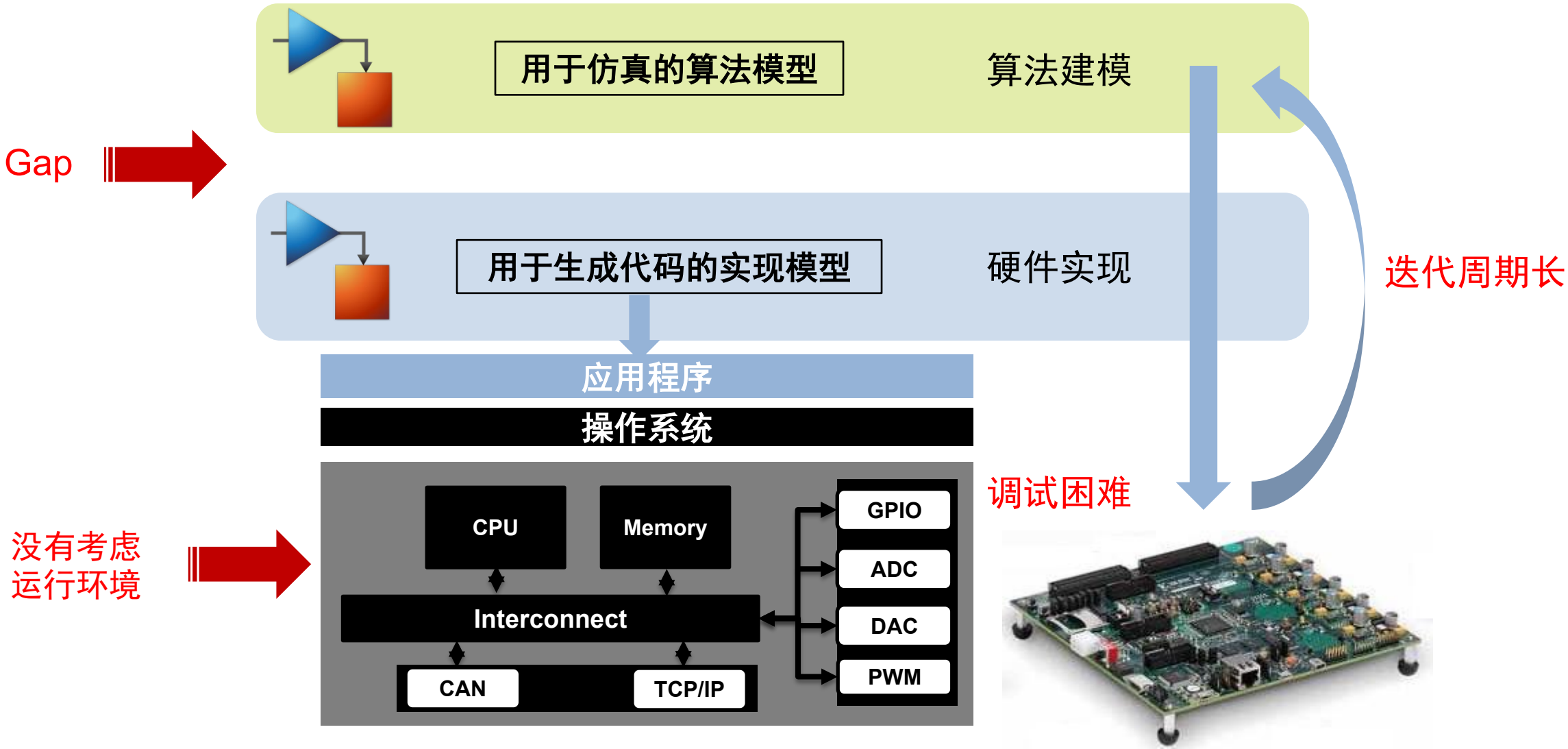
MATLAB EXPO

将算法模型快速部署到 DSP 和 FPGA

赵恒 MathWorks

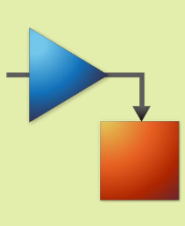
MathWorks®

算法和实现之间容易脱节



结合架构考虑算法的实现

No gap



系统模型
(算法 + 软硬件)

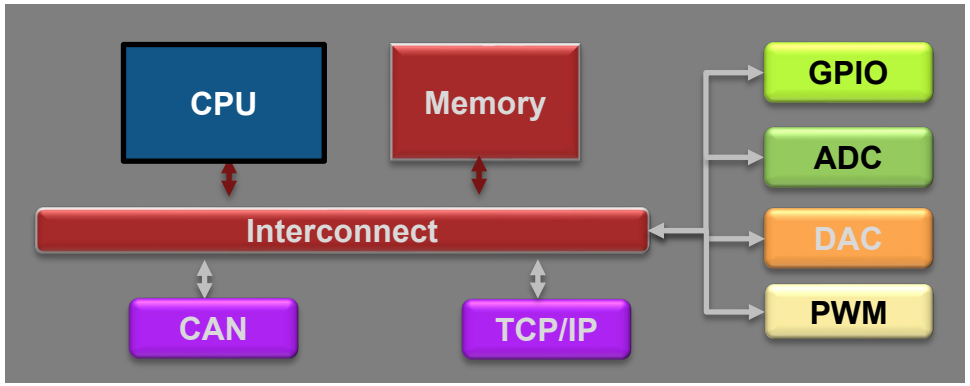
算法建模
+
硬件实现

缩短迭代周期

应用程序

操作系统

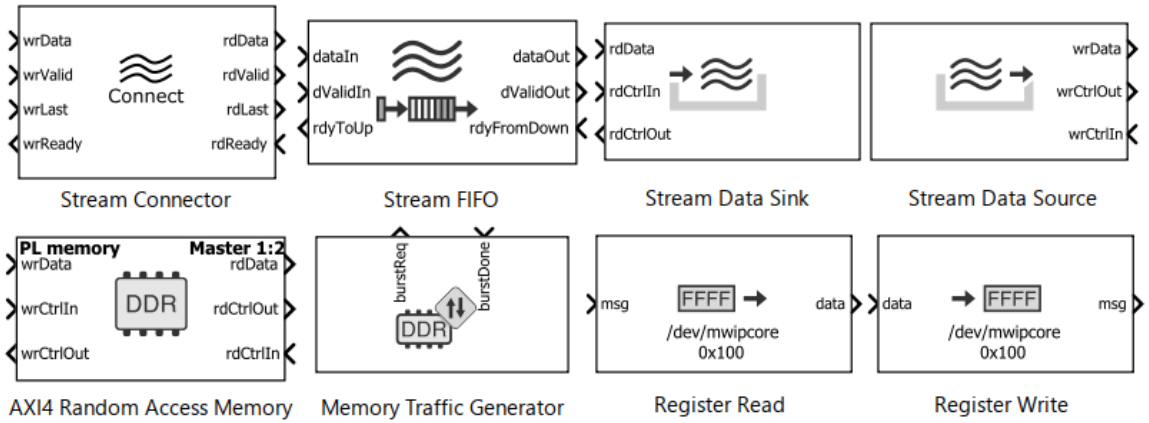
结合考虑
运行环境

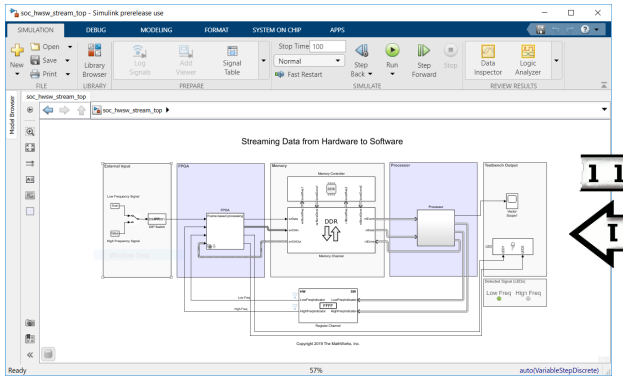


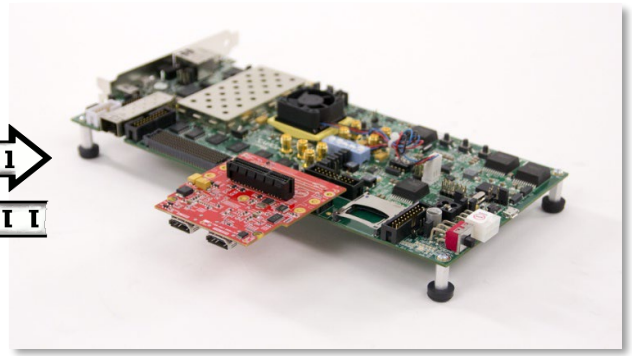
易于调试

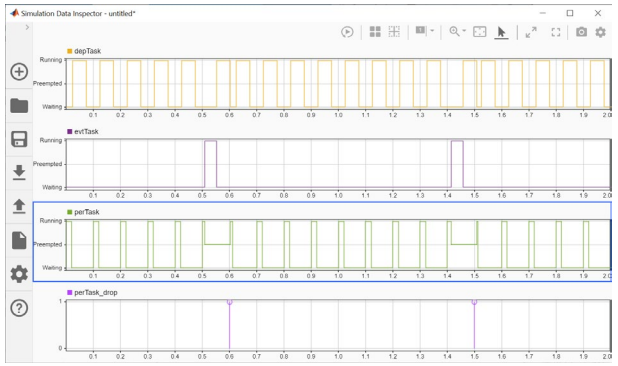
架构仿真的核心功能

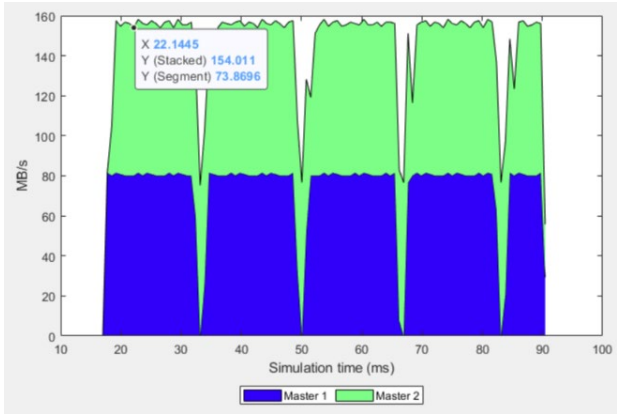
- 系统建模
  - 任务调度、中断
  - 核间通信、数据缓冲
  - 多核运行、可视化
- 快速原型
  - 软硬件工程创建
  - 集成设备驱动
  - 适配定制开发板
- 实测运行
  - 任务执行可视化
  - CPU利用率
  - 性能分析报告



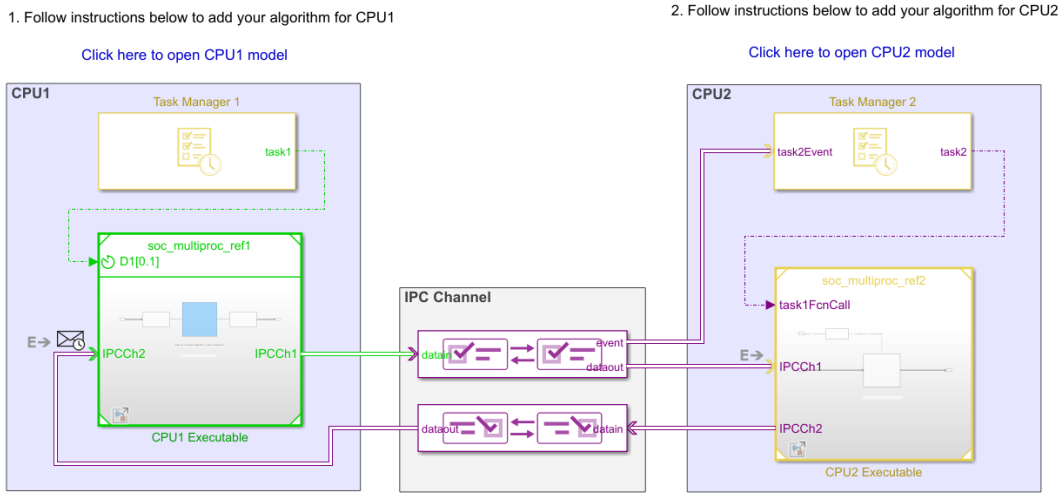




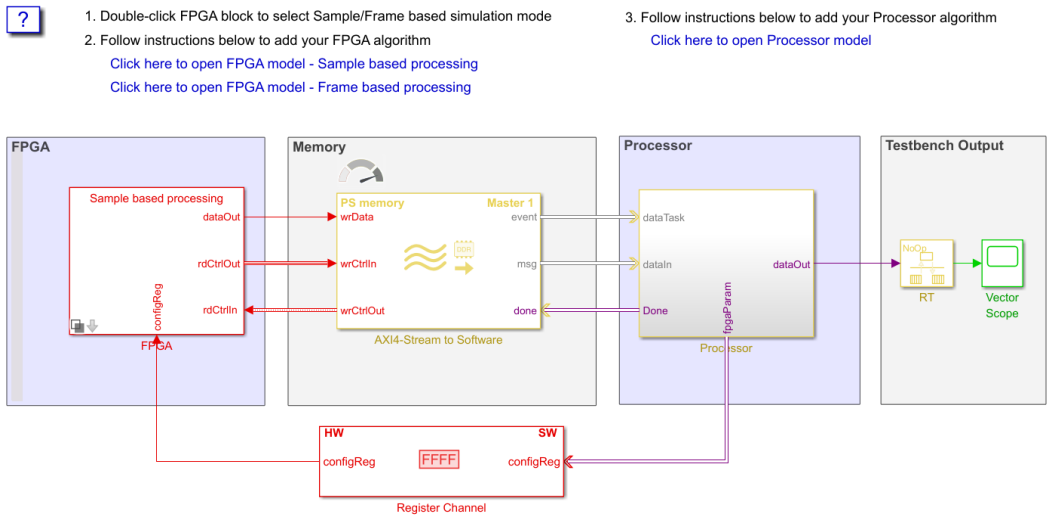




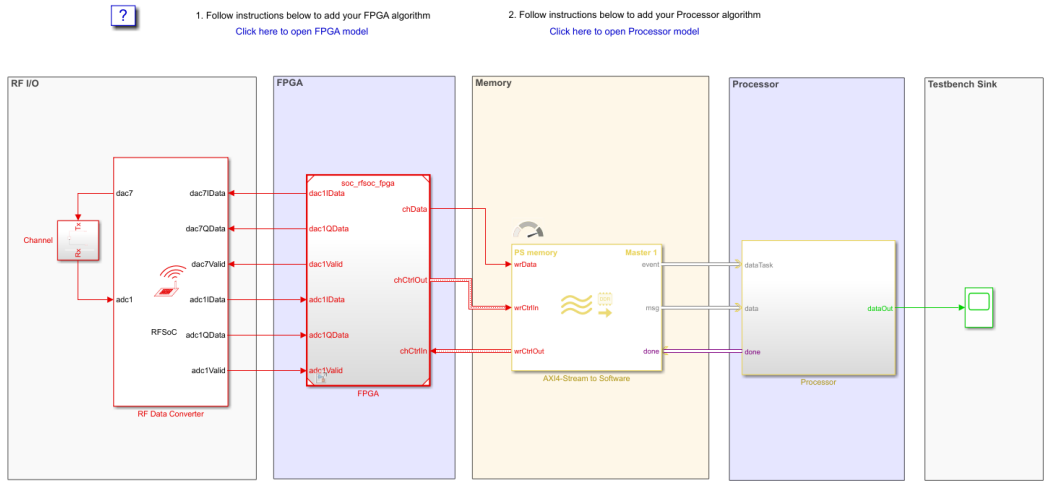
从模板创建架构模型



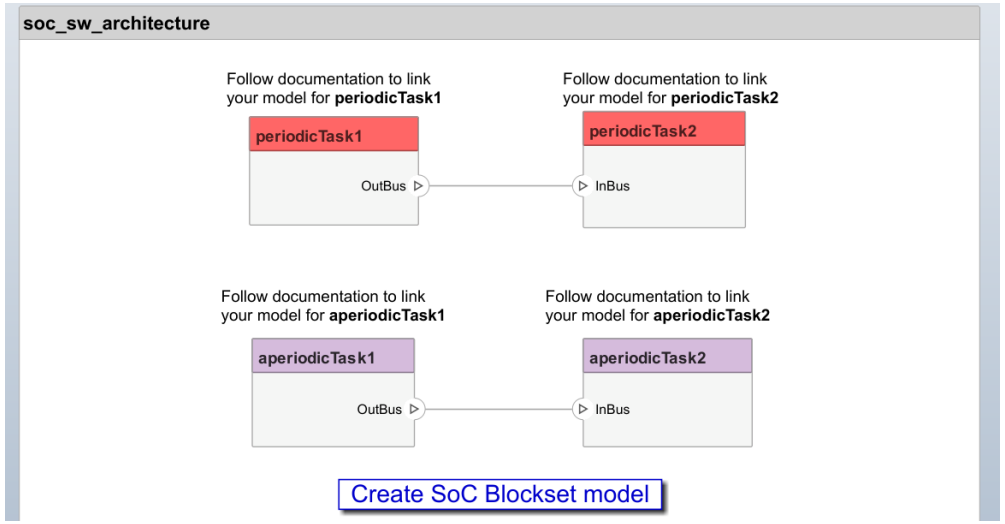
多核架构模型



FPGA和处理器数据流模型

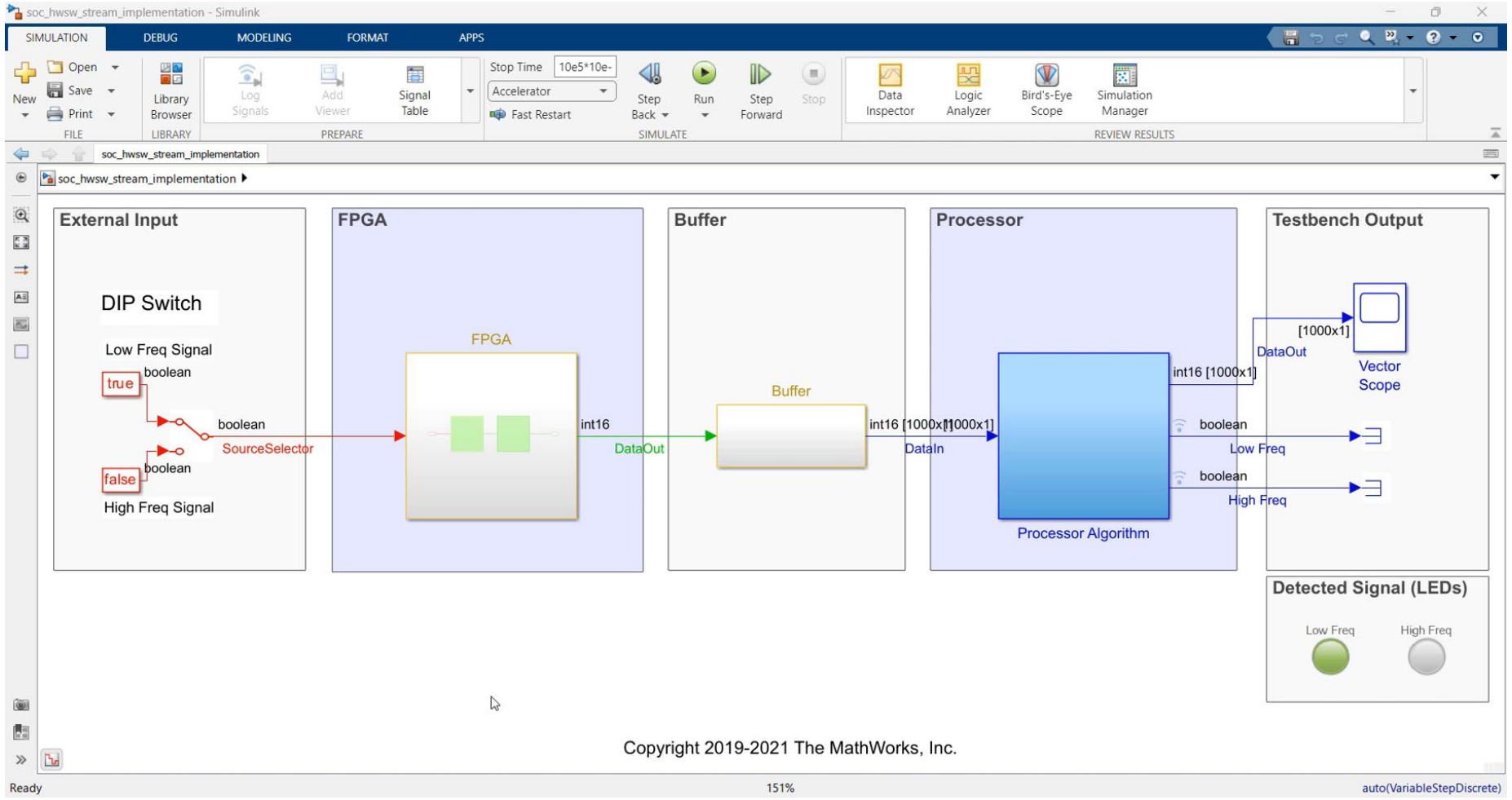


RFSoC应用模型

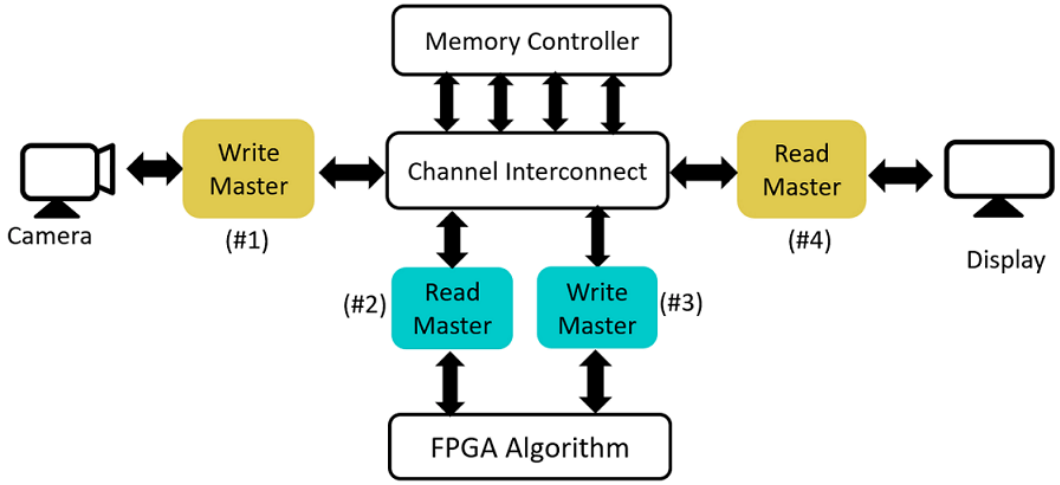


SoC软件架构模型

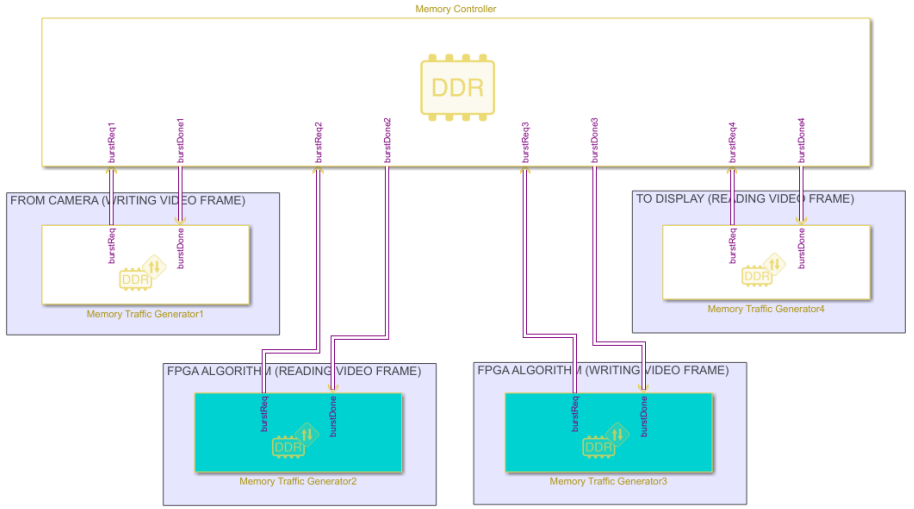
片内数据传输建模与性能分析



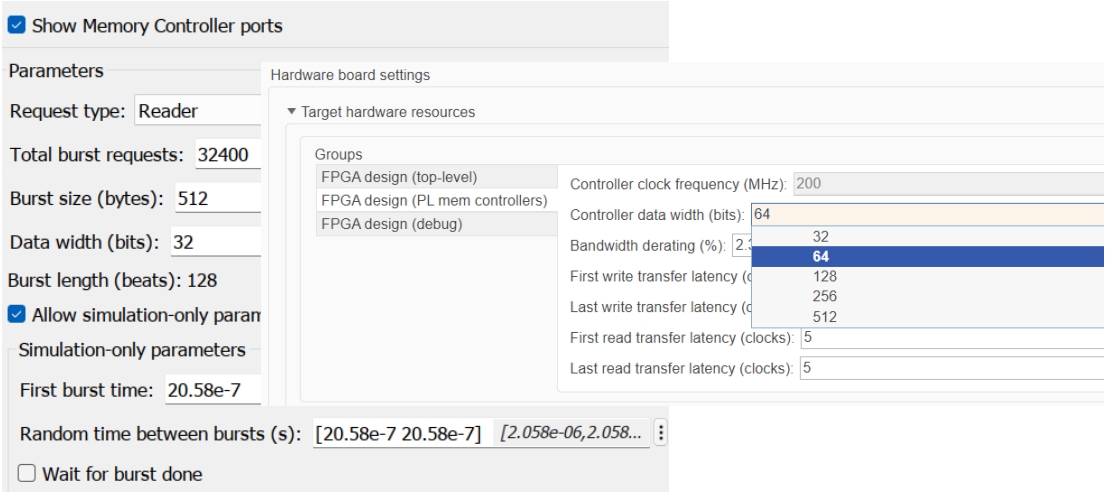
访存建模与性能分析



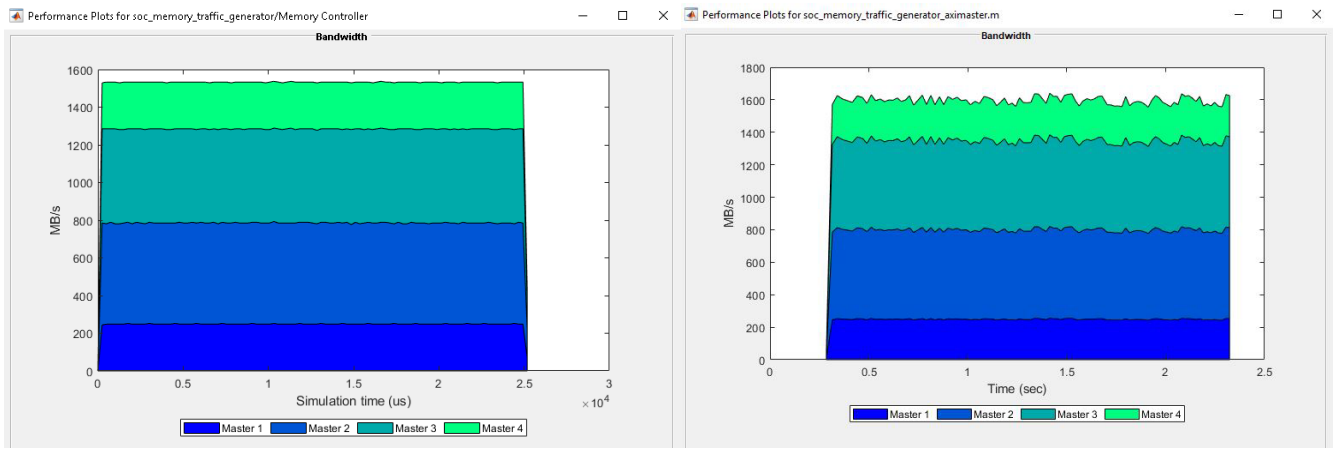
系统架构



仿真模型



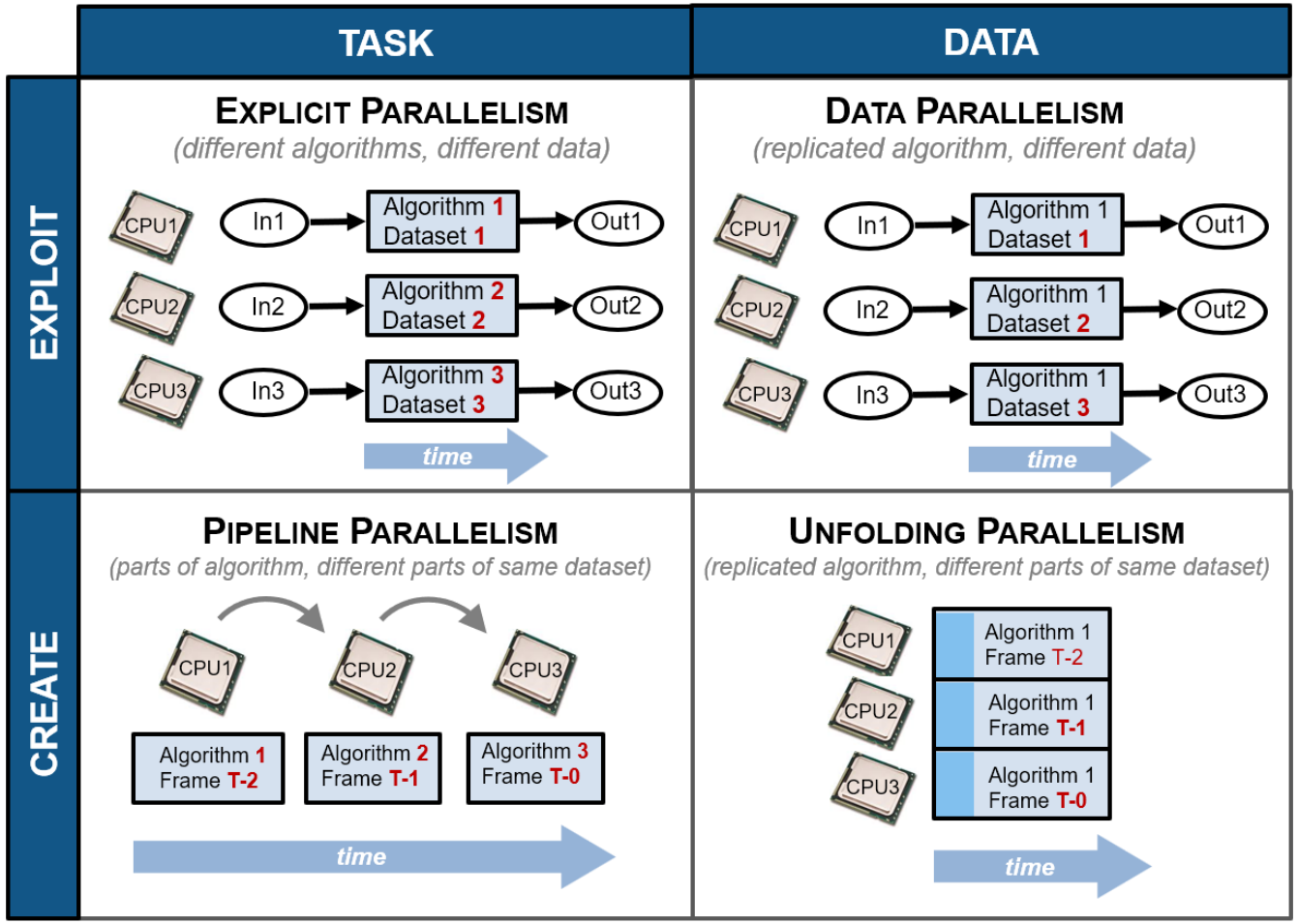
参数设置



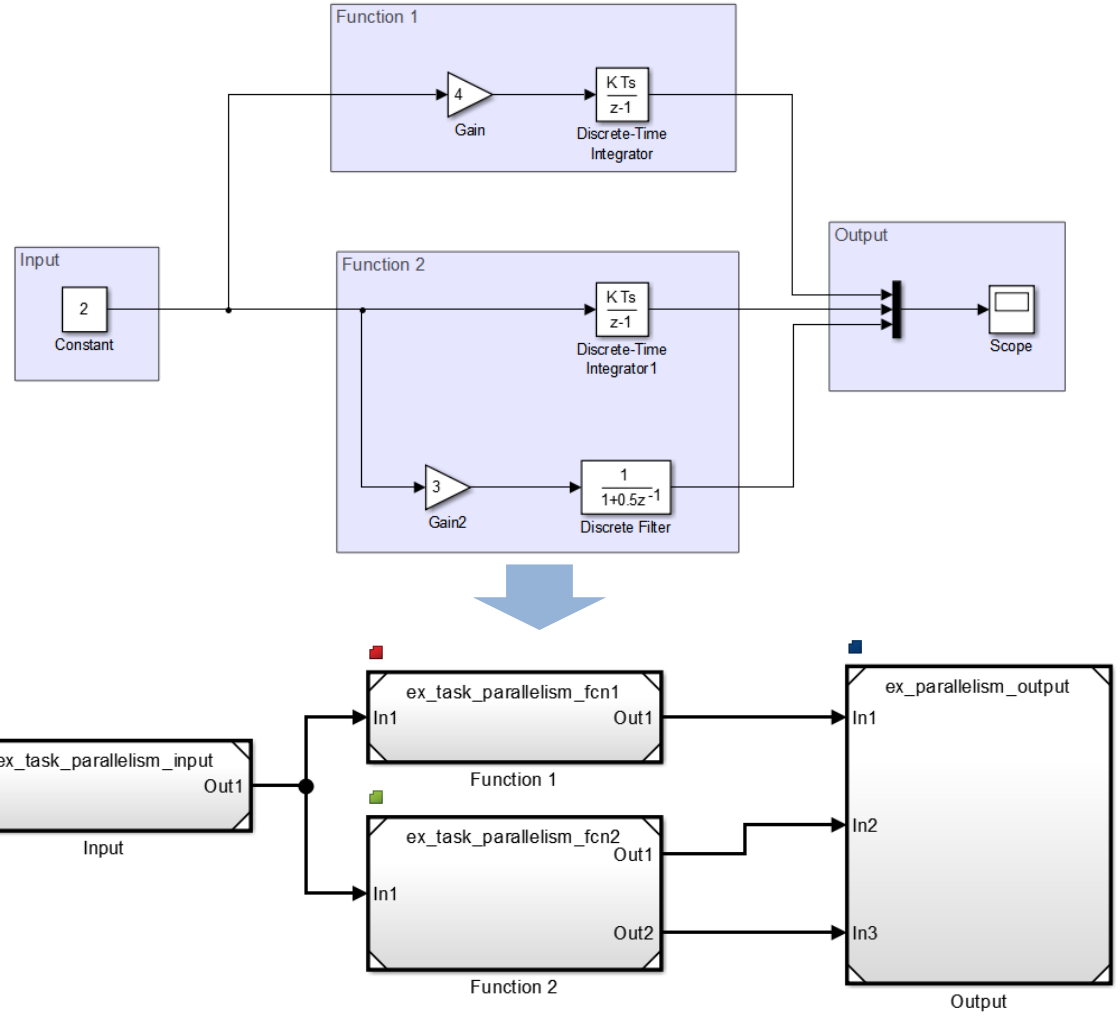
访存带宽

数据流（Dataflow）

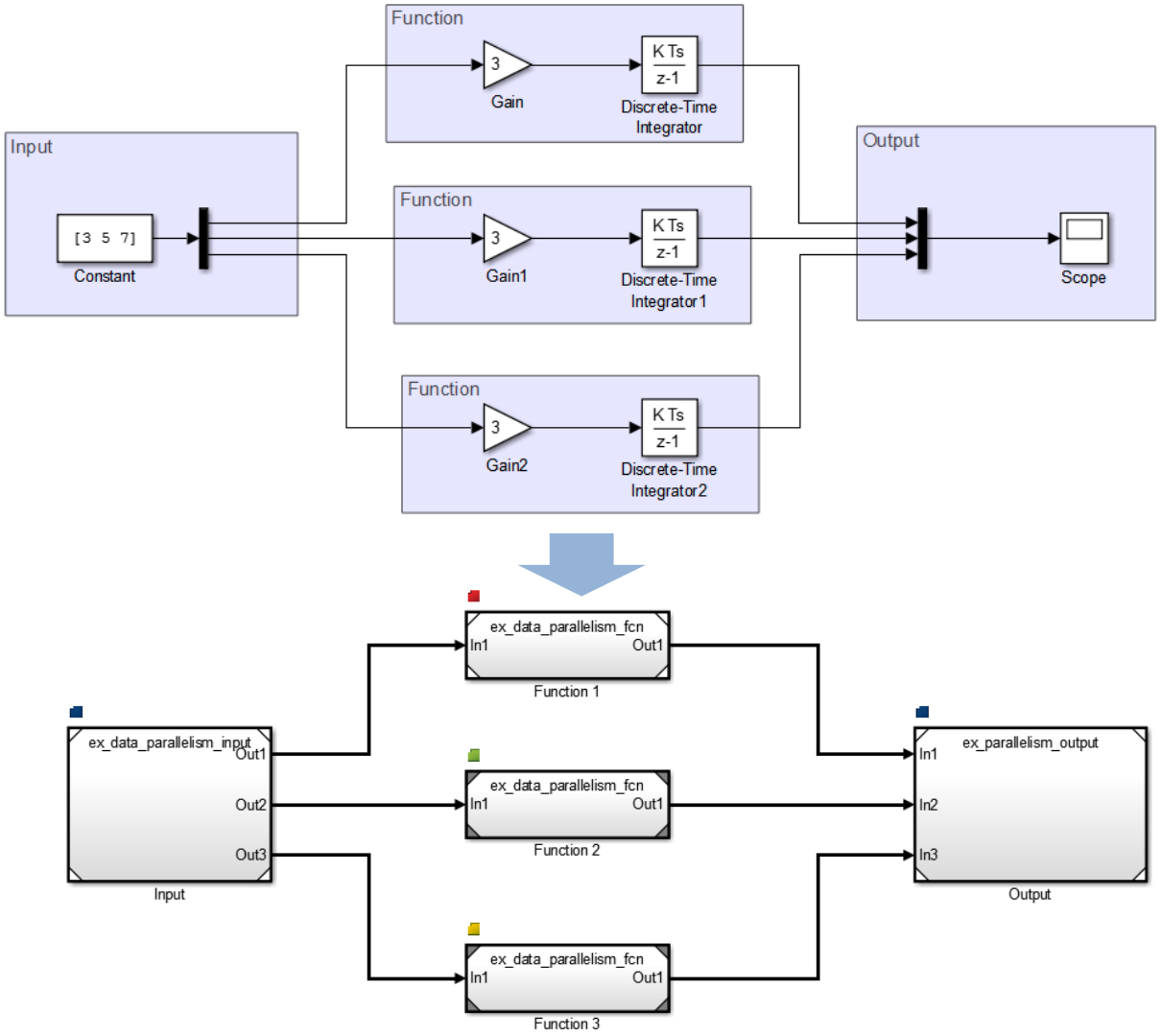
- 信号处理中的数据流
  - 模型计算密集部分
  - 数据驱动
  - 静态调度
- 使用数据流模型的收益
  - 开发算法内在并行性
  - 多线程提高仿真速度
  - 自动推断信号维度
- 数据流模型的仿真
  - 利用多核CPU
  - 多线程运行仿真
  - 代价分析



DSP算法的并行性

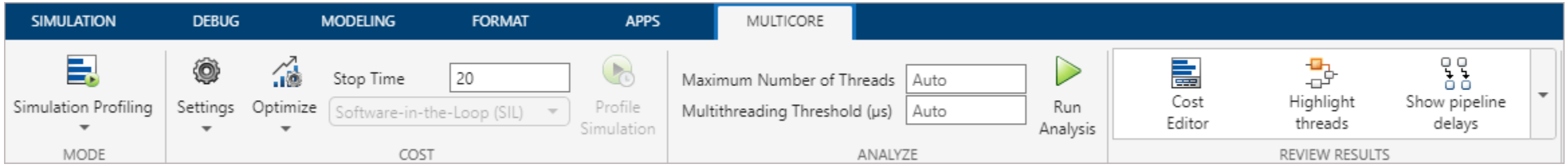


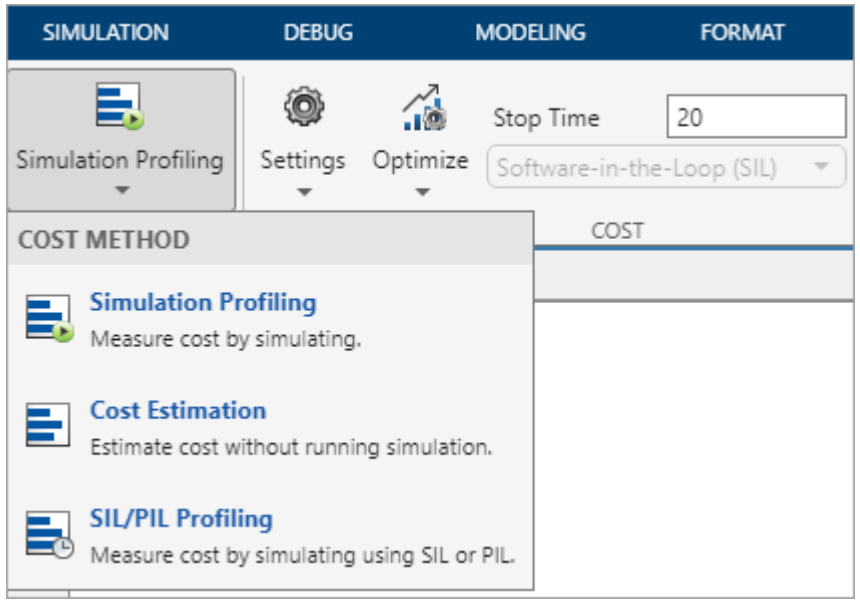
任务并行



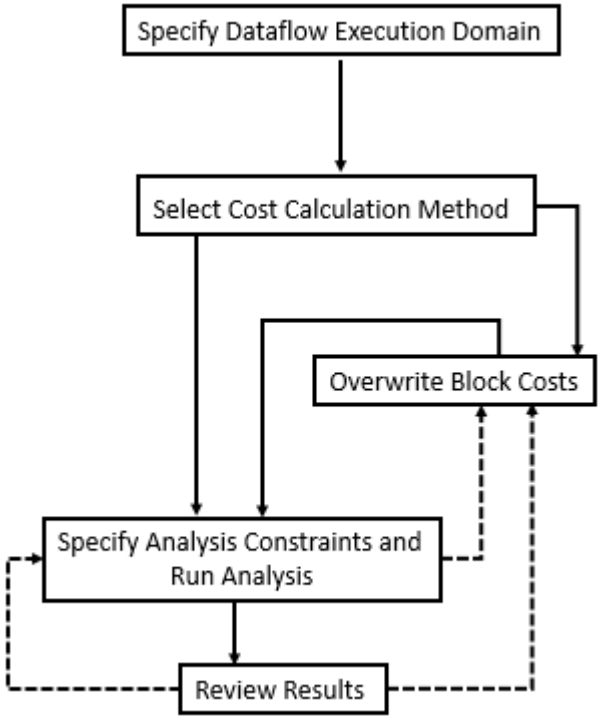
数据并行

多核模型性能分析

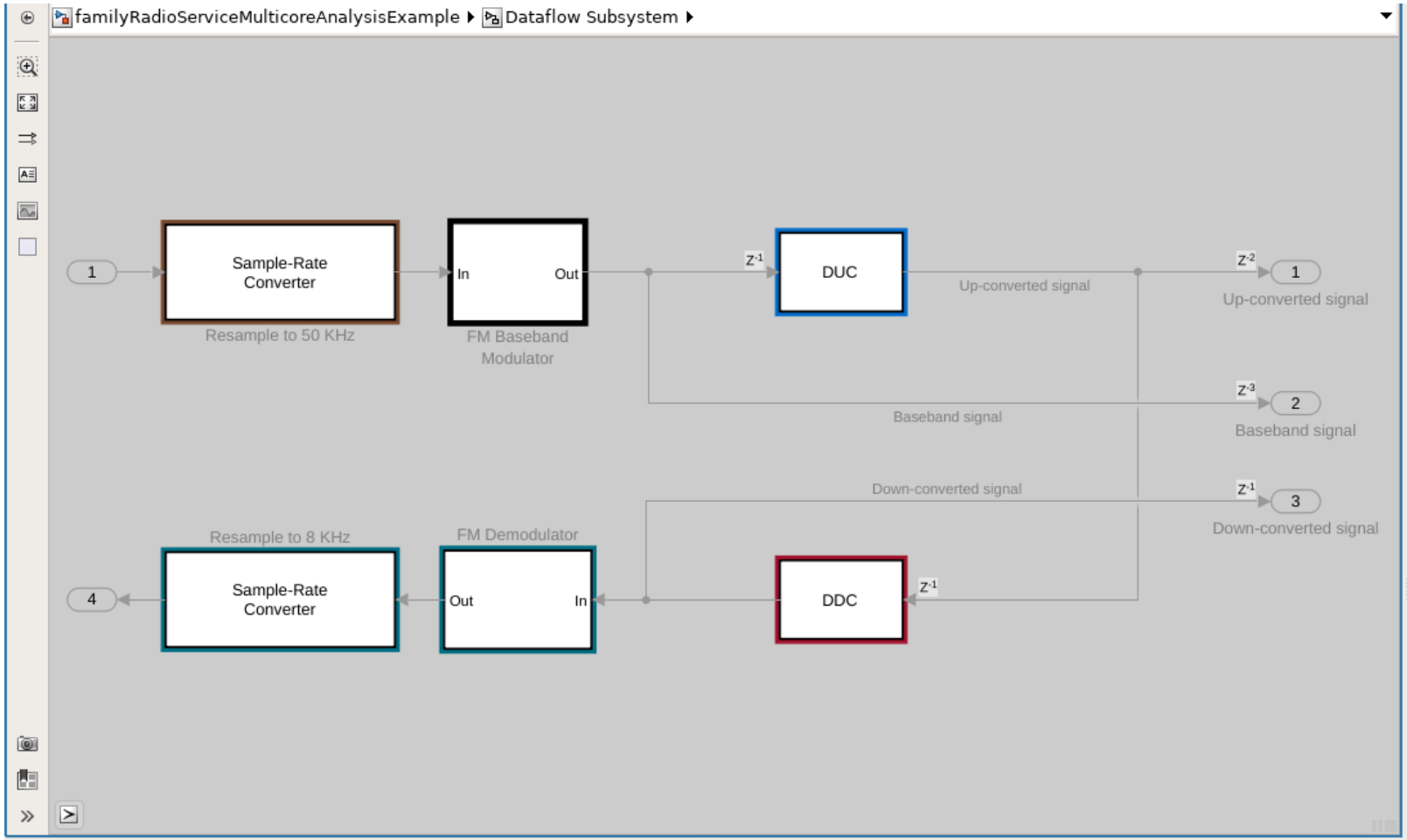




评估方式



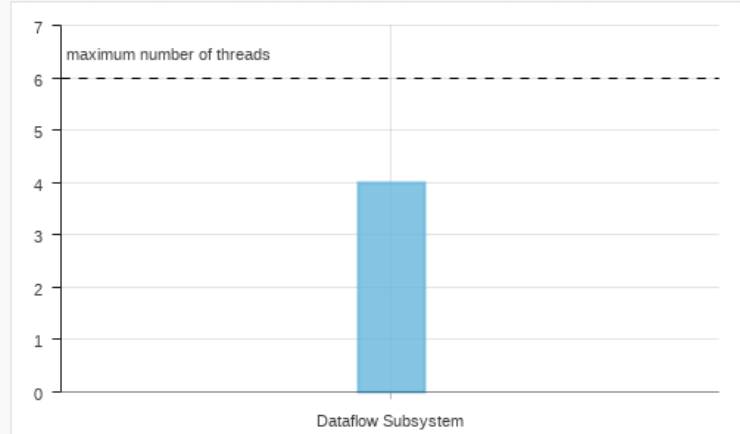
分析流程



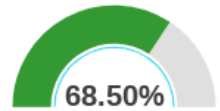
The dataflow subsystems will utilize 4 cores based on the analysis made with profiled cost values.

View: Threads

Number of threads per dataflow subsystem

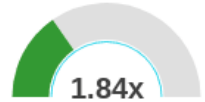


Relative weight of dataflow subsyste...



of entire model

Maximum theoretical speedup



compared to single-threaded execution

Property Inspector | Analysis Report and Suggestions

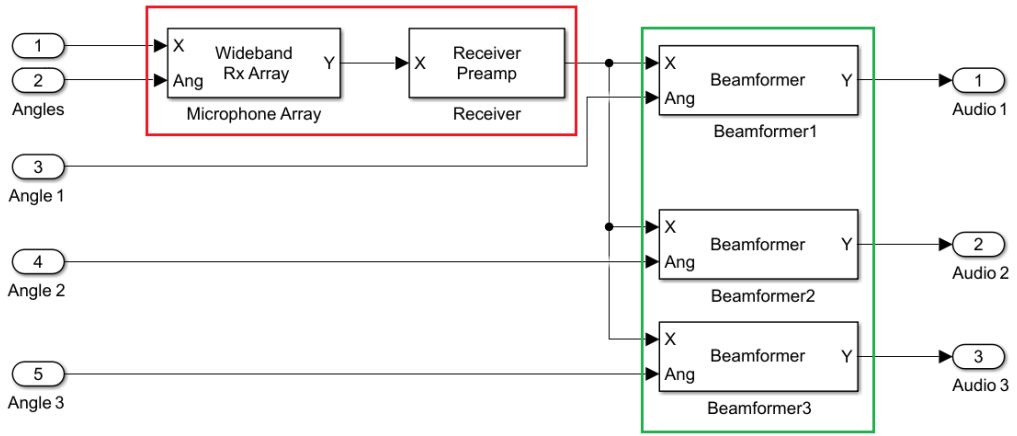
Cost Editor

Block	Auto	Cost (µs)	Relative Load
Dataflow Subsystem			
Dataflow Subsystem/Digital Down-Converter	☐	70000	
Dataflow Subsystem/Digital Up-Converter	☐	70000	
Dataflow Subsystem/Resample to 50 KHz	☐	70000	
Dataflow Subsystem/FM Baseband Modulator/Magnitude-Angle to Complex	☑	1921	
Dataflow Subsystem/FM Demodulator/Complex to Magnitude-Angle	☑	1504	

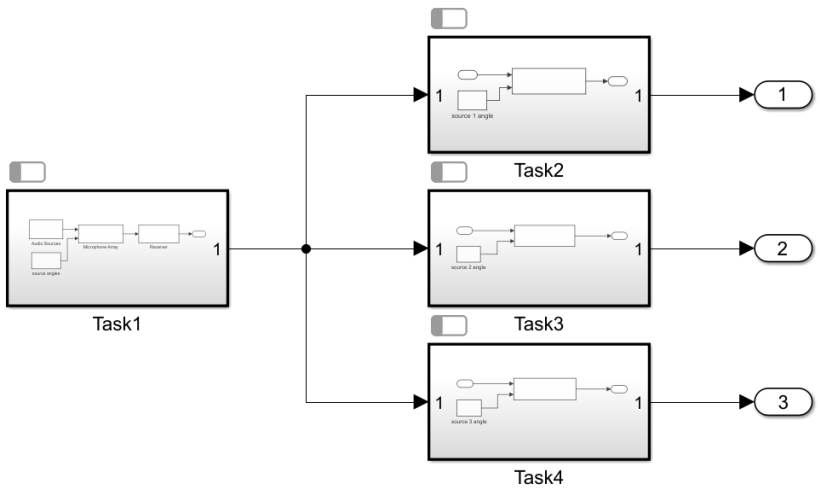
Thread Highlighting Legend

Enabled	Thread	Color
Dataflow Subsystem		
☑	Thread 1	
☑	Thread 2	
☑	Thread 3	
☑	Thread 4	
	Multiple	

算法多核映射与仿真



算法架构



任务划分

Task Execution Report

SoC Blockset Task Execution Report

Model: soc_beamforming_top

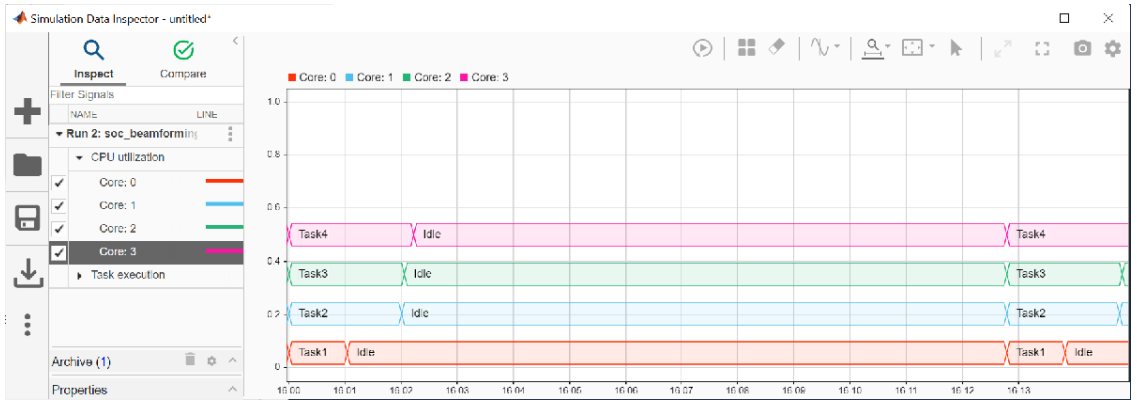
Date: 23-Dec-2022 21:42:03

Task execution statistics

Name	Finished	Min	Mean	Max	SD	Min Turn	Mean Turn	Max Turn
Task1	257	0.0100	0.0121	0.4598	0.0280	0.0100	0.0121	0.4598
Task2	258	0.0197	0.0201	0.0205	4.8354e-05	0.0197	0.0201	0.0205
Task3	258	0.0201	0.0205	0.0210	5.7632e-05	0.0201	0.0205	0.0210
Task4	258	0.0221	0.0222	0.0227	4.1512e-05	0.0221	0.0222	0.0227

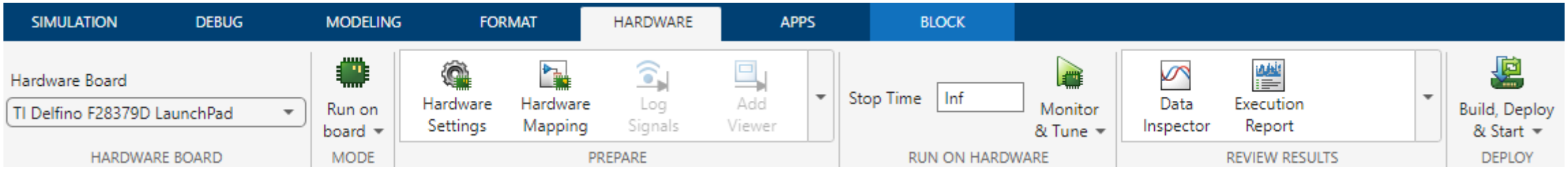
Core usage statistics

Core	Task1	Task2	Task3	Task4	Idle
Core: 0	9.4487	0	0	0	90.5513
Core: 1	0	15.7203	0	0	84.2797
Core: 2	0	0	16.0388	0	83.9612
Core: 3	0	0	0	17.4174	82.5826

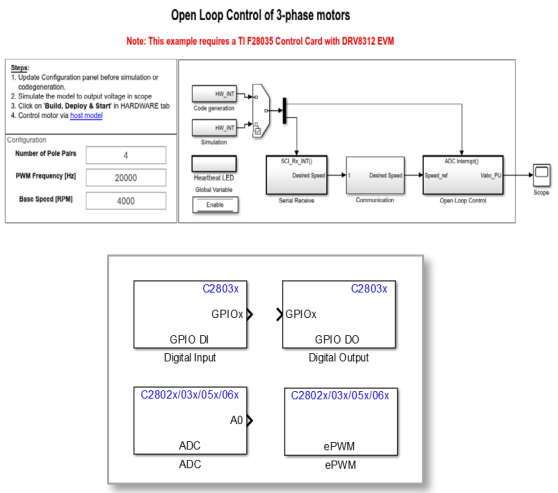


仿真分析

多核DSP部署 – C2000



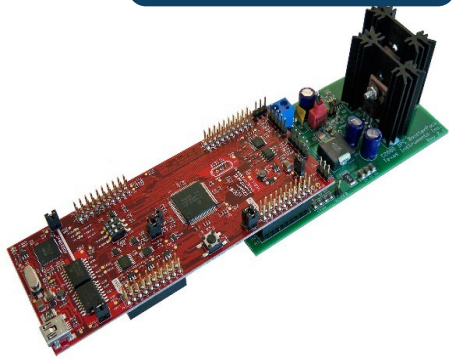
Simulink Model

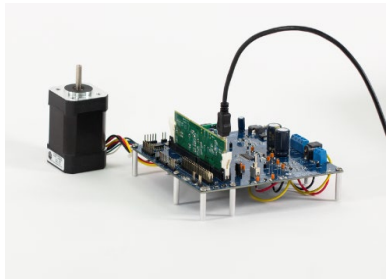


Embedded Coder

CCS Project

Run on C2000





FPGA设计流程

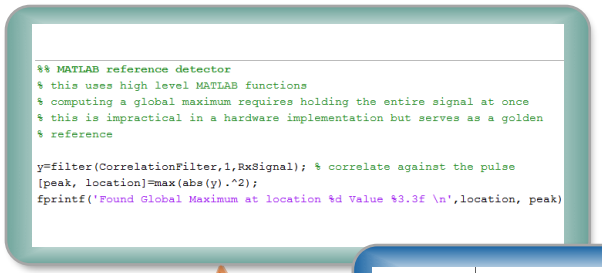
MATLAB
参考算法

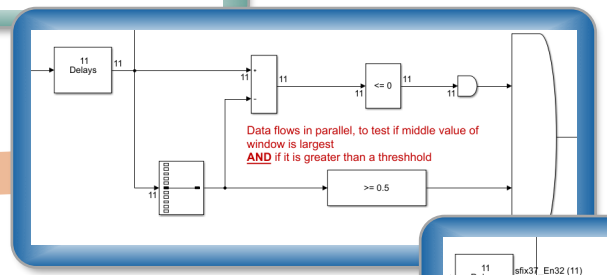
硬件架构

定点实现

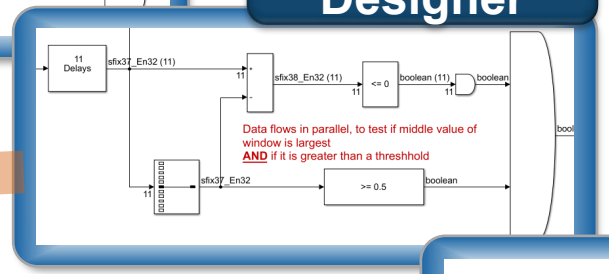
HDL代码
生成和优化

HDL验证和部署



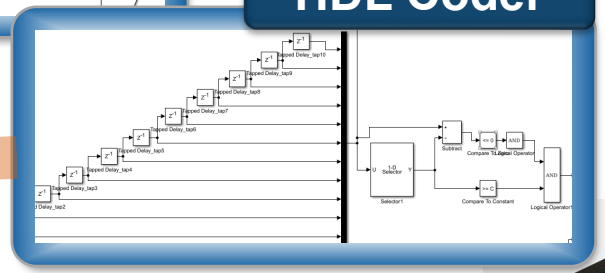


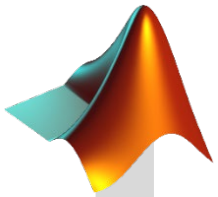
Fixed Point Designer



逐级验证

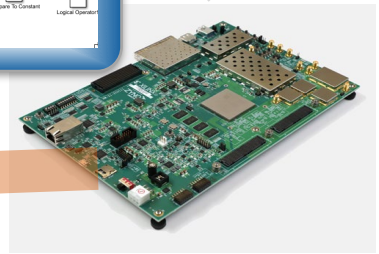
HDL Coder





MATLAB

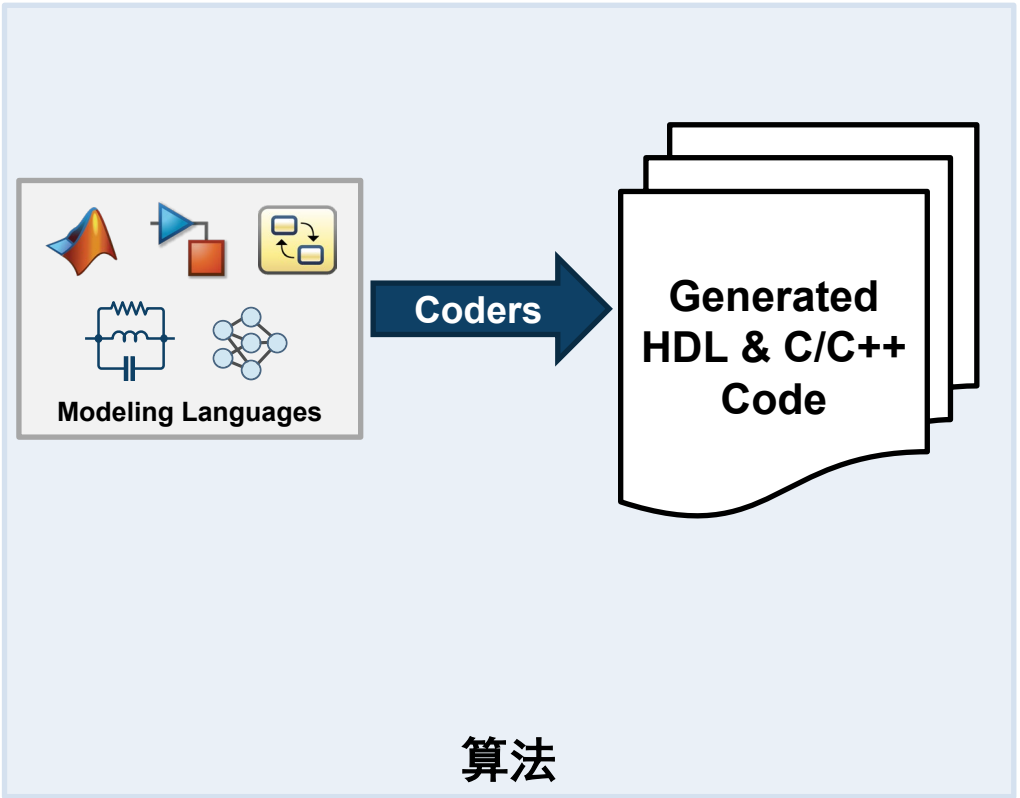
Simulink



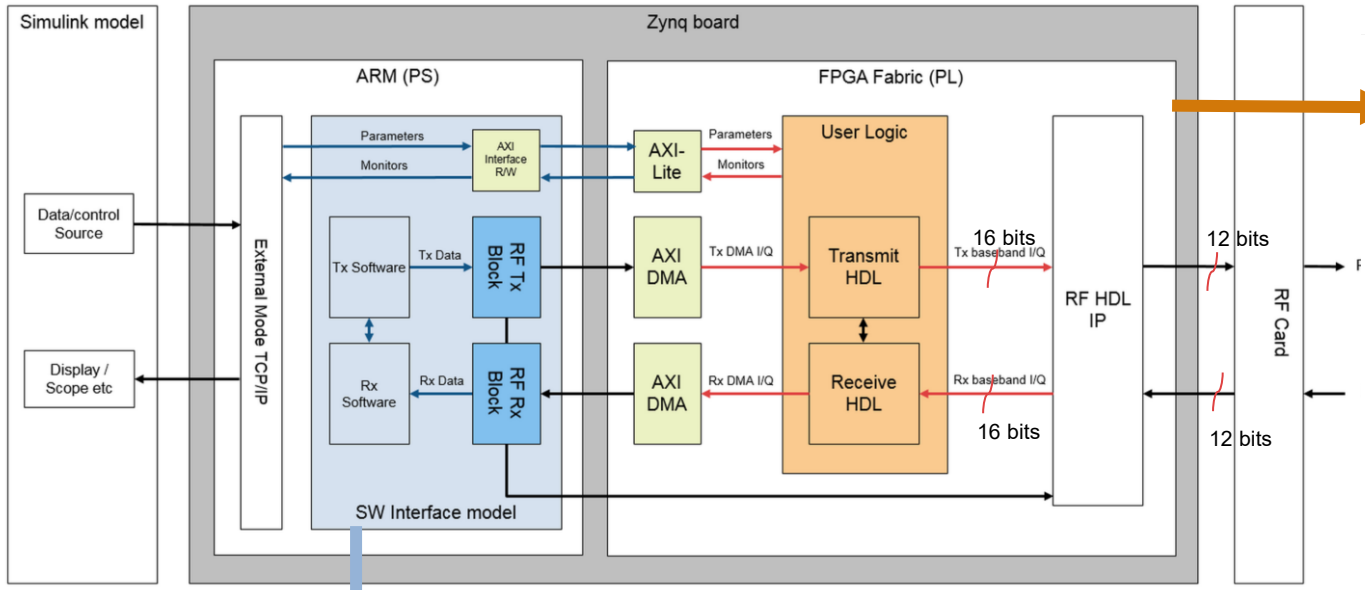
软硬件联合设计

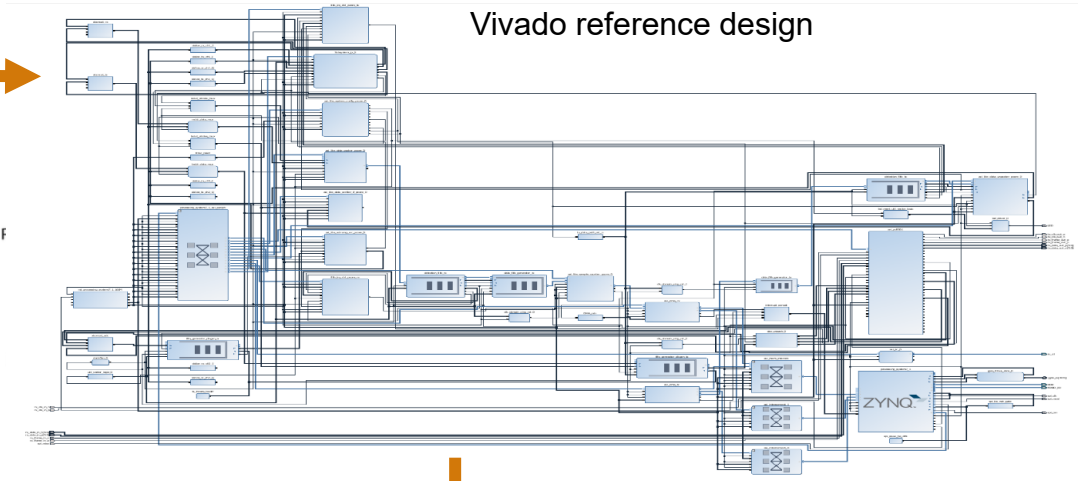
将生成的HDL代码集成到FPGA工程
将生成的C代码集成到嵌入式工程

让算法在实际硬件板卡上运行起来



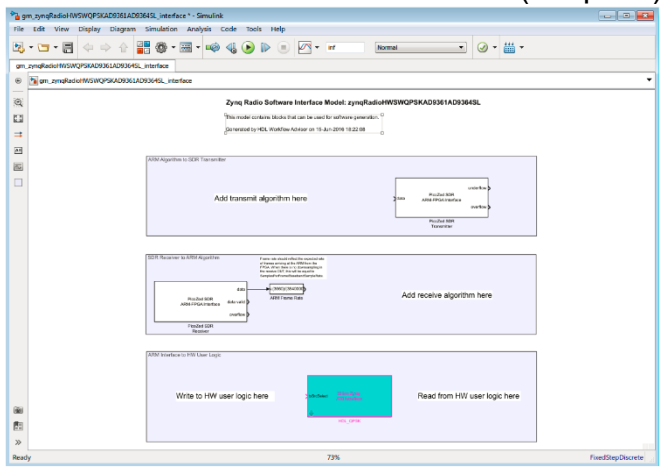
软硬件联合设计



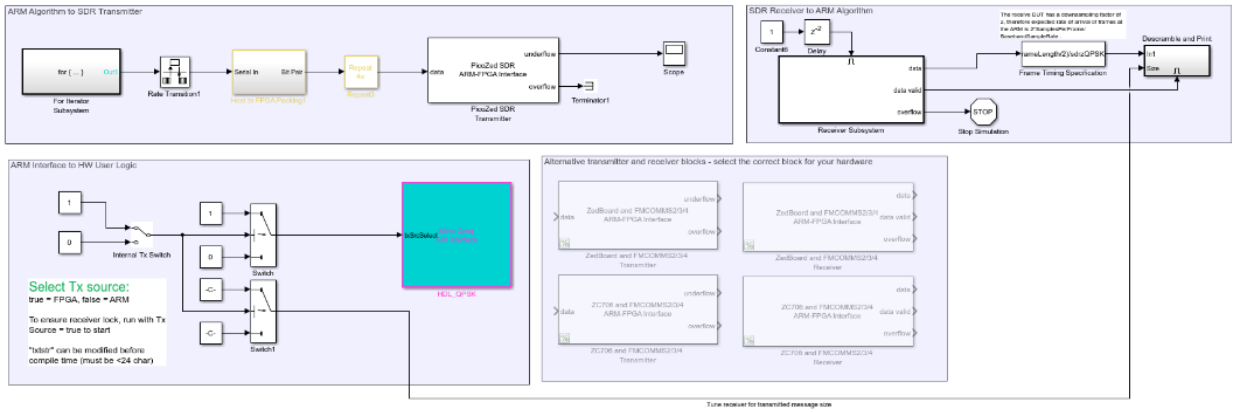


FPGA bitstream

SW interface model (template)



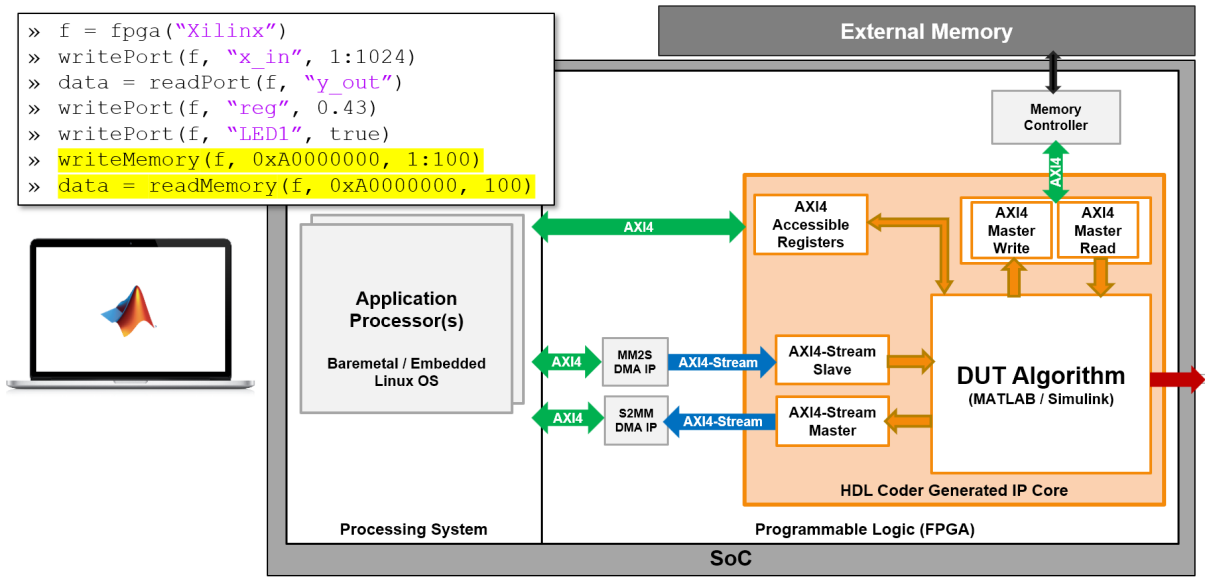
SW interface model (+user logic)



软硬件联合设计功能更新

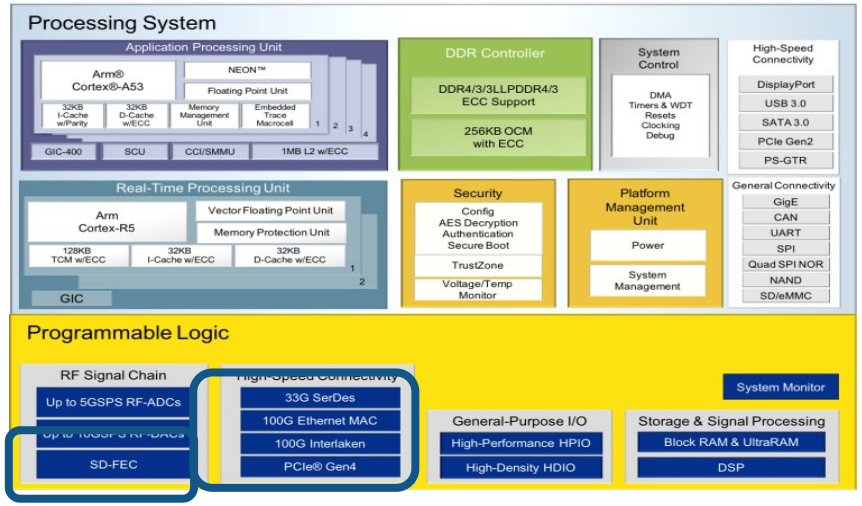
- IP核流程
  - 新增支持生成通用IP核
- 帧模型及部署
  - 将帧信号映射到AXI4-Stream视频接口
  - 将帧延迟映射到外部存储器
- IP核接口
  - AXI4从接口寄存器支持>32位数据类型
  - AXI4主接口支持访问>32位地址位宽
- 硬件平台
  - Xilinx Versal IP核流程参考设计
  - Microchip硬件支持
  - NI硬件支持

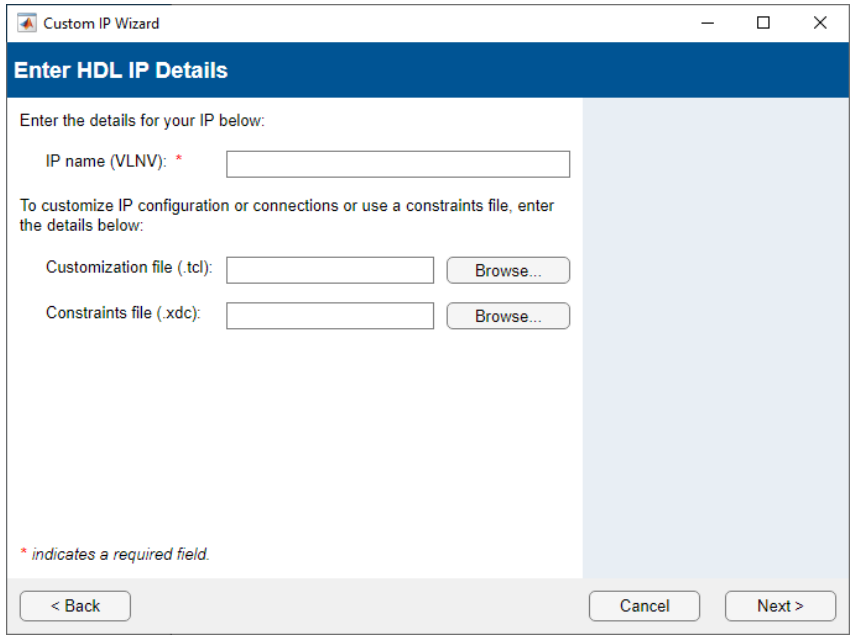
```
» f = fpga("Xilinx")
» writePort(f, "x_in", 1:1024)
» data = readPort(f, "y_out")
» writePort(f, "reg", 0.43)
» writePort(f, "LED1", true)
» writeMemory(f, 0xA0000000, 1:100)
» data = readMemory(f, 0xA0000000, 100)
```



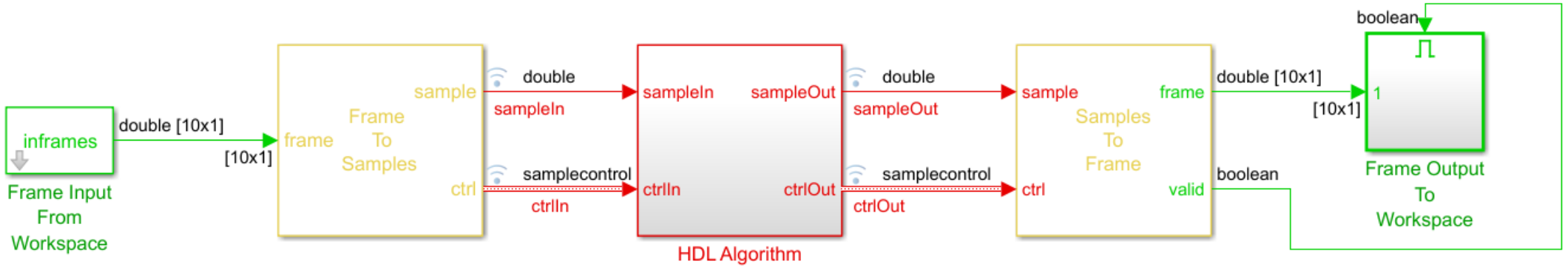
IP 集成

- IP 集成
  - 在 SoC 模型中集成第三方 IP 核
  - 从用户输入生成 SoC 模块
  - 向导式 IP 集成界面
- 使用场景
  - 集成高速外设 – PCIe, 100G Ethernet, 150G Interlaken and GTH
  - 集成第三方 IP – DL IP, RF 前端控制 IP
  - 集成 Xilinx IP – SPI, SDFEC
- 支持定制
  - 支持 Crebrus RFSoC
  - 支持 Aurora IP 集成

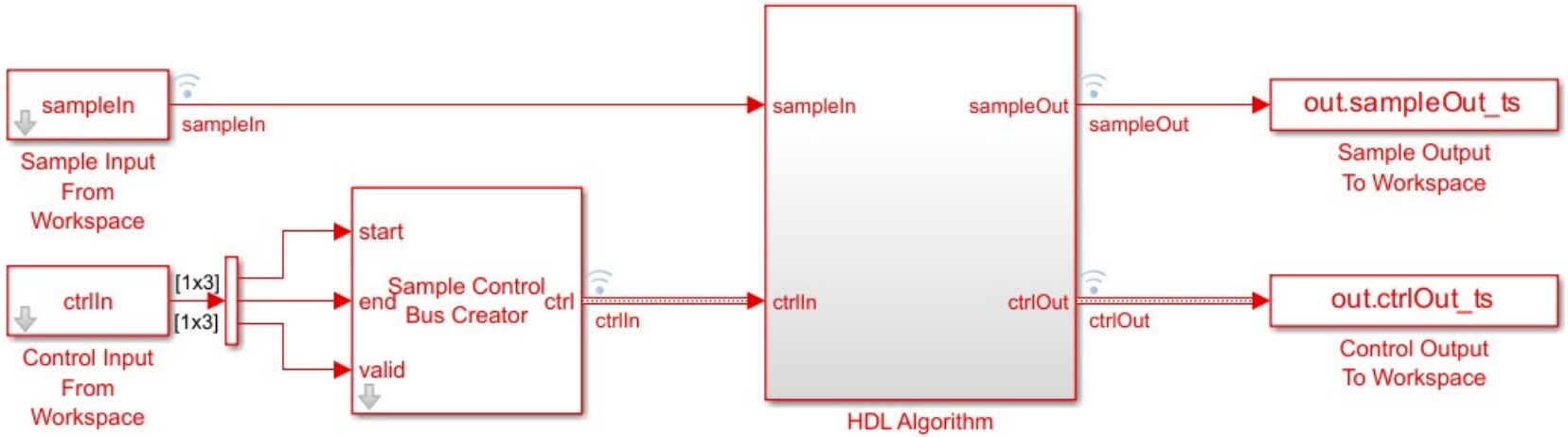




从模板创建无线通信HDL模型

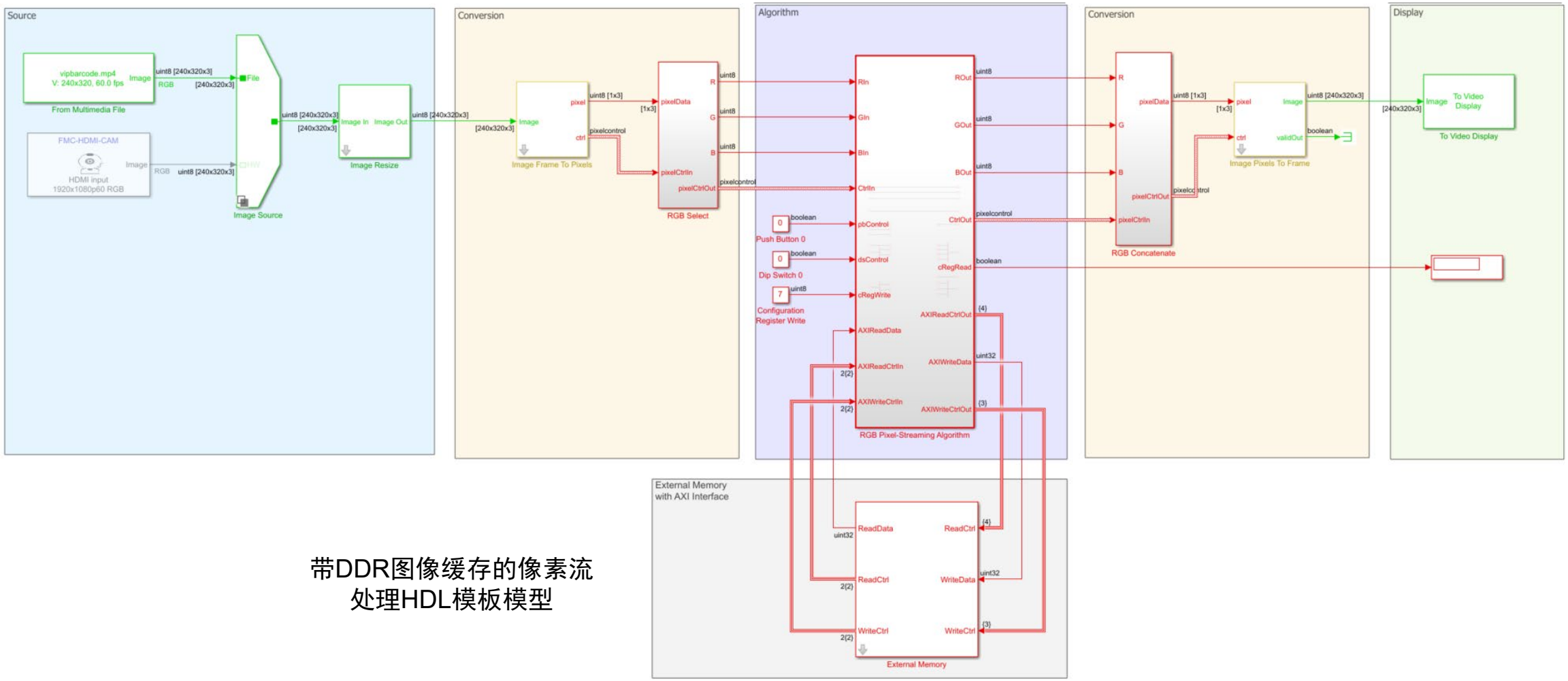


信号帧输入/输出模板模型



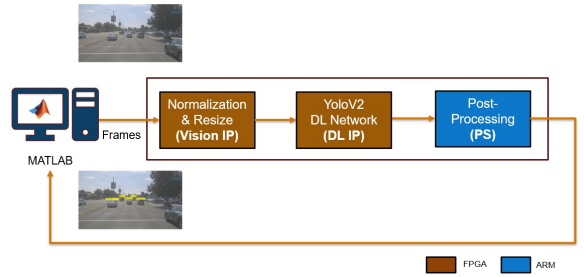
信号流输入/输出模板模型

从模板创建图像处理HDL模型

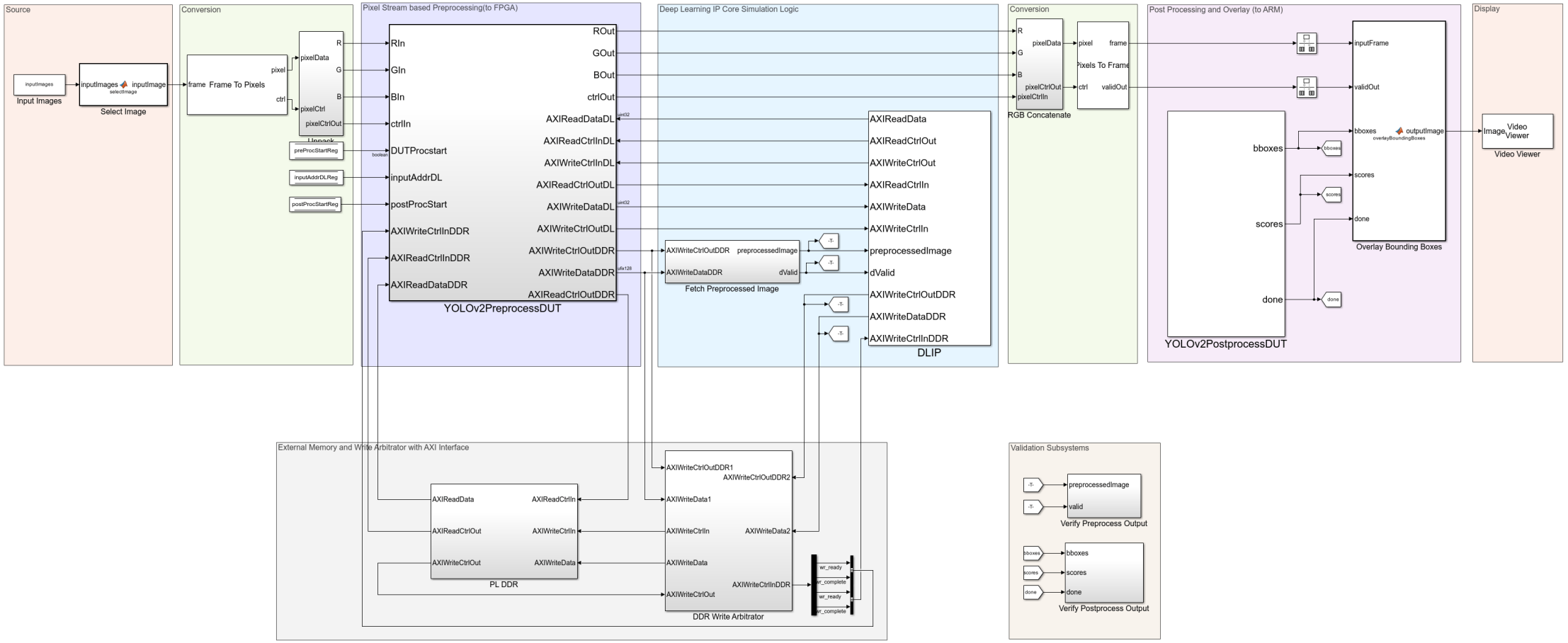


带DDR图像缓存的像素流
处理HDL模板模型

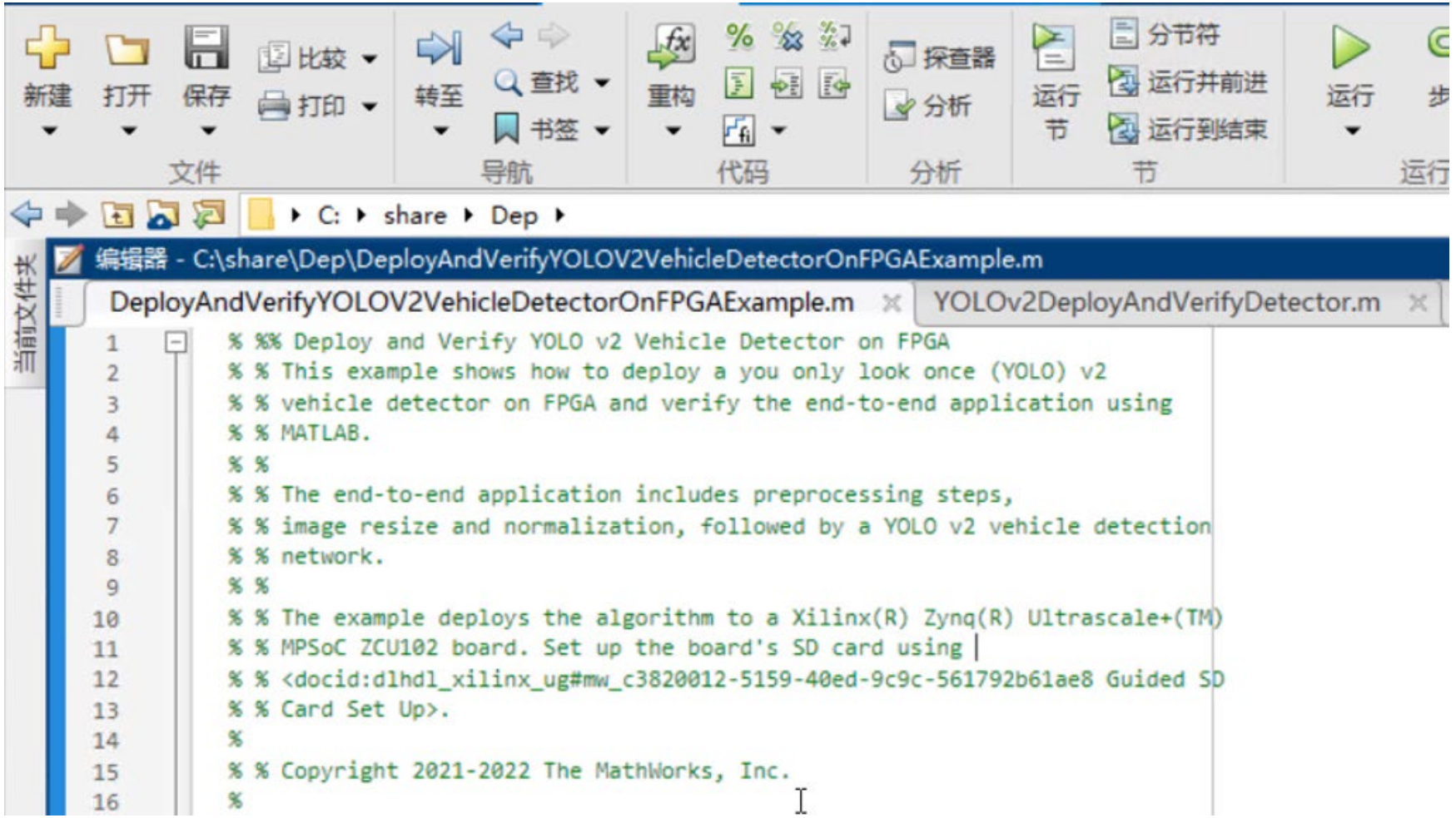
深度学习FPGA部署



YOLO v2 vehicle detector on SoC - Preprocess and Postprocess with deep learning handshake logic



深度学习FPGA部署示例



MATLAB EXPO

谢 谢