

MATLAB EXPO

MATLAB和Simulink在电路仿真中的应用

周前程



赵晨星

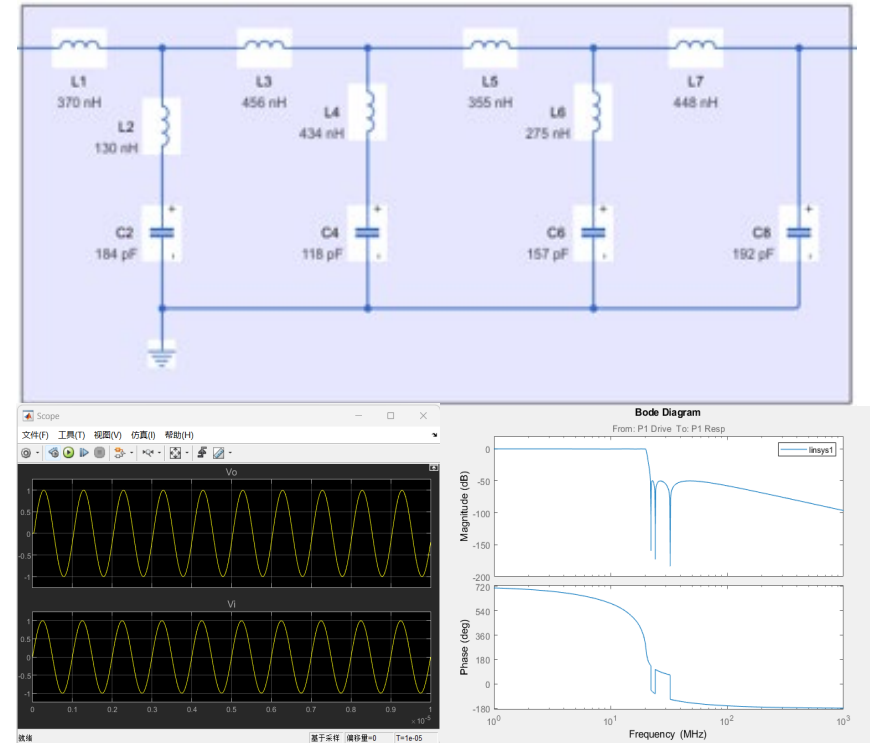


Agenda

- 基于 Simscape 的电路仿真
- 射频电路仿真
- 高速电路信号完整性仿真

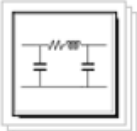
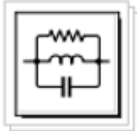

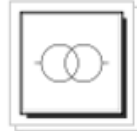
















基于 Simscape 的电路仿真

- Simscape 特性
 - 基于原理图建模
 - 时域仿真 + 频域分析
 - 多物理域 + 控制系统仿真
 - 开放的自定义元件与物理域接口







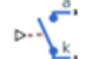















电气元件库






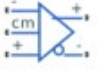

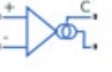
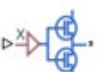


无源器件

			
Lines	RLC Assemblies	Thermal	Transformers
			
Capacitor	Constant Power Load	Crystal	Diffusion Resistor
			
Eddy Current	Incandescent Lamp	Inductor	Nonlinear Inductor
			
Nonlinear Reluctance	Passive Harmonic Filter (Three-Phase)	Potentiometer	Resistor
			
Supercapacitor	Variable Capacitor	Variable Inductor	Varistor

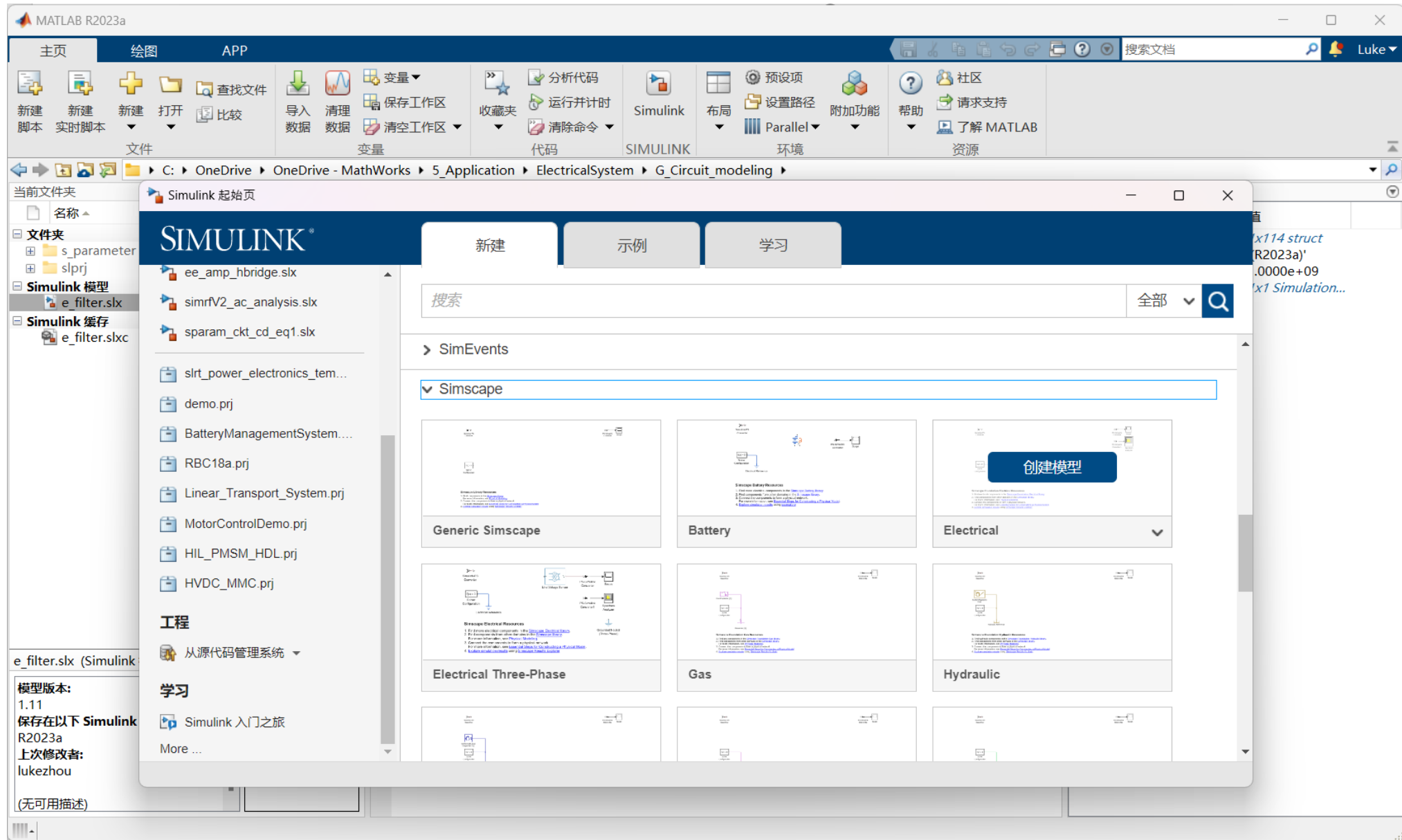
半导体器件

			
Converters	Current Limiter	Diode	Gate Driver
			
GTO	Half-Bridge Driver	Ideal Semiconductor Switch	IGBT (Ideal, Switching)
			
MOSFET (Ideal, Switching)	N-Channel IGBT	N-Channel JFET	N-Channel LDMOS FET
			
N-Channel MOSFET	NPN Bipolar Transistor	Optocoupler	P-Channel JFET
			
Channel LDMOS FET	P-Channel MOSFET	PNP Bipolar Transistor	Thyristor

IC

	
Logic	Band-Limited Op-Amp
	
Comparator	Controlled PWM Voltage
	
Finite-Gain Op-Amp	Fully Differential Op-Amp
	
Multiplier	Operational Transconductance Amplifier
	
Push-Pull Output	Timer
	
Voltage-Controlled Oscillator	

建立电路模型



添加元件到模型中

The screenshot displays the Simulink software interface. At the top, there is a menu bar with options: 仿真 (Simulation), 调试 (Debug), 建模 (Modeling), 格式 (Format), and APP. Below the menu bar is a toolbar with various icons for file operations (新建, 打开, 保存, 打印), library access (库浏览器), signal recording (记录信号), adding viewers (添加查看器), signal table (信号表), simulation control (步退, 运行, 步进, 停止), and data checking (数据检查器). The main workspace is divided into two panes. The left pane is the '库浏览器' (Library Browser) showing a tree structure of libraries: Robotics System Toolbox, Robust Control Toolbox, ROS Toolbox, Sensor Fusion and Tracking Toolbox, SerDes Toolbox, SimEvents, and Simscape. Under Simscape, the 'Foundation Library' is expanded to 'Electrical', and 'Electrical Elements' is further expanded. A 'Capacitor' component is highlighted with a blue border. An orange arrow labeled '拖拽' (Drag) points from the Capacitor icon to the main workspace. The main workspace is labeled 'untitled' and contains a block diagram with a 'Simulink-PS Converter' block, a 'Solver Configuration' block (with $f(x) = 0$), and an 'Electrical Reference' block. An orange box labeled '编辑器' (Editor) is overlaid on the workspace. The right pane shows a 'Scope' and a 'Spectrum Analyzer' block. At the bottom, the status bar shows '73%' zoom and 'VariableStepAuto' simulation mode.

untitled * - Simulink

仿真 调试 建模 格式 APP

新建 打开 保存 打印 文件

库浏览器 库

记录信号 添加查看器 信号表 准备

停止时间 10.0 普通 快速重启 步退 运行 步进 停止 仿真

数据检查器 查看结果

库浏览器

输入搜索词

库 搜索结果

模型库

编辑器

拖拽

Capacitor

Diode

Electrical Reference

Gyrator

Ideal Transformer

Inductor

Simulink-PS Converter

Solver Configuration

Electrical Reference

Scope

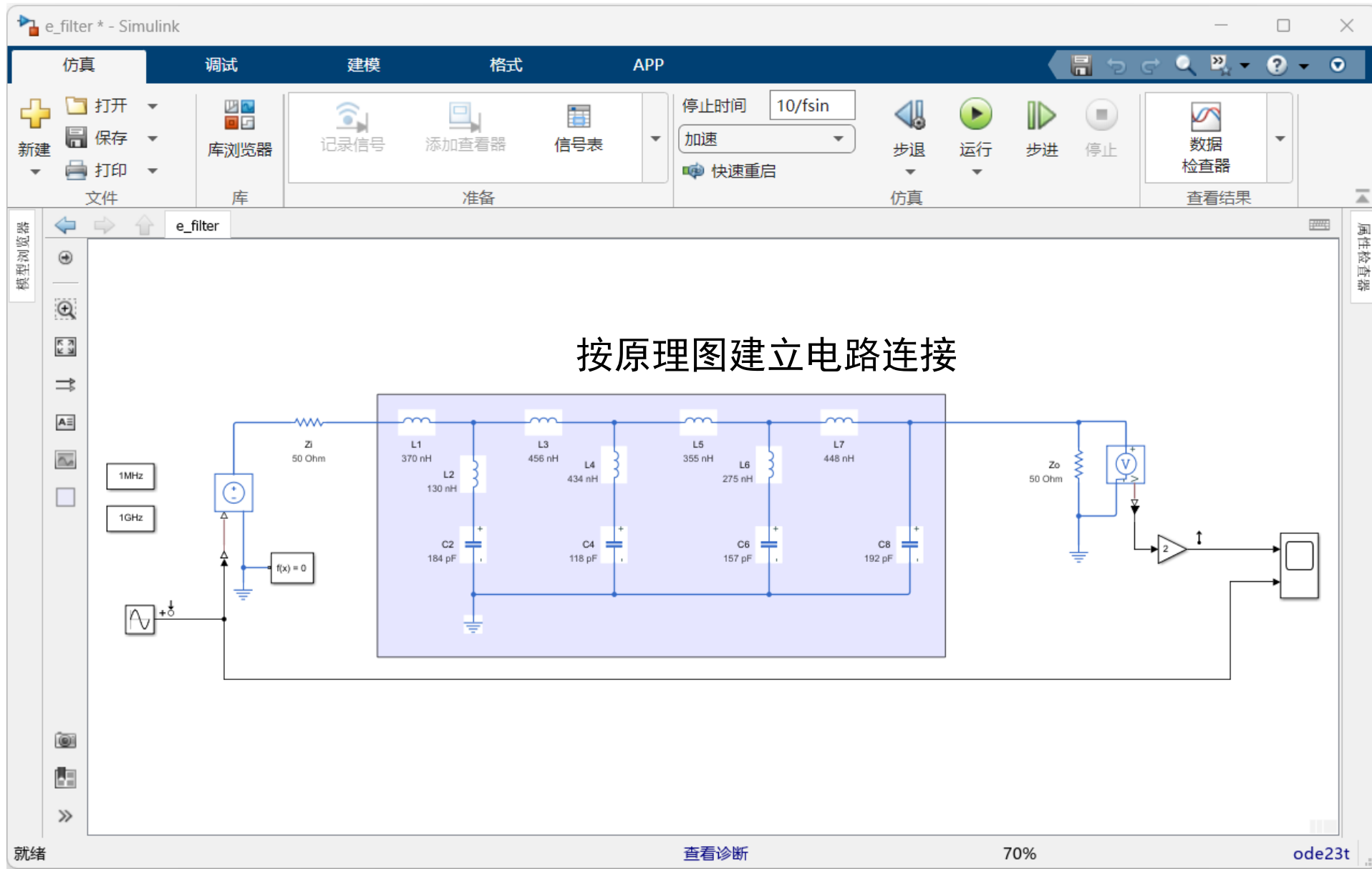
Spectrum Analyzer

Simscape Foundation Electrical Resources

1. Find electrical components in the [Simscape Foundation Electrical library](#).
2. Find components from other domains in the [Simscape library](#). For more information, see [Physical Modeling](#).
3. Connect the components to form a physical network. For more information, see [Essential Steps for Constructing a Physical Model](#).
4. [Explore simulation results](#) using [Simscape Results Explorer](#)

73% VariableStepAuto

建立元件连接关系



设置模块参数

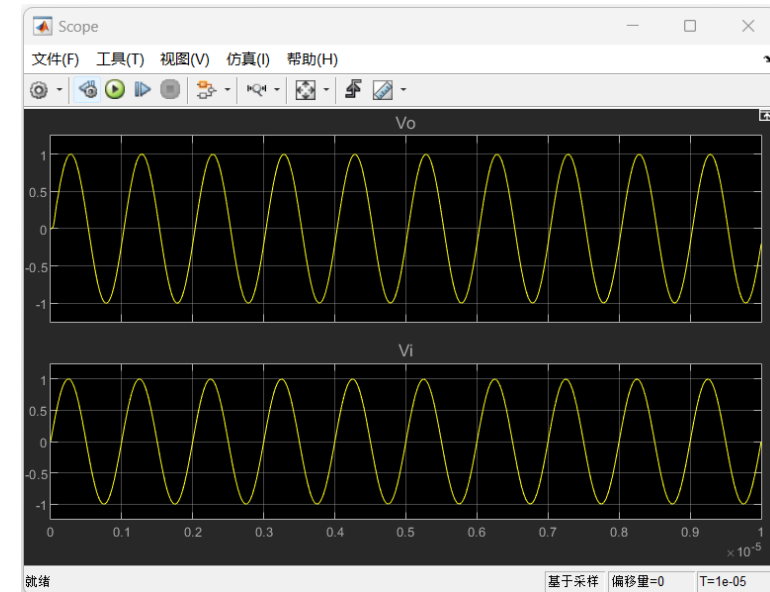
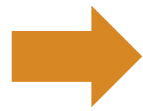
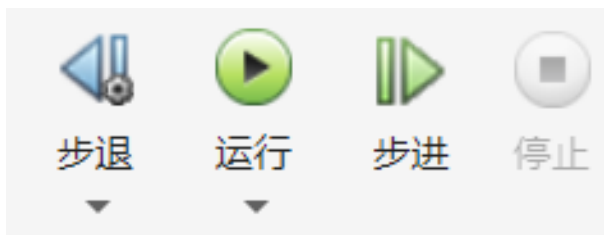
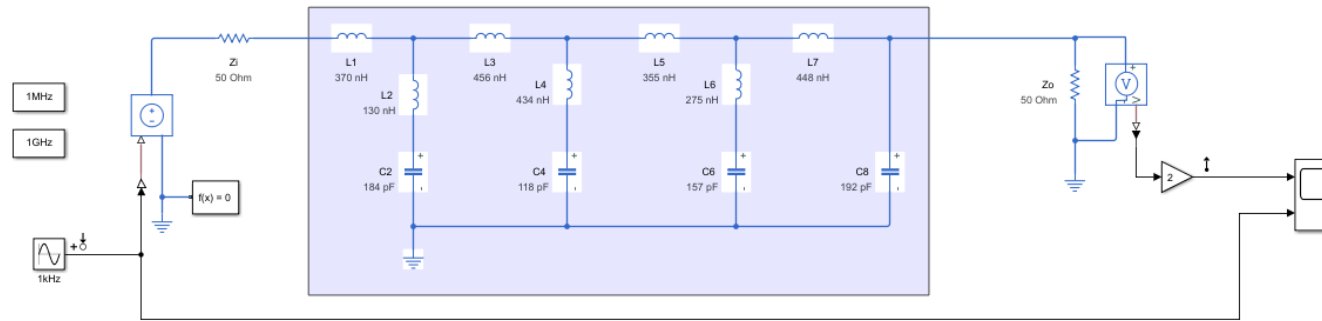
The screenshot displays the Simulink environment with a circuit diagram and a parameter configuration window for an inductor module (L1). The circuit includes a 1MHz and 1GHz signal source, a 50 Ohm resistor (Z1), an inductor (L1, 370 nH), another inductor (L2, 130 nH), and a capacitor (C2, 184 pF). The parameter window for L1 is open, showing the following settings:

名称	值
Main	
> Inductance	370 nH
Tolerance application	None - use nominal value
> Series resistance	0 Ohm
> Parallel conductance	1e-9 1/Ohm
Operating Limits	
Faults	
Initial Targets	
Nominal Values	

The status bar at the bottom indicates the simulation is ready (就绪), the progress is 70%, and the current module is ode23t.

电路分析

- 在Simulink中进行电路分析



仿真 调试 建模 格式 APP

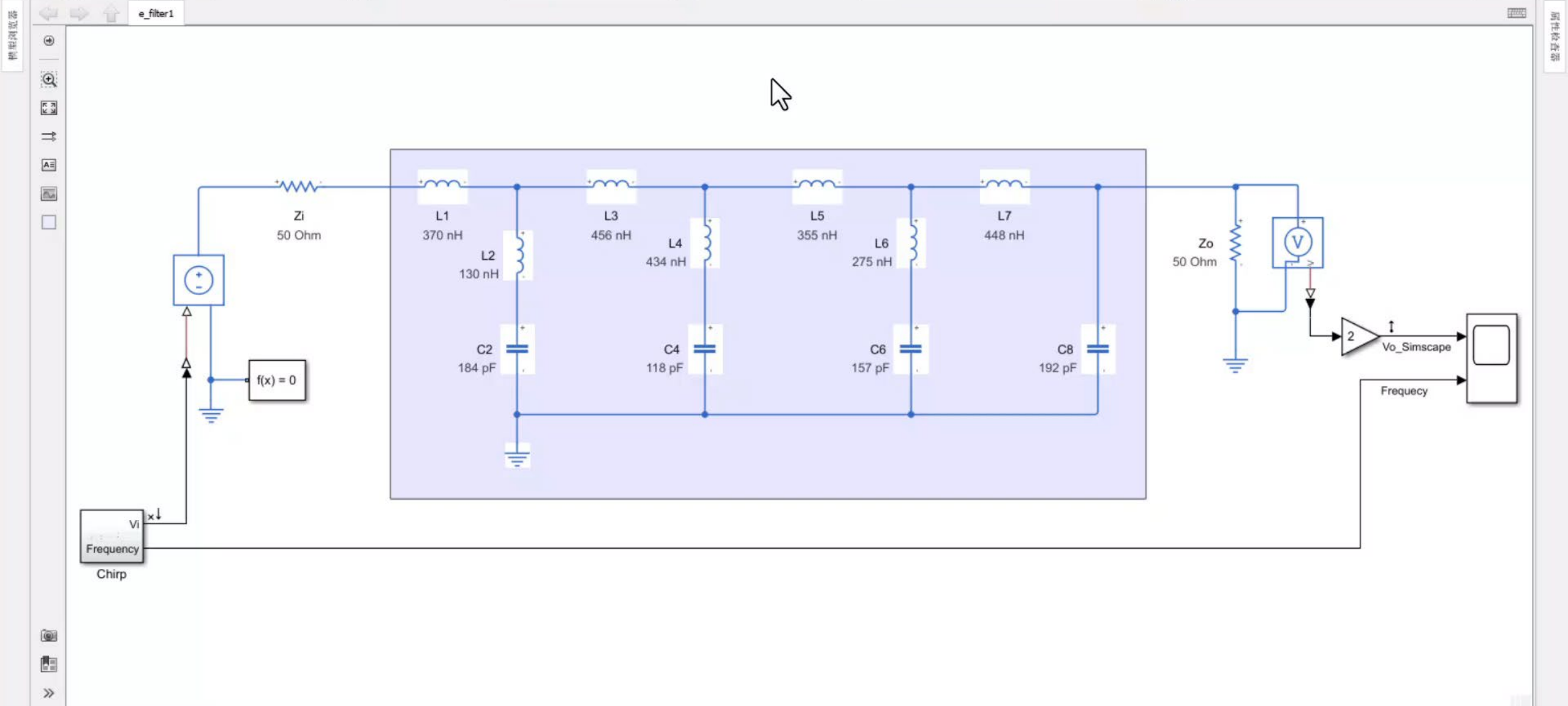
停止时间 0.005

普通

快速重启

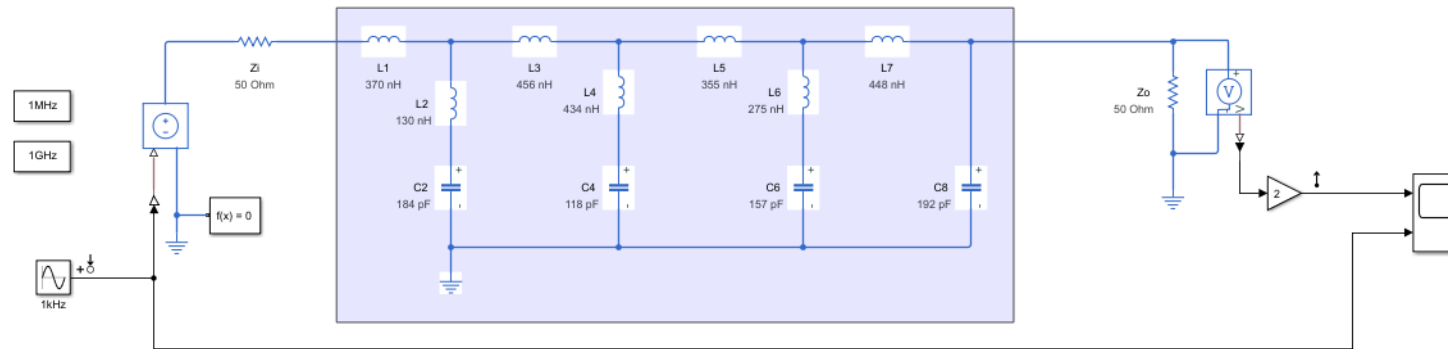
数据检查器 逻辑分析仪 鸟瞰图 仿真管理器

查看结果



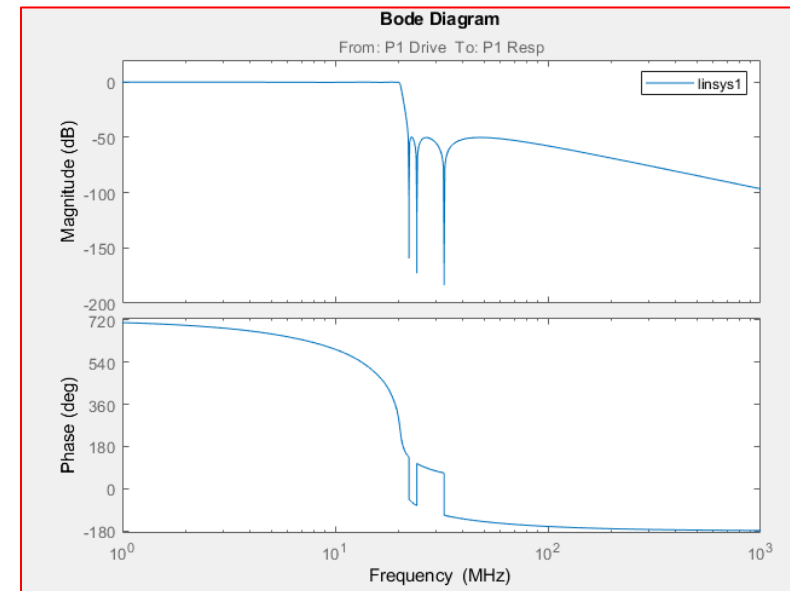
电路分析

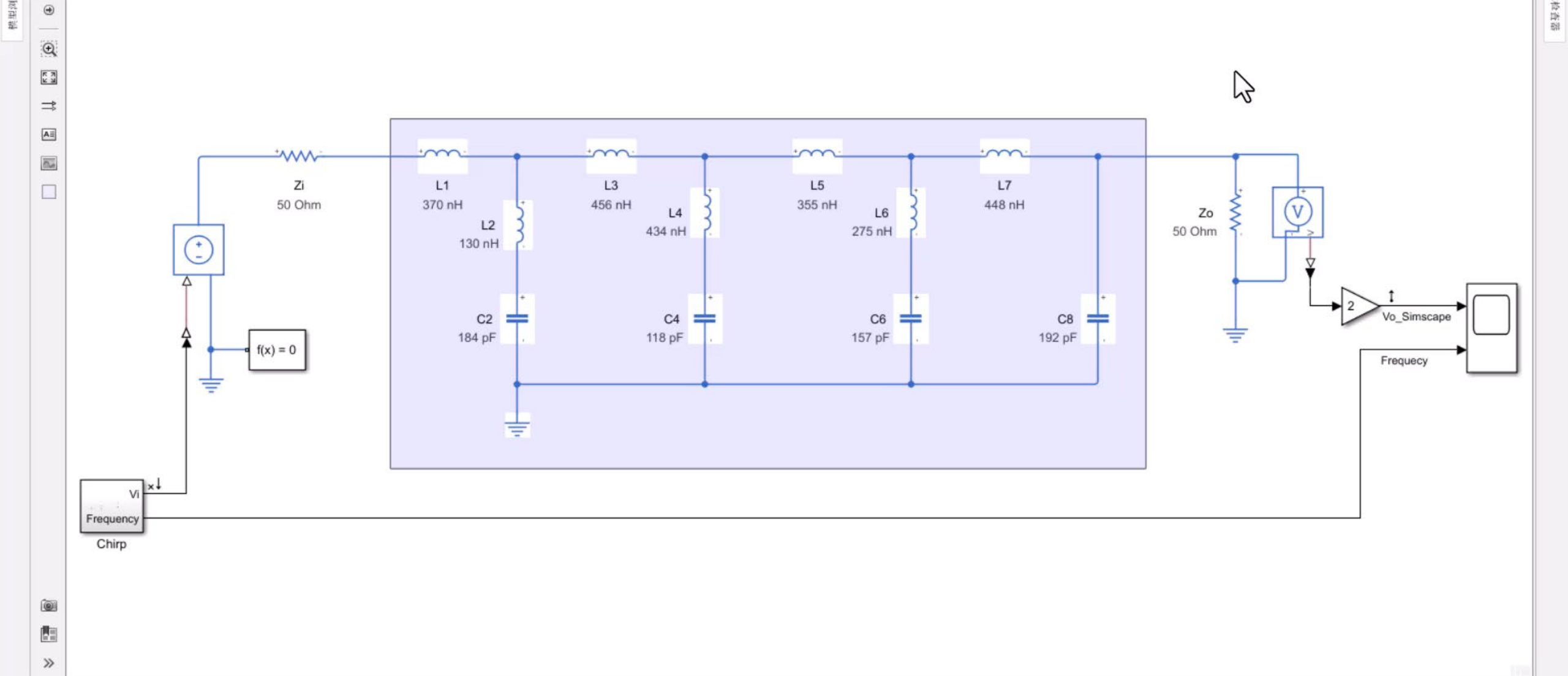
- 在Simulink中进行电路分析



```
io = getlinio(bdroot);
op = operpoint(bdroot);
sys = linearize(bdroot,io,op);
```

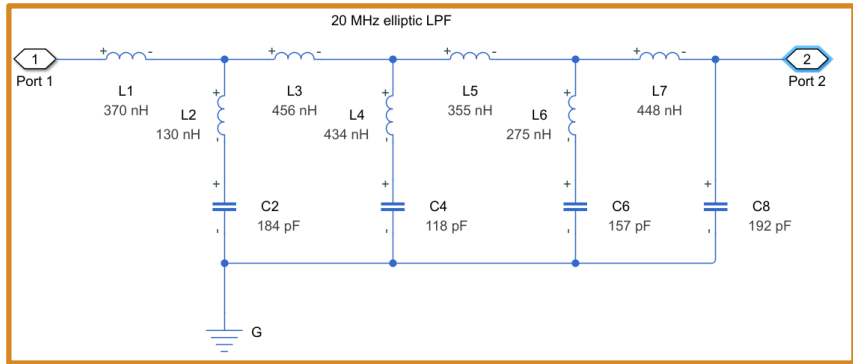
sys contains A,B,C,D state-space matrices





电路分析

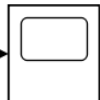
频域与时域仿真对比



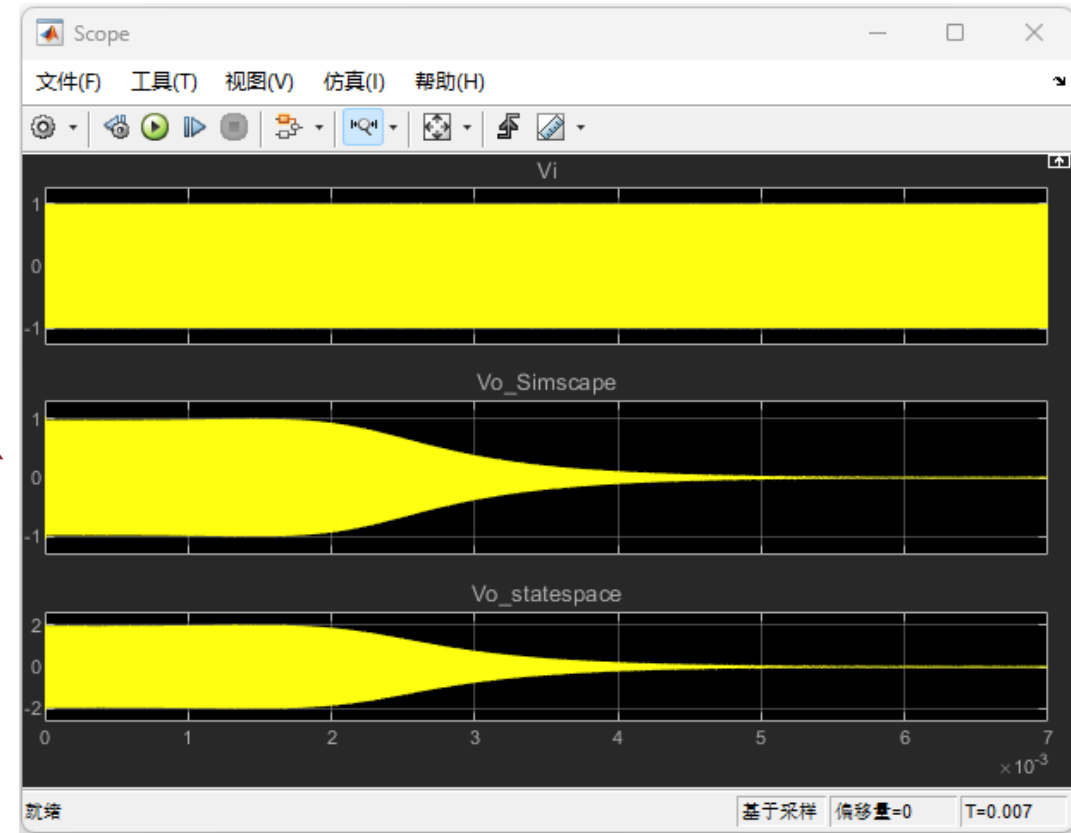
$$\dot{x} = Ax + Bu$$

$$y = Cx + Du$$

State-Space
Version of Elliptic Filter

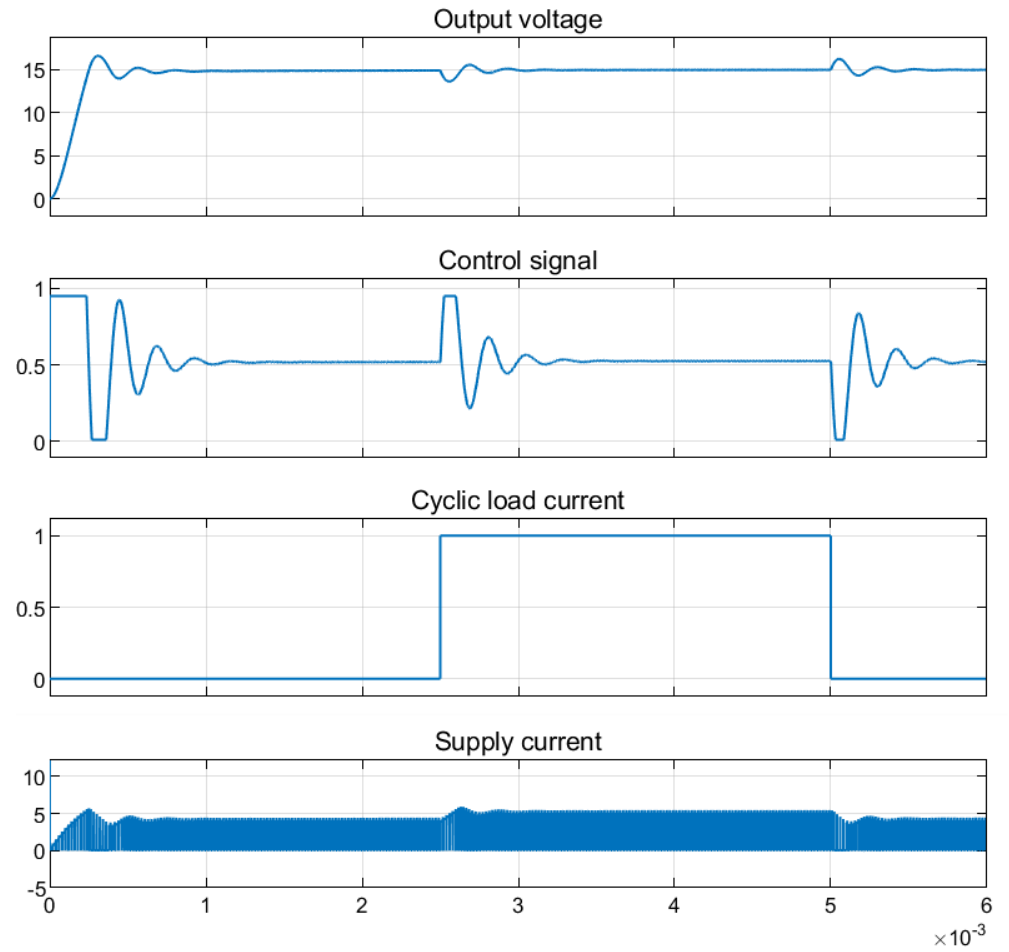
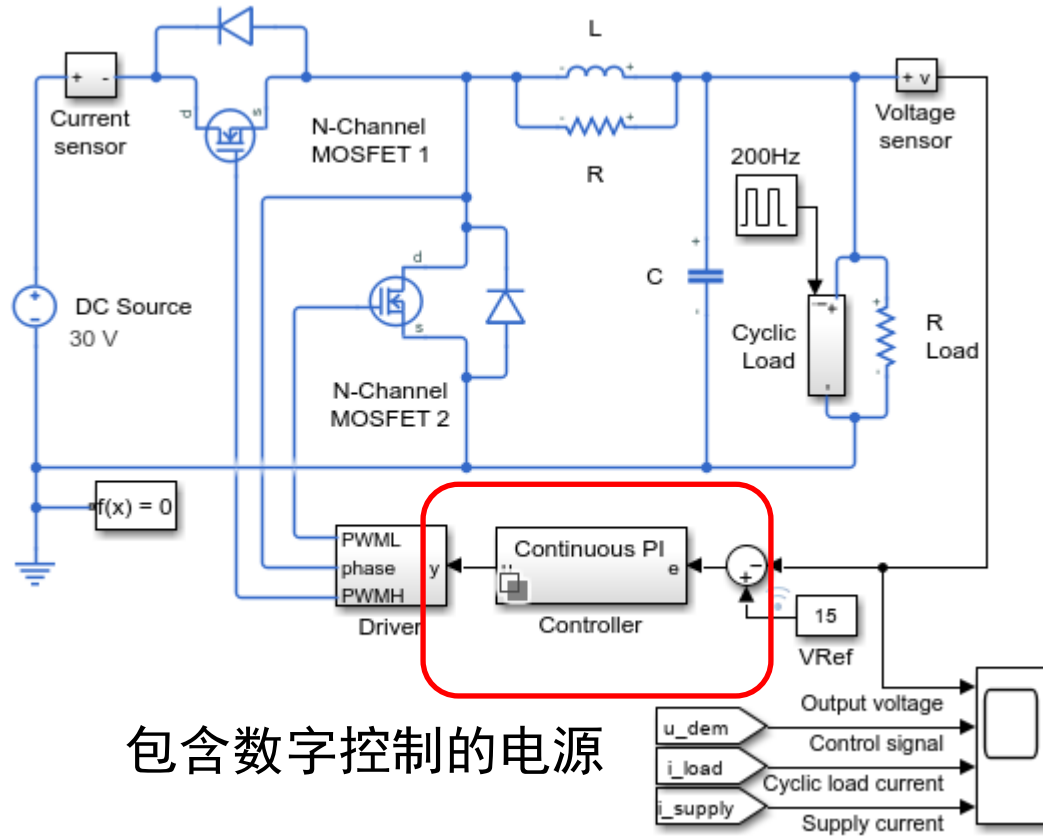


状态方程模型



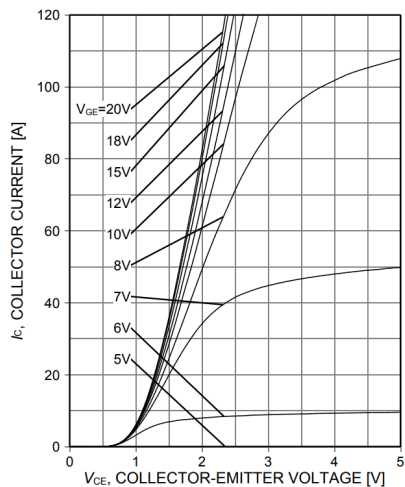
电源系统设计

闭环仿真

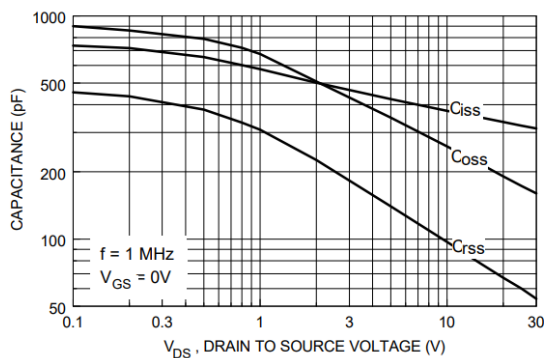


电源系统设计

精细化器件建模



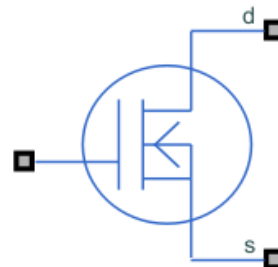
导通特性



开关断特性

从datasheet建模

动态、静态、温升



N-Channel
MOSFET 1

SPICE
Simulator

暂态开关断性能
损耗与温升

利用SPICE Netlist 15

电源系统设计

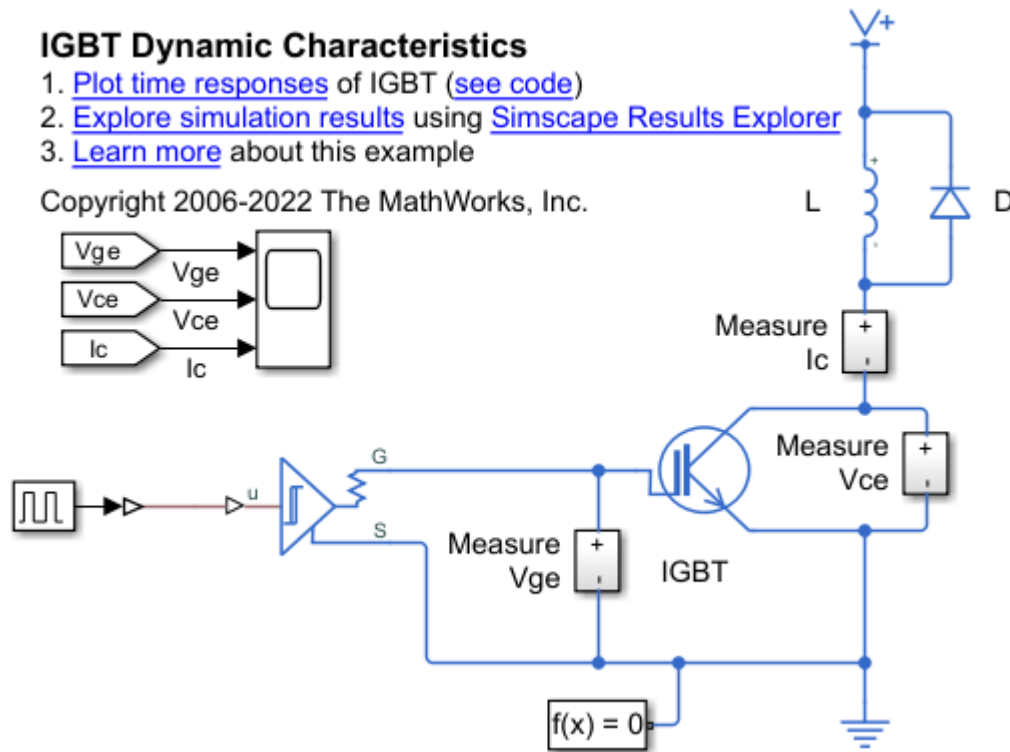
功率器件特性模拟 - 双脉冲测试

驱动与功率器件

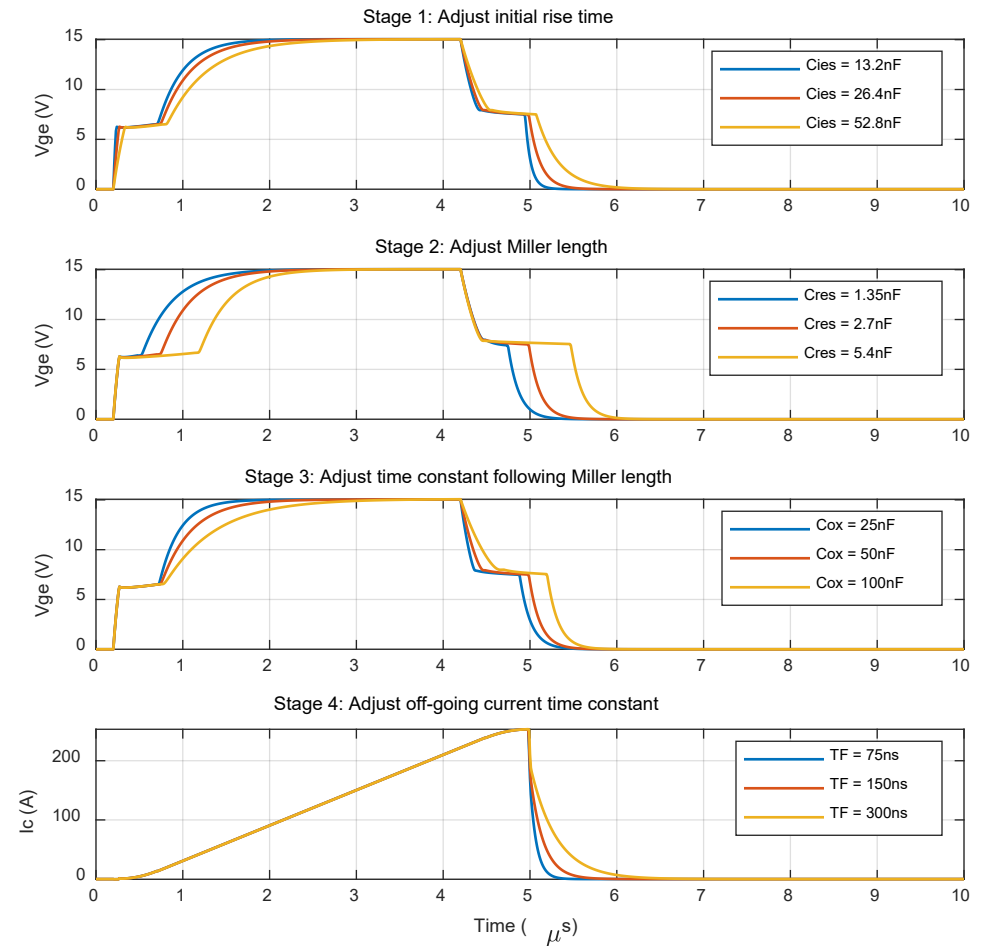
IGBT Dynamic Characteristics

1. [Plot time responses](#) of IGBT ([see code](#))
2. [Explore simulation results](#) using [Simscape Results Explorer](#)
3. [Learn more](#) about this example

Copyright 2006-2022 The MathWorks, Inc.



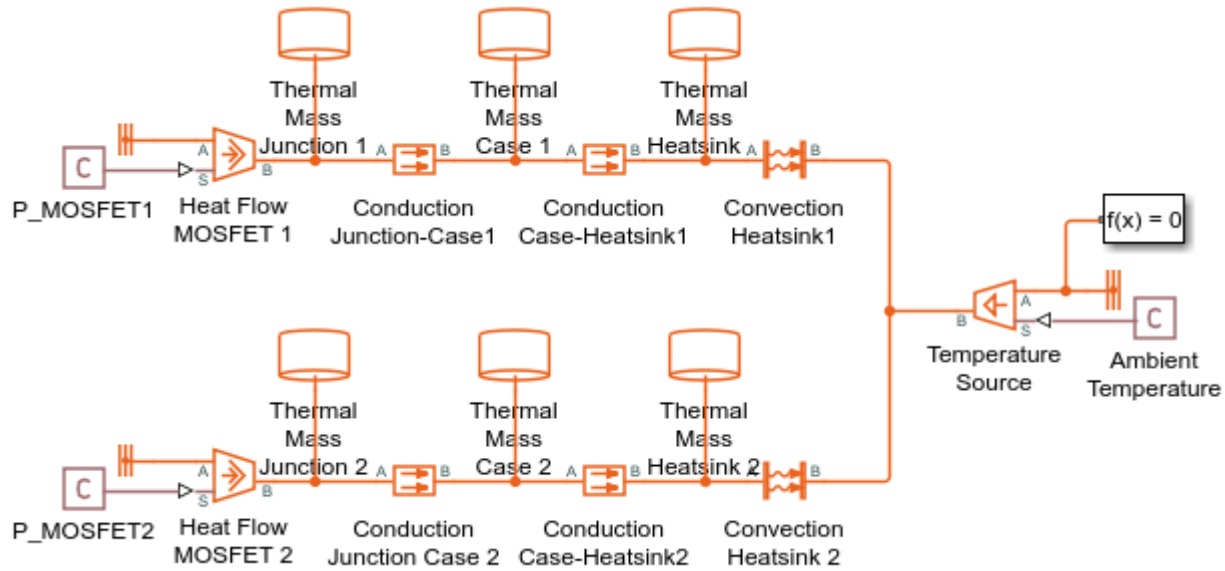
暂态仿真



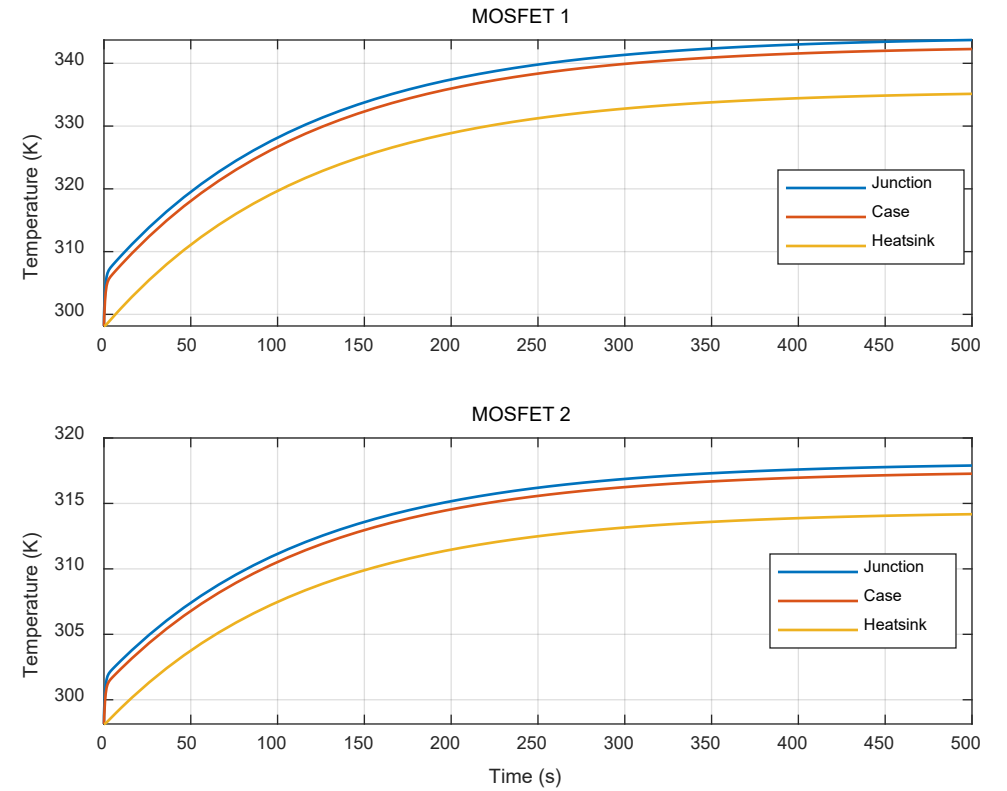
电源系统设计

电源温升建模

散热模型

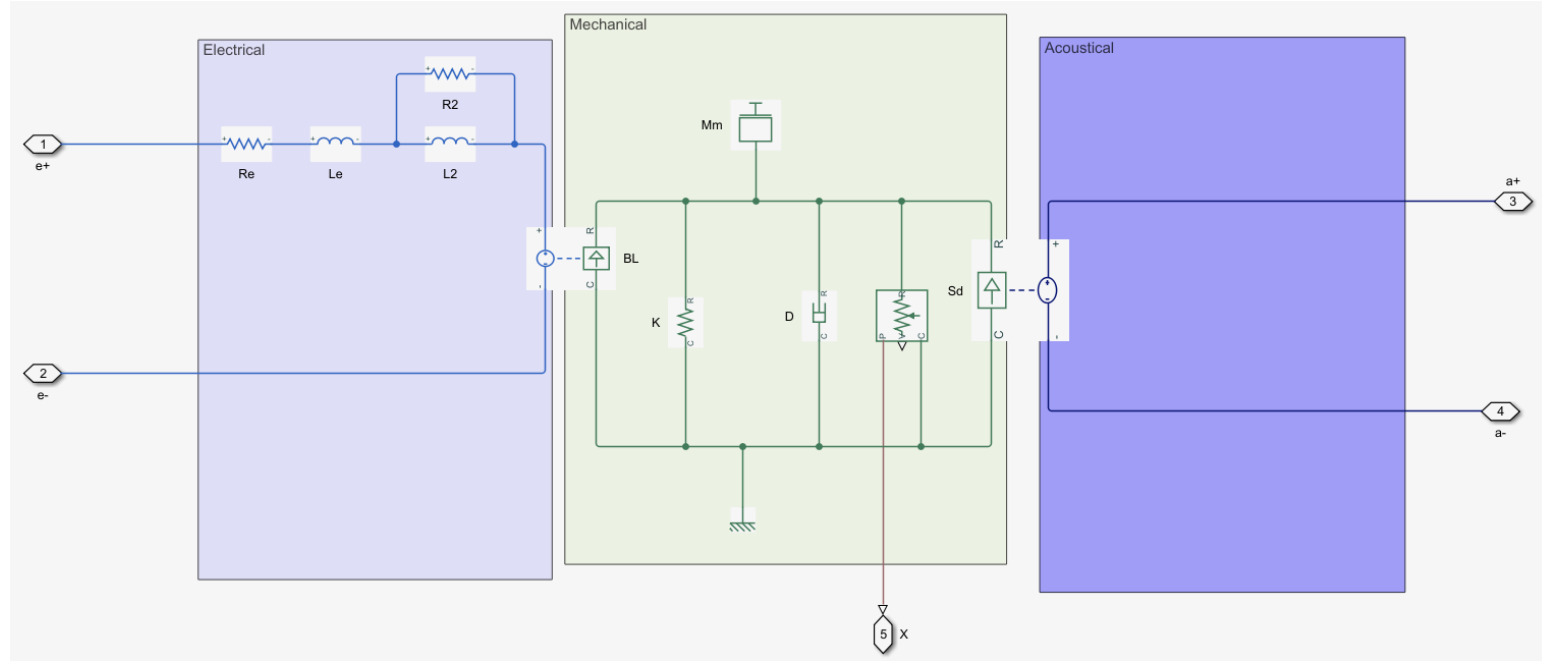
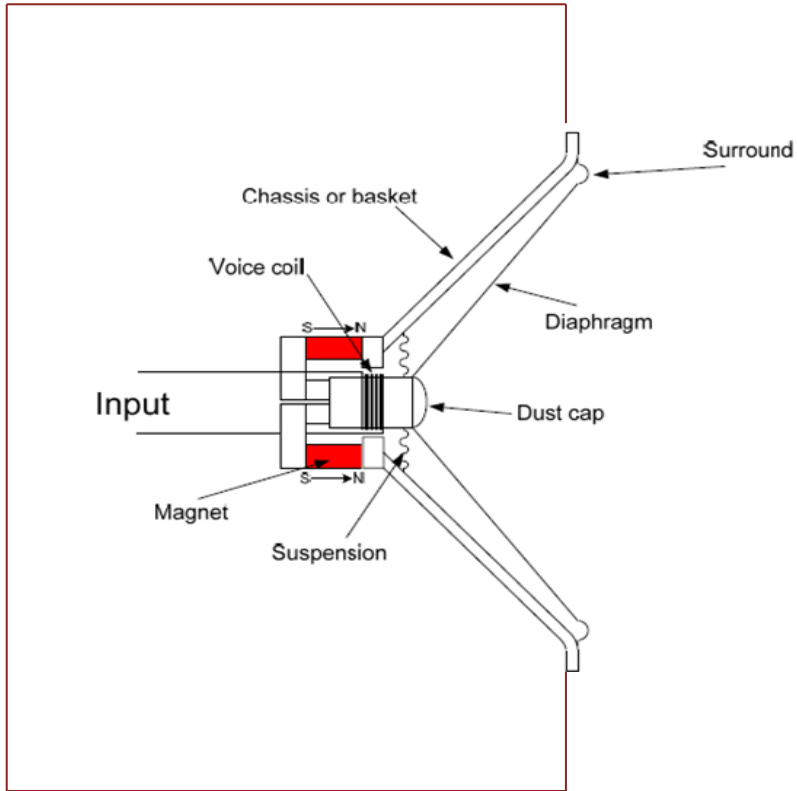


温升仿真



多物理域系统

扬声器

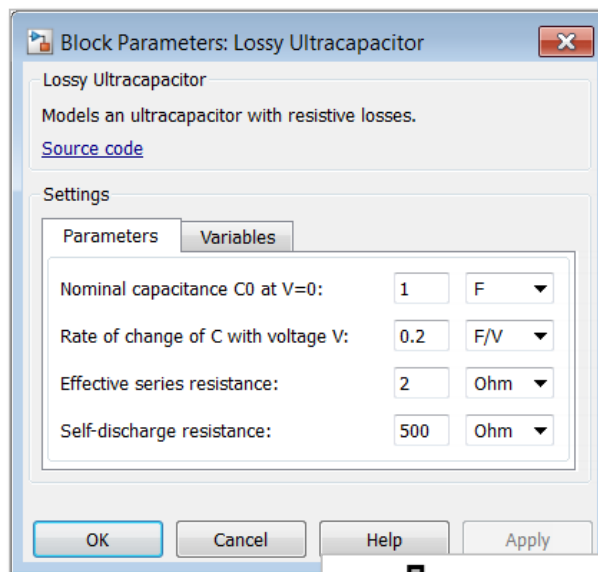


原生支持

Simscape Language
自定义

基于 Simscape Language 自定义元件

- 类MATLAB语言，定义物理域、元件和库
 - 基于MATLAB
 - 面型对象，方便重用
 - 生成Simulink模块
 - 支持二进制 IP 保护



```

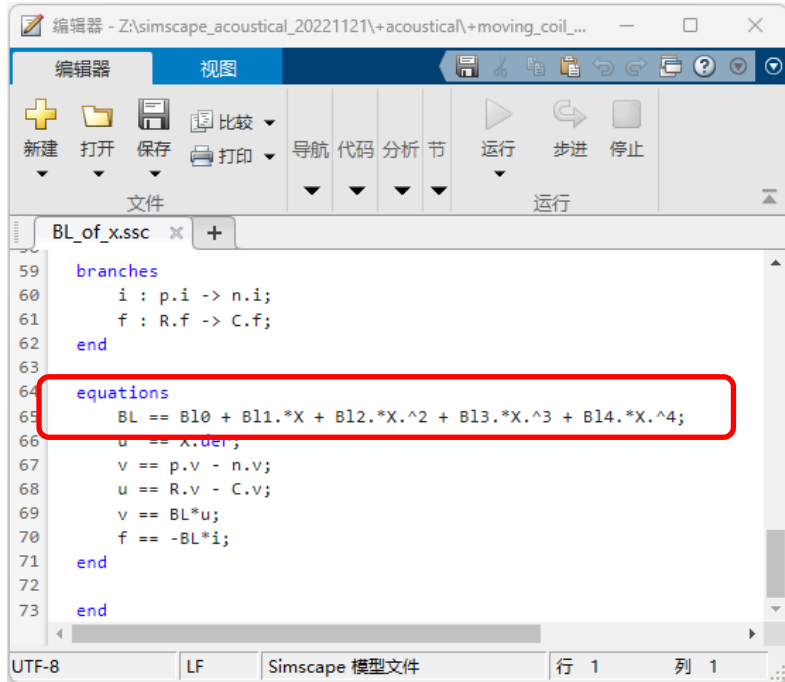
MATLAB
Editor - C:\MyComponents\LossyUltraCapacitor.ssc
1 component LossyUltraCapacitor
2 % Lossy Ultracapacitor
3 % Models an ultracapacitor with resistive losses.
4 nodes
5     p = foundation.electrical.electrical; % +:top
6     n = foundation.electrical.electrical; % -:bottom
7 end
8 parameters
9     C0 = { 1, 'F' }; % Nominal capacitance C0 at V=0
10    Cv = { 0.2, 'F/V' }; % Rate of change of C with voltage V
11    R = { 2, 'Ohm' }; % Effective series resistance
12    Rd = { 500, 'Ohm' }; % Self-discharge resistance
13 end
14 variables
15    i = { 0, 'A' }; % Current through variable
16    v = { 0, 'V' }; % Voltage across variable
17    vc = { 0, 'V' }; % Capacitor voltage
18 end
19 function setup
20     if R <= 0
21         error('Resistance must be greater than zero' )
22     end
23 end
24 branches
25     i : p.i -> n.i; % Through variable i from node p to node
26 end
27 equations
28     v == p.v - n.v; % Across variable v from p to n
29     i == (C0 + Cv*vc)*vc.der + vc/Rd; % Equation 1
30     v == vc + i*R; % Equation 2
31 end
32 end
  
```



Lossy
Ultracapacitor

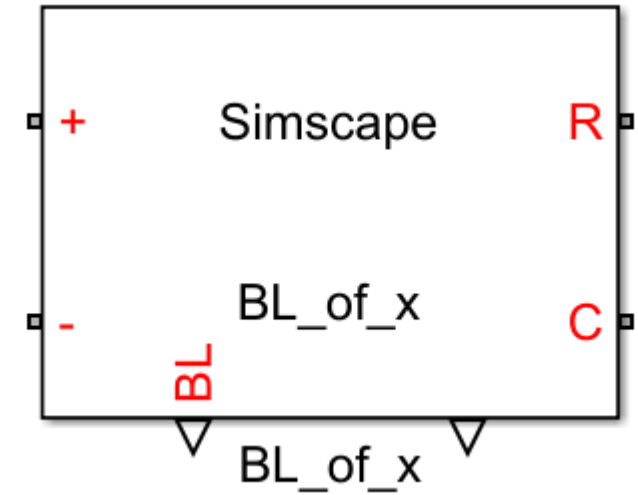
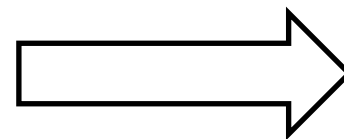
$$i = (C_0 + C_v v) \frac{dv}{dt} + \frac{v}{r_d}$$

自定义非线性互感元件



```
59 branches
60   i : p.i -> n.i;
61   f : R.f -> C.f;
62 end
63
64 equations
65   BL == B10 + B11.*x + B12.*x.^2 + B13.*x.^3 + B14.*x.^4;
66   u == x.der;
67   v == p.v - n.v;
68   u == R.v - C.v;
69   v == BL*u;
70   f == -BL*i;
71 end
72
73 end
```

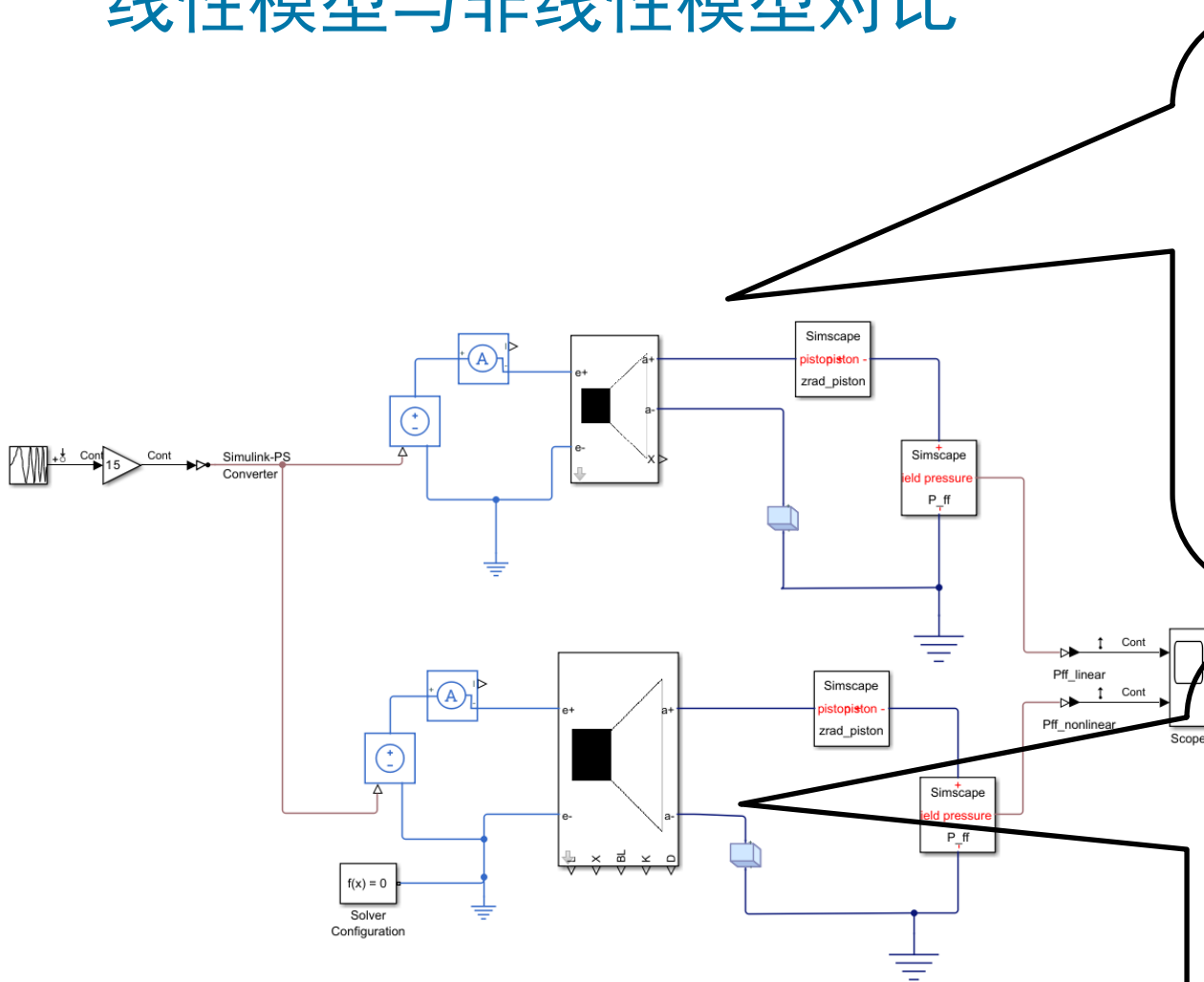
ssc_build



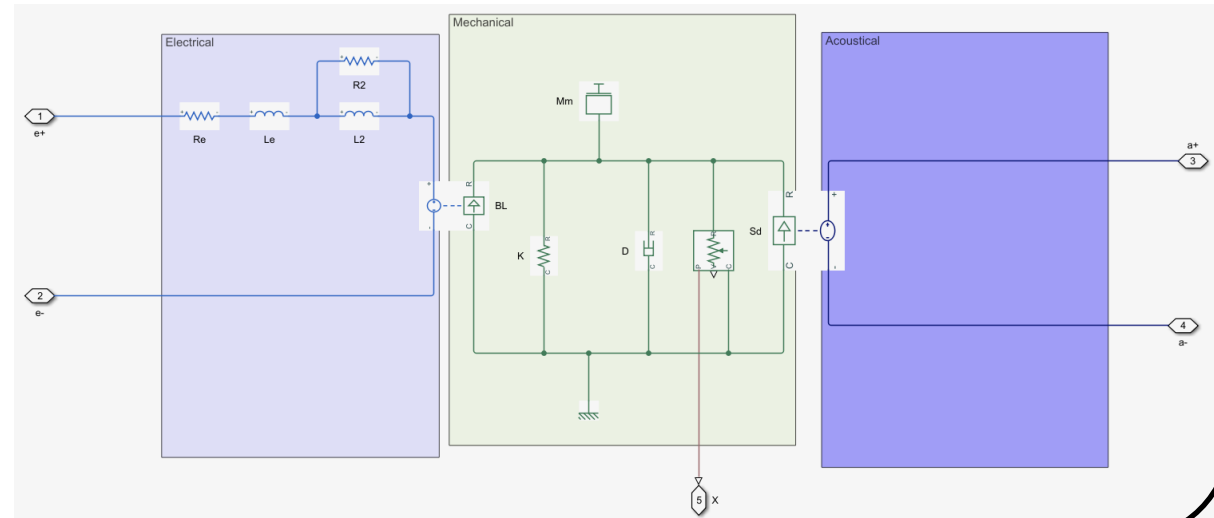
Simscape 语言定义模块方程

生成自定义互感模块

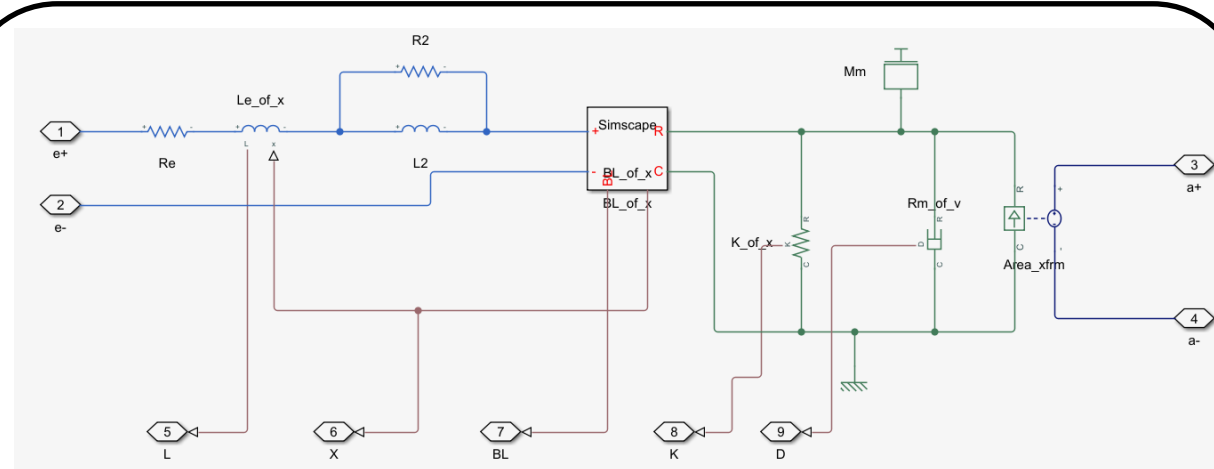
线性模型与非线性模型对比



线性模型

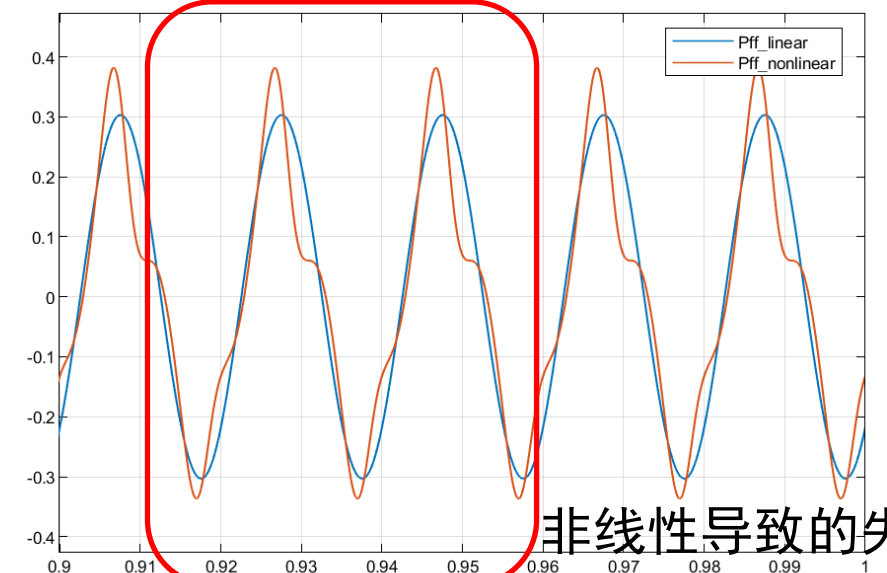
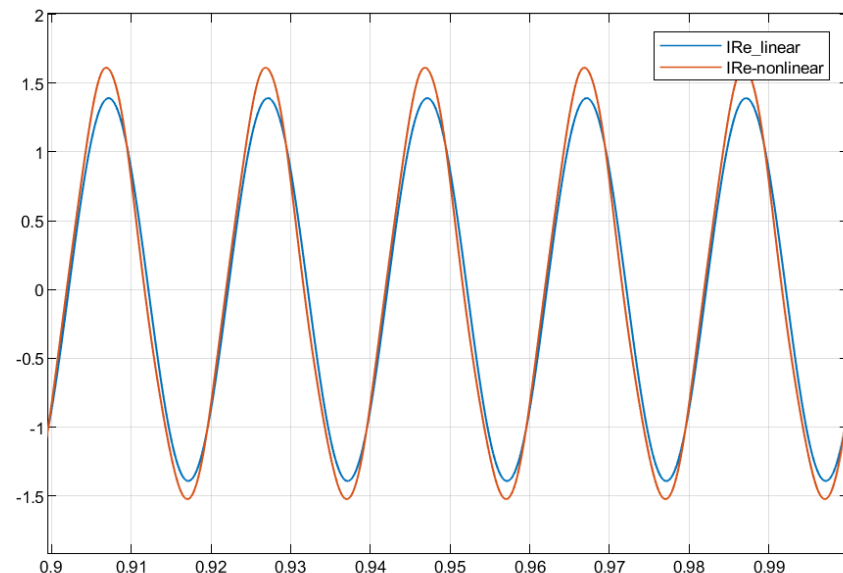
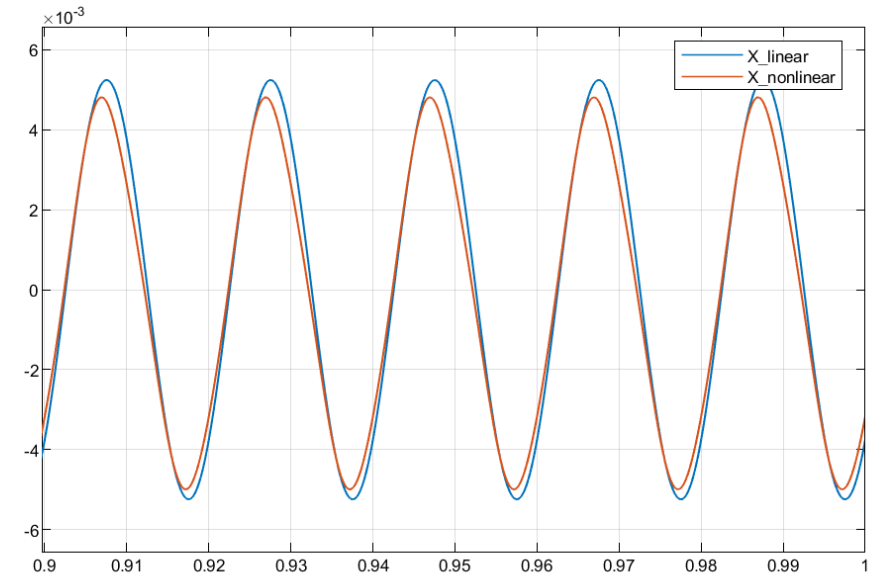
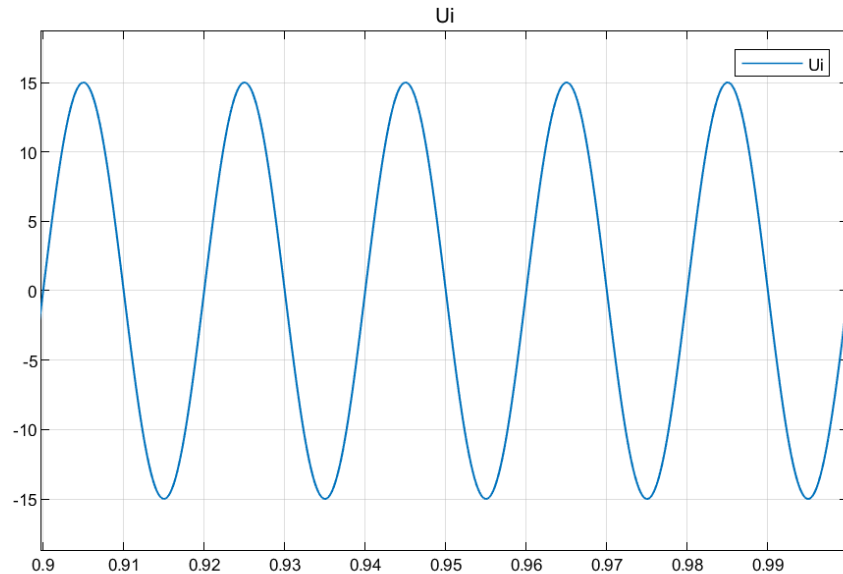


非线性模型



线性模型与非线性模型对比

- 非线性模型相对线性模型，在同样输入情况下电流、膜片位移和声压都有不同程度的失真



非线性导致的失真

Agenda

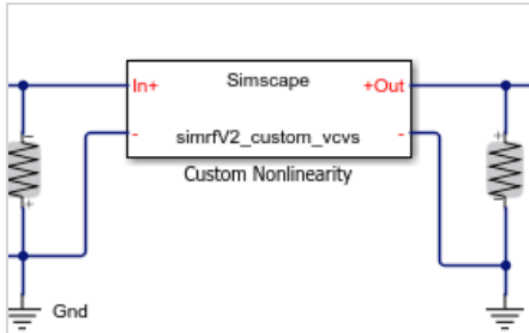
- 基于 Simscape 的电路仿真
- 射频电路仿真
- 高速电路信号完整性仿真

MathWorks 射频电路设计应用的四个特点：

- ✓ MATLAB& Simulink强大的建模能力：数学公式级/数据拟合行为级
 - ✓ 灵活的系统链路实现方式
 - ✓ 与通信算法的总体考量
 - ✓ 独立小程序的开发及发布
- 模块/芯片厂家的模型简单或者难以获取，传统工具提供的库或者PDK有限
 - 传统工具只能采用传统的拖拽方式搭建链路，不方便在不同版本间设计迭代和共享
 - 传统工具很难提供和算法的统一考量
 - 传统工具无法支持独立应用程序开发

案例1 使用Simscape创建模型

Featured Examples

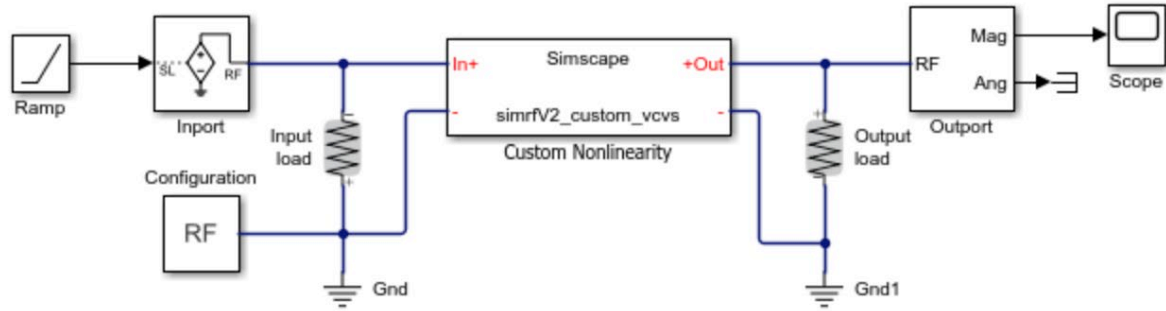


Copyright 2013-2018 The MathWorks, Inc.

Create Custom RF Blockset Models

Write your own RF Blockset™ Circuit Envelope model in Simscape® language for complex baseband simulation.

Shipping Demo



Copyright 2013-2018 The MathWorks, Inc.

Examine the Model

Double-click the "Custom Nonlinearity" block or type `open_system([model '/Custom Nonlinearity'])` in the command window.

SIMRFV2_CUSTOM_VCVS

Defines a VCVS (voltage controlled voltage source) using a third order polynomial with saturation. $V_{out} = c_0 + c_1 V_{in} + c_2 V_{in}^2 + c_3 V_{in}^3$ for $|V_{in}| \leq V_{sat}$; constant for $|V_{in}| > V_{sat}$

[Source code](#) Choose source

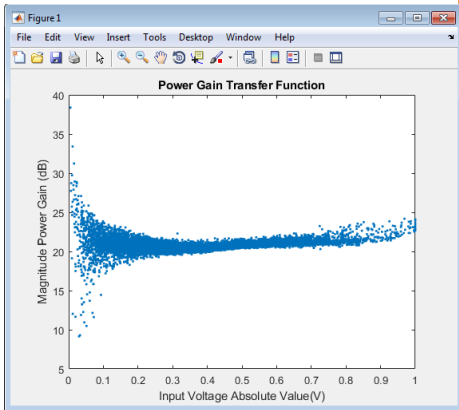
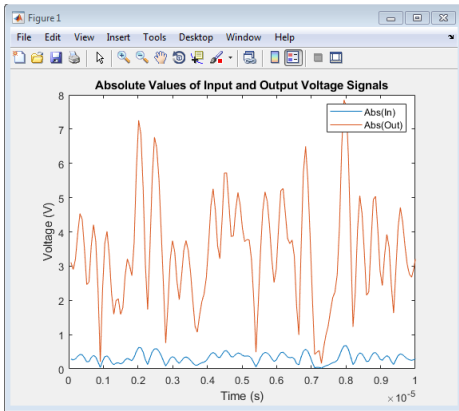
Settings

Parameters

c0:	<input type="text" value="0"/>	<input type="text" value="V"/>
c1:	<input type="text" value="1"/>	
c2:	<input type="text" value="0"/>	<input type="text" value="1/V"/>
c3:	<input type="text" value="-0.6"/>	<input type="text" value="1/V^2"/>
Input saturation voltage:	<input type="text" value="0.7"/>	<input type="text" value="V"/>

案例2 PA 模型的创建

PA Data



MATLAB fitting procedure (White box)

```
function a_coef = fit_memory_poly_model(x,y,memLen,degLen,modType)
% FIT_MEMORY_POLY_MODEL
% Procedure to compute a coefficient matrix given input and output
% signals, memory length, nonlinearity degree, and model type.
%
% Copyright 2017 MathWorks, Inc.

x = x(:);
y = y(:);
xLen = length(x);

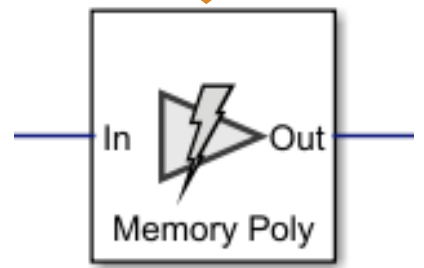
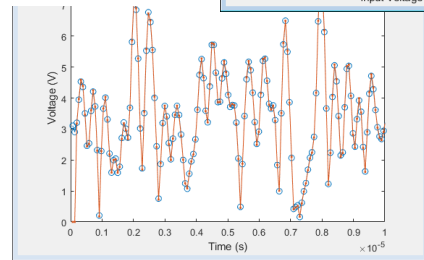
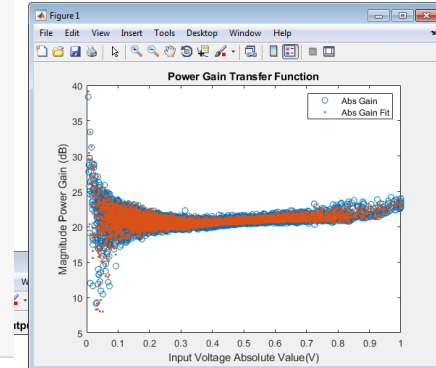
switch modType
case 'memPoly' % Memory polynomial
xrow = reshape((memLen:-1:1)' + (0:xLen:xLen*(degLen-1)),1,[]);
xVec = (0:xLen-memLen)' + xrow;
xPow = x.*(abs(x).^(0:degLen-1));
xVec = xPow(xVec);
case 'ctMemPoly' % Cross-term memory polynomial
absPow = (abs(x).^(1:degLen-1));
partTop1 = reshape((memLen:-1:1)' + (0:xLen:xLen*(degLen-2)),1,[]);
topPlane = reshape(
[ones(xLen-memLen+1,1),absPow((0:xLen-memLen)' + partTop1)].', ...
1,memLen*(degLen-1)+1,xLen-memLen+1);
sidePlane = reshape(x((0:xLen-memLen)' + (memLen:-1:1)).', ...
memLen,1,xLen-memLen+1);
cube = sidePlane.*topPlane;
xVec = reshape(cube,memLen*(memLen*(degLen-1)+1),xLen-memLen+1).';
end

coef = xVec\y(memLen:xLen);
a_coef = reshape(coef,memLen,numel(coef)/memLen);
```



PA model coefficients

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	7.1756 + 1.1238i	57.1783 - 12.3324i	10.5876 - 7.5994i	-2.423... -4.379... -1.125...	24.61... 1.461... 4.390... -94.35... -2.338... -8.825... 1.934... 1.8...									
2	3.2336 - 0.7538i	-25.2834 + 7.1506i	-4.4593 + 13.8723i	-9.675... 2.191... 2.847... 1.131... -8.420... -9.565... -4.801... 1.563... 2.309... 9.079... -1.4...										
3	-1.6834 + 1.1150i	12.5544 - 6.4201i	-4.6721 - 4.7128i	16.98... -1.006... 51.69... -1.516... 3.683... -2.068... 5.637... -6.580... 3.495... -9.910... 5.7...										
4														
5														
6														
7														
8														



PA model for circuit envelope simulation

案例3： 利用RF Budget Analyzer快速创建RF系统链路

Add RF components

Export to MATLAB / RF Blockset

The screenshot shows the RF Budget Analyzer interface with the following components in the cascade:

- TRSwitch (Stage 1)
- RF_Filter (Stage 2)
- LNA (Stage 3)
- Gain (Stage 4)
- Demod (Stage 5)
- IF_Filter (Stage 6)
- IFAmp (Stage 7)
- AGC (Stage 8)

The 'Results' section contains the following data table:

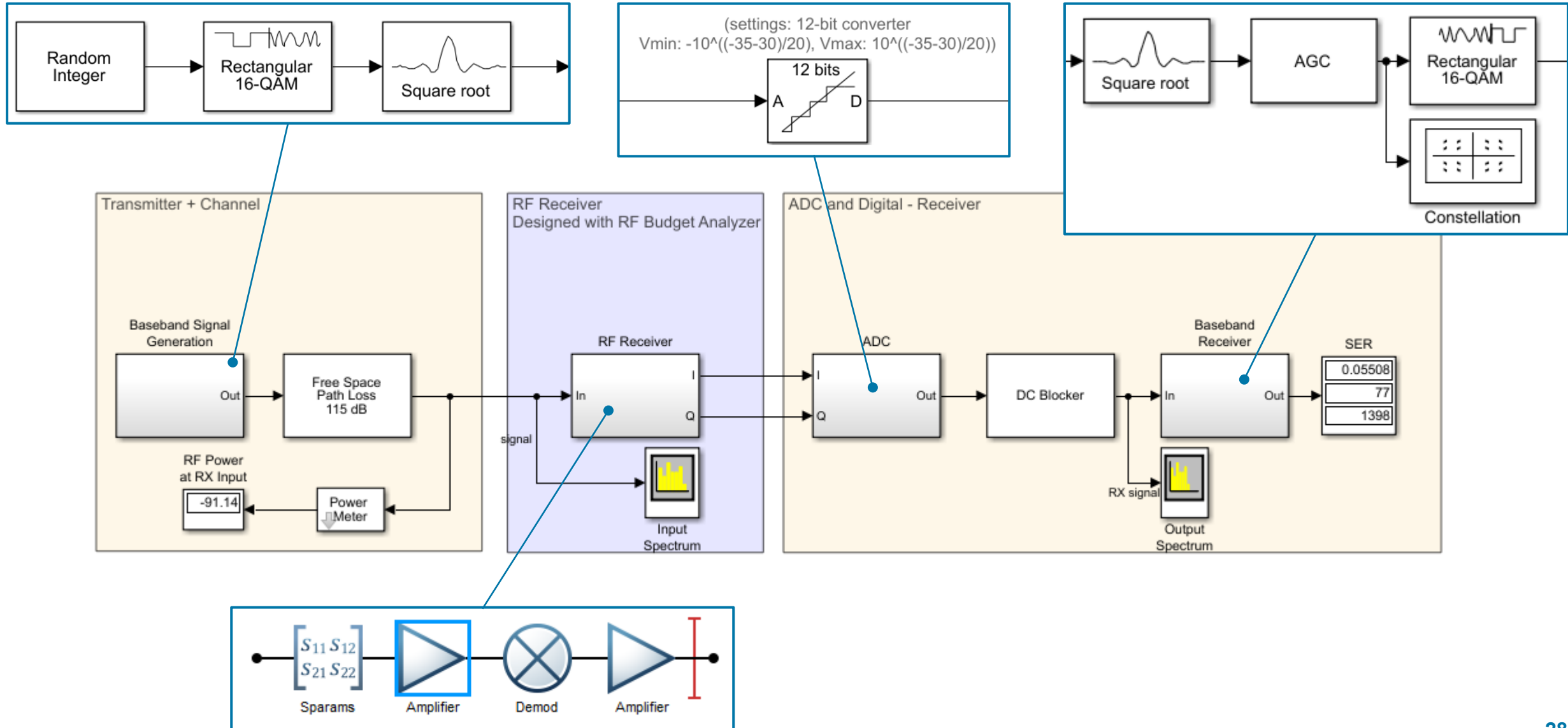
Cascade	1..1	1..2	1..3	1..4	1..5	1..6	1..7	1..8
Fout (GHz)	5.8000	5.8000	5.8000	5.8000	5.8000	0.4000	0.4000	0.4000
Friis-Pout (dBm)	-67.3000	-67.3000	-53.3000	-42.8000	-49.8000	-49.8000	-10.8000	6.7000
Friis-GainT (dB)	-1.3000	-1.3000	12.7000	23.2000	16.2000	16.2000	55.2000	72.7000
Friis-NF (dB)	2.3000	2.3000	3.5310	3.6572	3.6930	3.6930	3.7275	3.7275
Friis-OIP3 (dBm)	37	37	25.9863	22.8096	12.3757	12.3757	51.3757	35.9978
Friis-SNR (dB)	32.6649	32.6649	31.4339	31.3076	31.2719	31.2719	31.2374	31.2373

RF Cascade

Component specifications

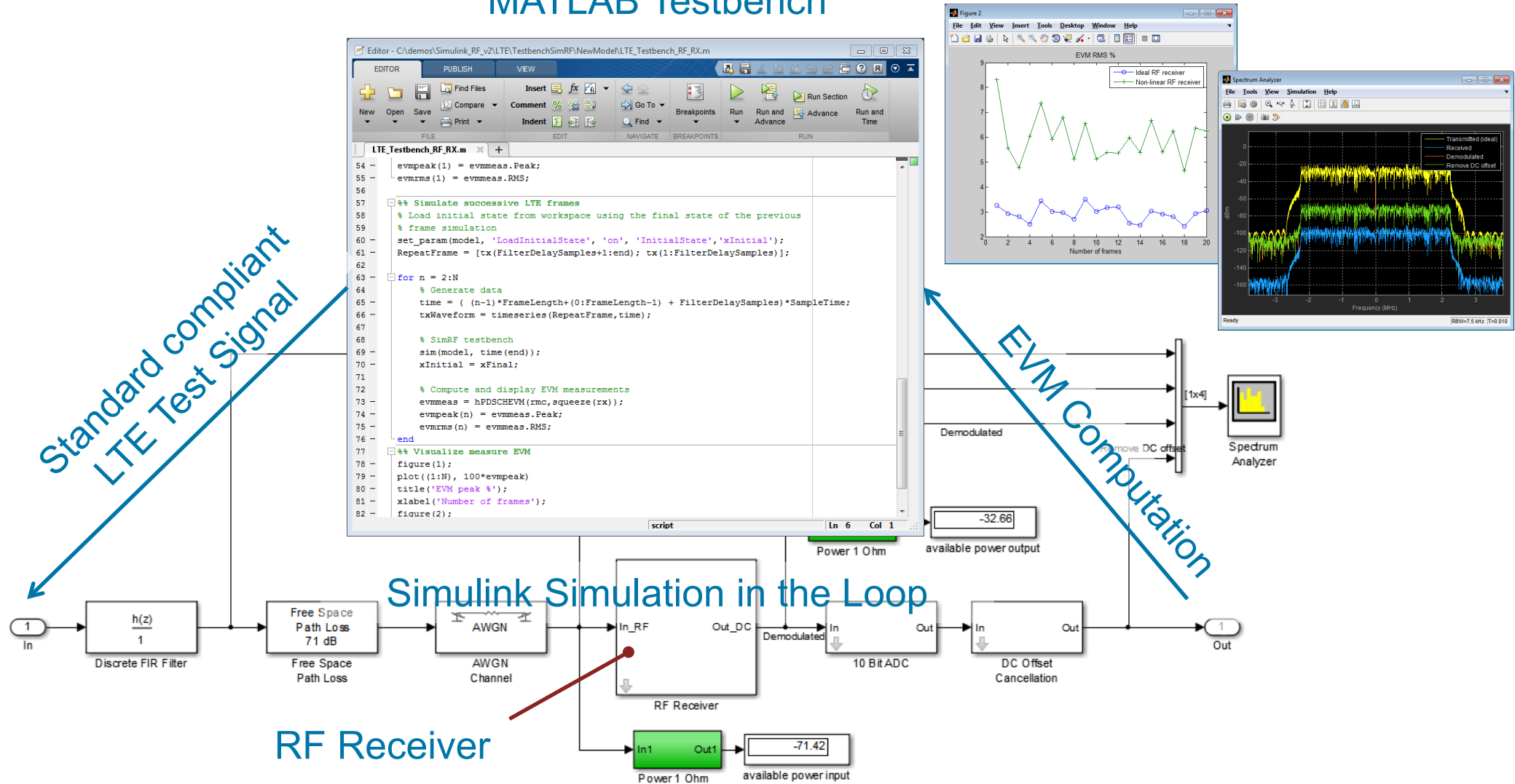
Cascade Budget Analysis

案例3： 利用RF Budget Analyzer快速创建RF系统链路



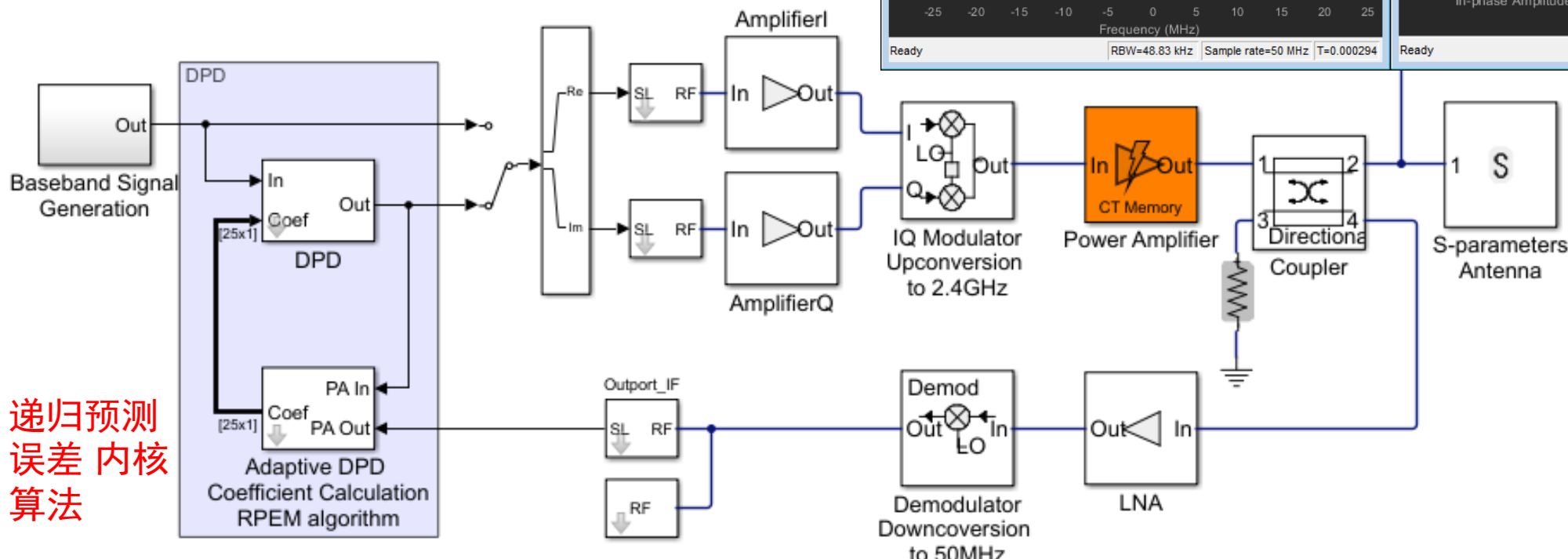
案例3 RF Receiver Integrated in MATLAB Testbench

MATLAB Testbench

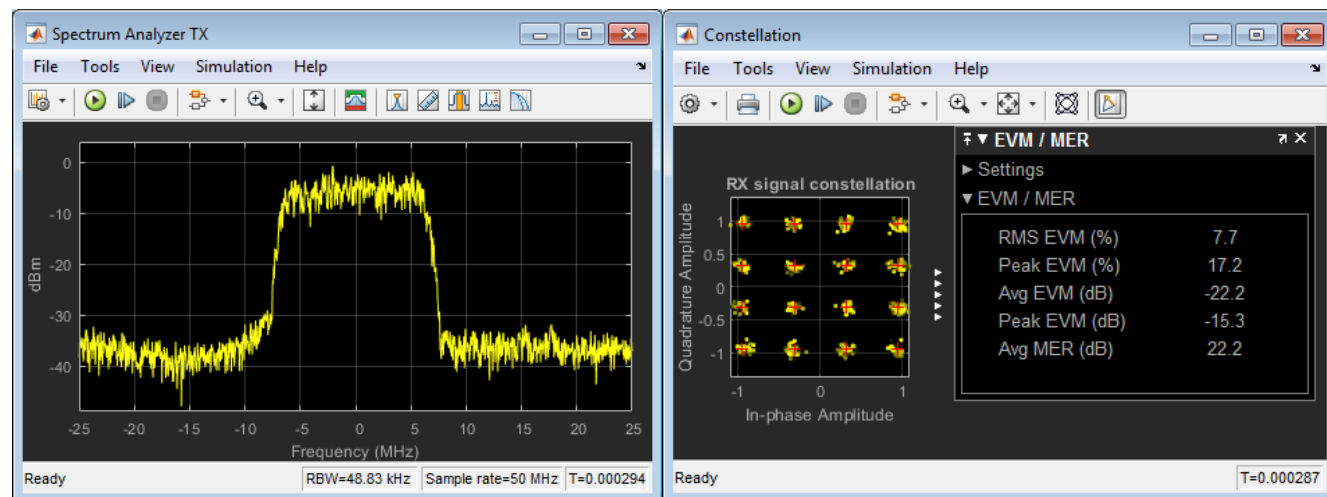


案例4 PA + DPD Simulation

- Circuit Envelope for fast RF simulation
- Low-power RF and analog components
 - Up-conversion / down-conversion
 - Antenna load
- Digital signal processing algorithm: DPD

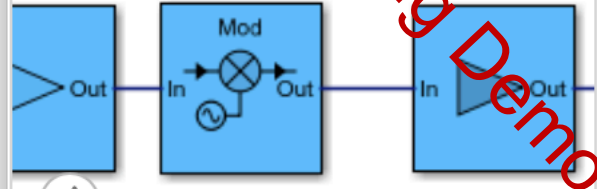


递归预测
误差内核
算法



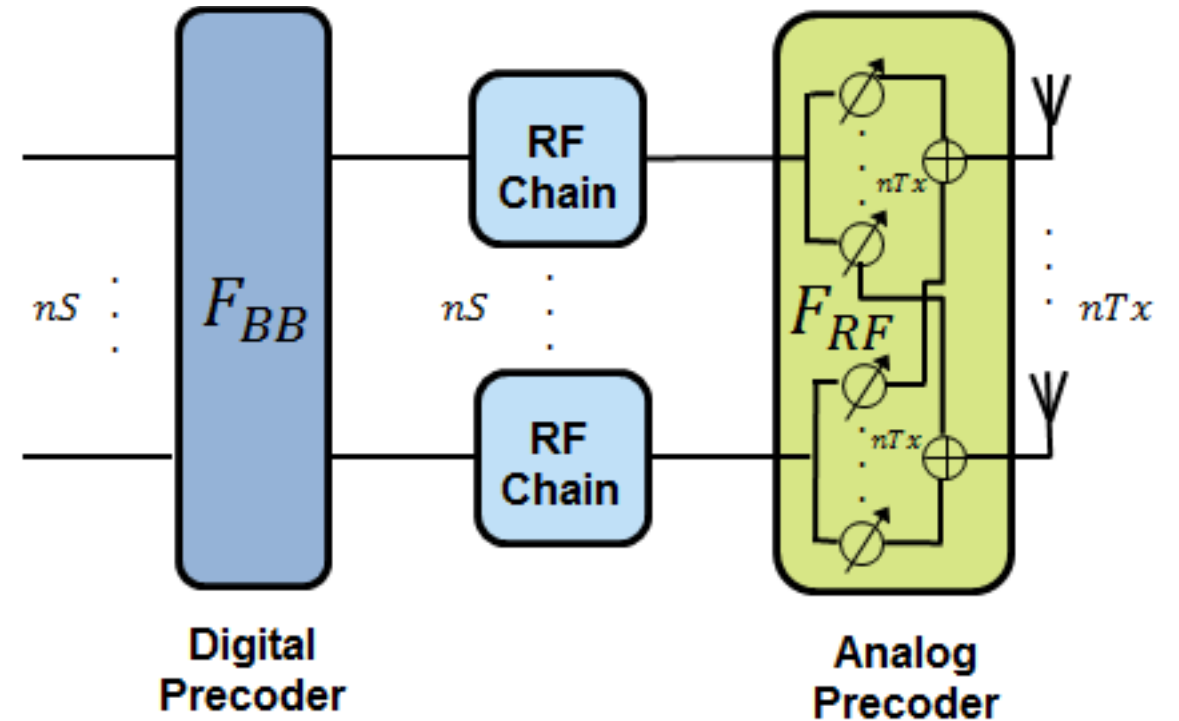
案例5 混合波束成形算法和RF链路的集成

Shipping Demo



Massive MIMO Hybrid Beamforming with RF Impairments

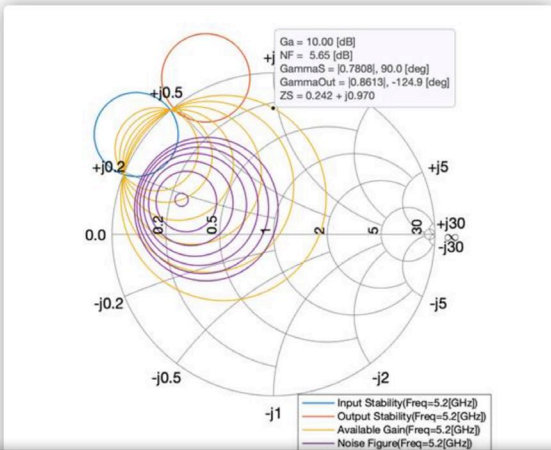
How hybrid beamforming is employed at the transmit end of a massive MIMO communications system, using



其他电路层面的应用

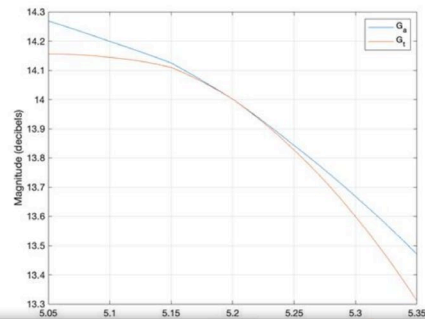
LNA阻抗匹配网络

Demo: RF Toolbox “Designing Matching Networks (Part 1: Networks with an LNA and Lumped Elements)”

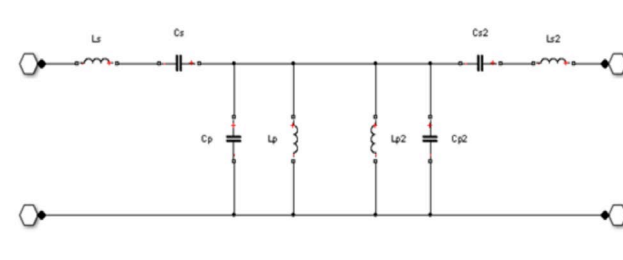


```
input_match = rfckt.cascade('Ckts', ...
    {rfckt.shuntrlc('C',Cin),rfckt.seriesrlc('L',Lin)});
output_match = rfckt.cascade('Ckts', ...
    {rfckt.seriesrlc('L',Lout),rfckt.shuntrlc('C',Cout)});
LNA = rfckt.cascade('ckts', ...
    {input_match,unmatched_amp,shunt_r,output_match});
```

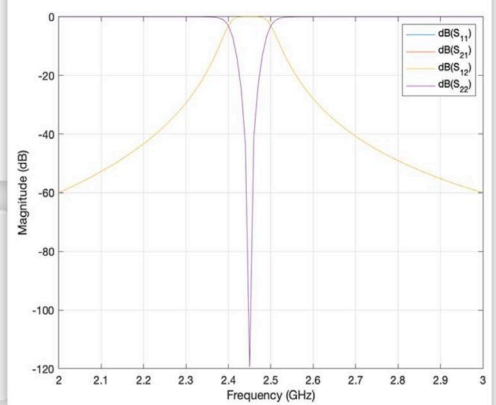
```
analyze(LNA,5.05e9:10e6:5.35e9);
plot(LNA,'Ga','Gt','dB');
```



滤波器设计



```
freq = linspace(2e9,3e9,101);
setports(ckt,[2 1],[6 1]);
S = sparameters(ckt,freq);
rfplot(S)
```



Ro = 50;
f1C = 2400e6;
f2C = 2500e6;

$$L_s = (R_o / (\pi * (f_2C - f_1C))) / 2;$$

$$C_s = 2 * (f_2C - f_1C) / (4 * \pi * R_o * f_2C * f_1C);$$

$$L_p = 2 * R_o * (f_2C - f_1C) / (4 * \pi * f_2C * f_1C);$$

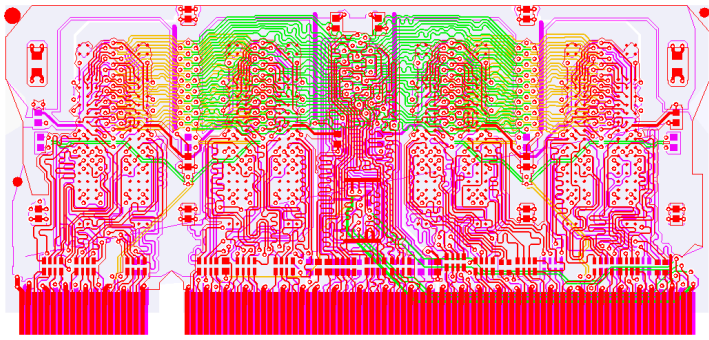
$$C_p = (1 / (\pi * R_o * (f_2C - f_1C))) / 2;$$

独立应用程序的开发，满足内部不同应用

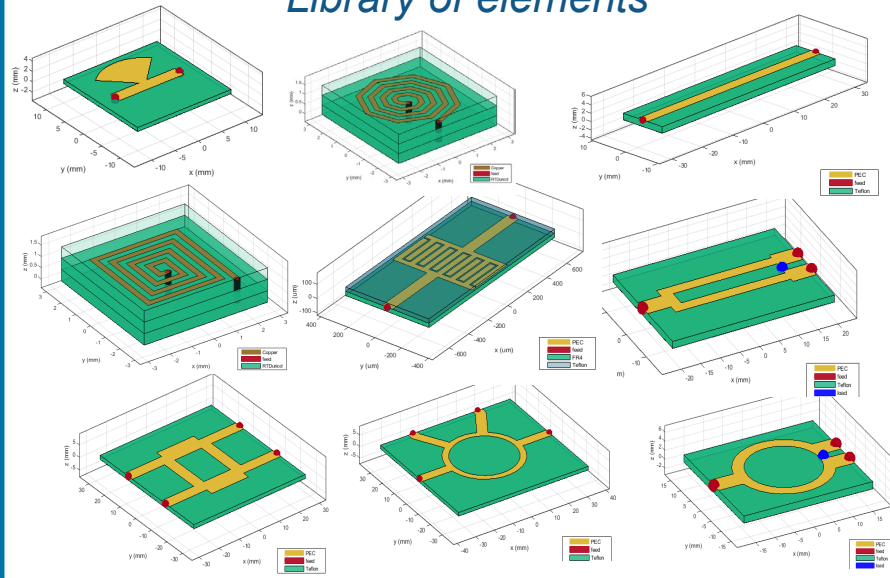
天线匹配网络设计

R2022a新功能：射频PCB板分析

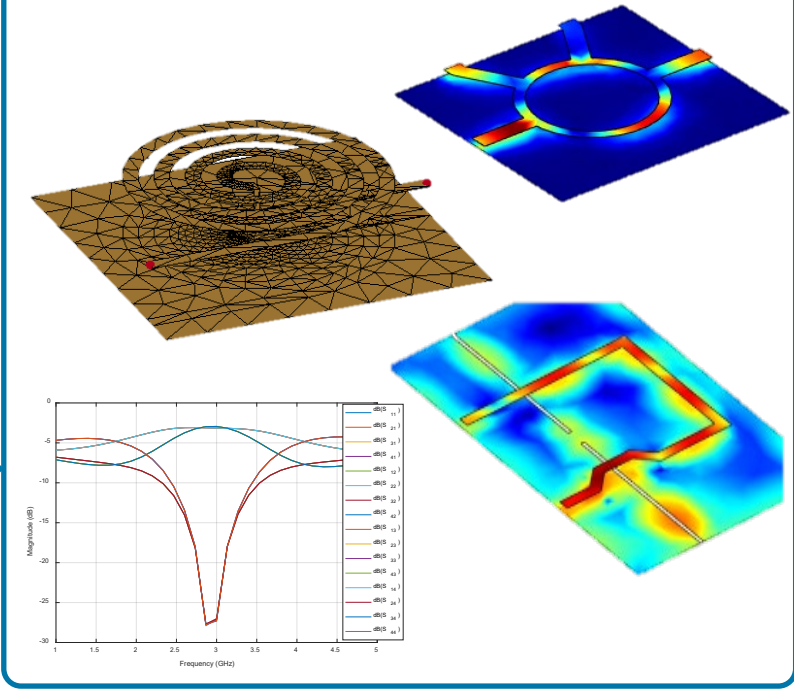
PCB database import



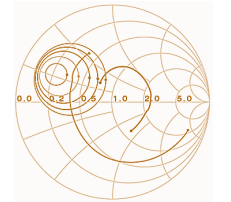
Library of elements



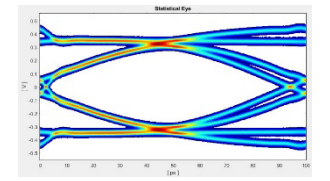
EM Analysis



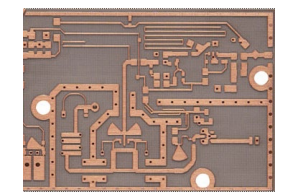
S-parameters



Channel Models



Prototyping (Gerber)

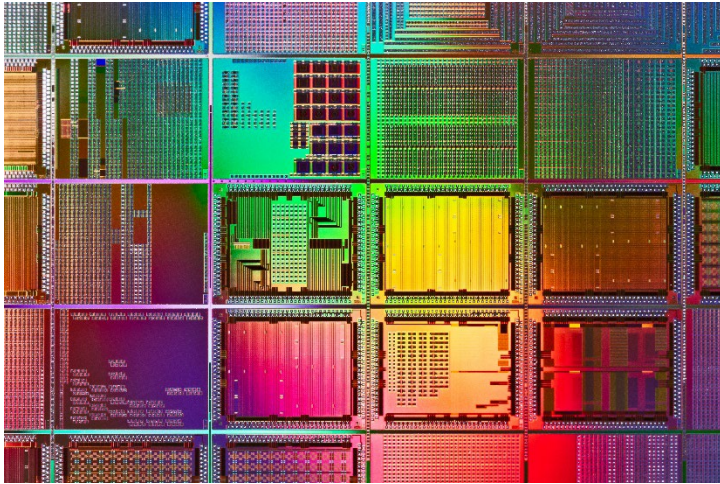


Agenda

- 基于 Simscape 的电路仿真
- 射频电路仿真
- 高速电路信号完整性仿真

高速设计中信号完整性

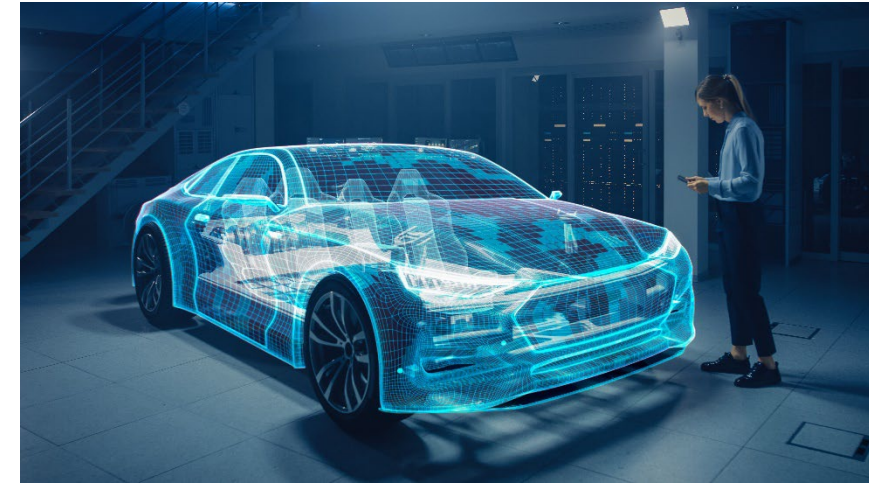
Semiconductor



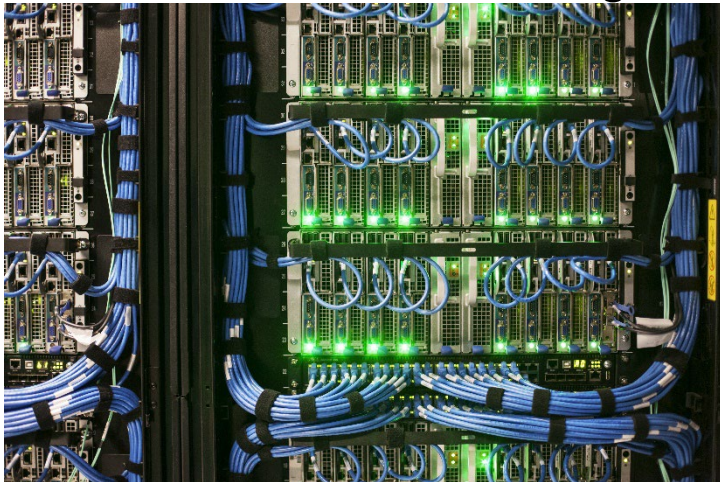
AeroDef



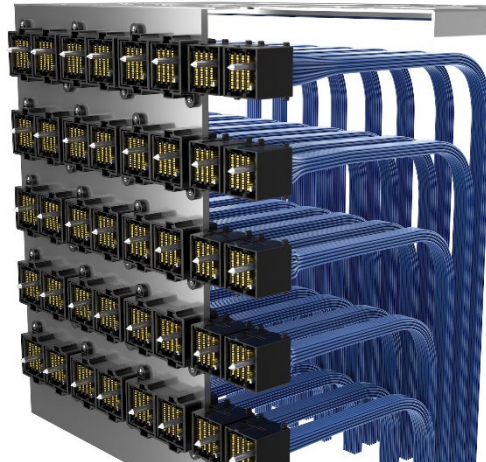
Automotive



Server / Switch / Storage



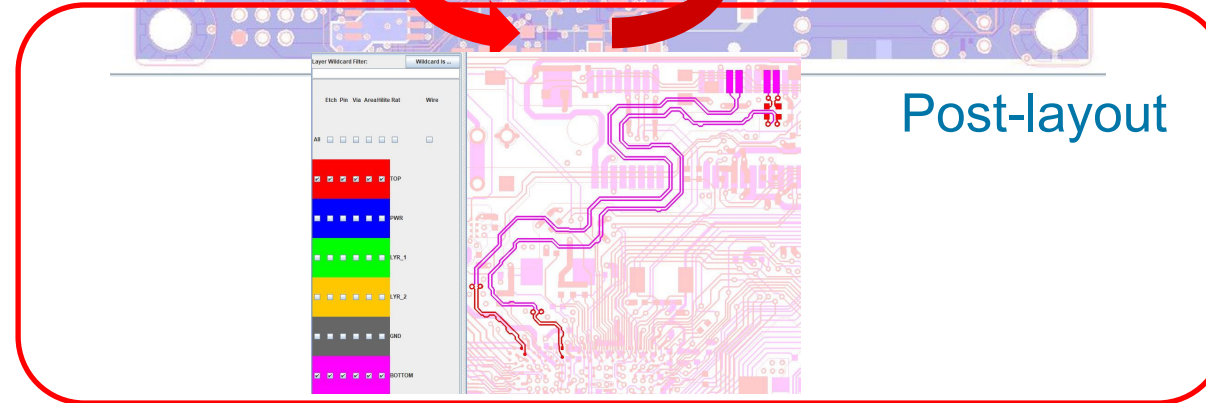
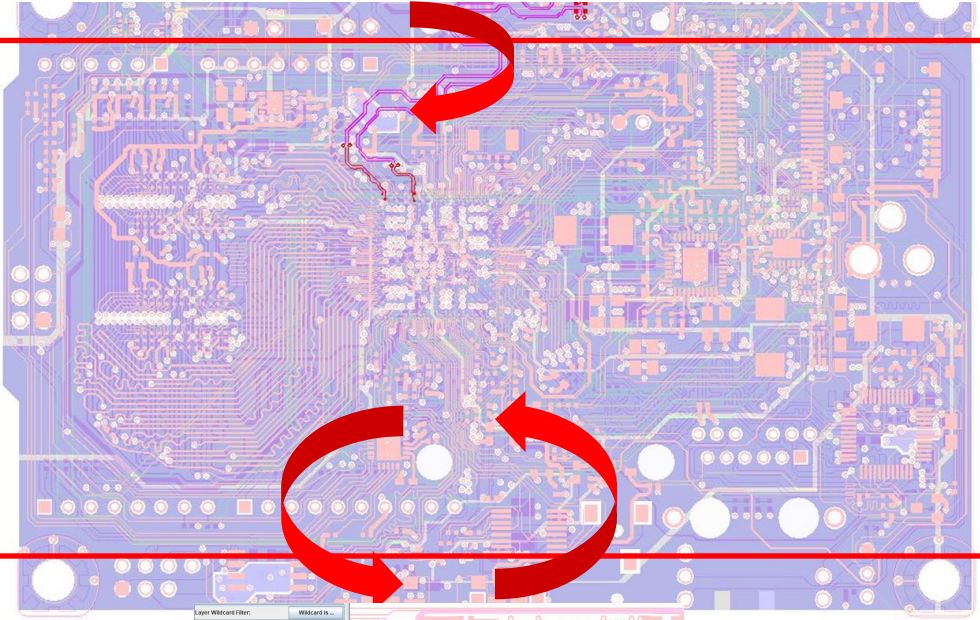
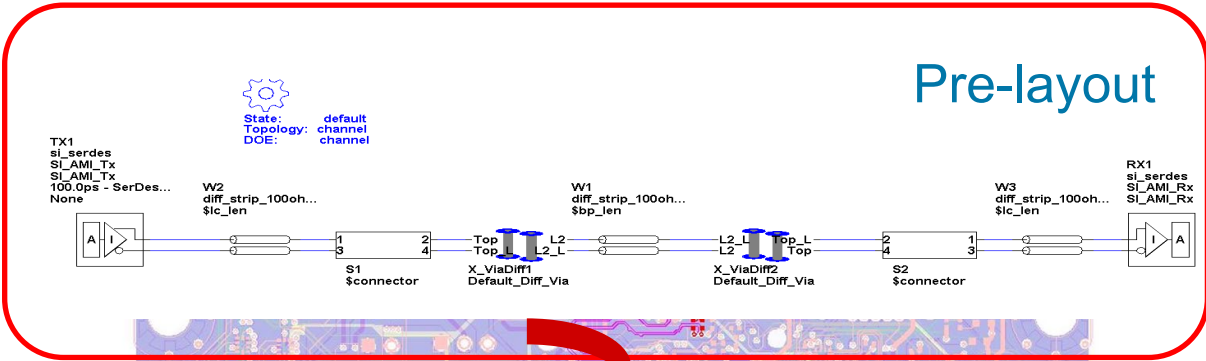
PCB / Connector / Cables



Test & Measurement



MathWorks 解决方案



MATLAB

Signal Integrity Toolbox

RF Toolbox

SerDes Toolbox

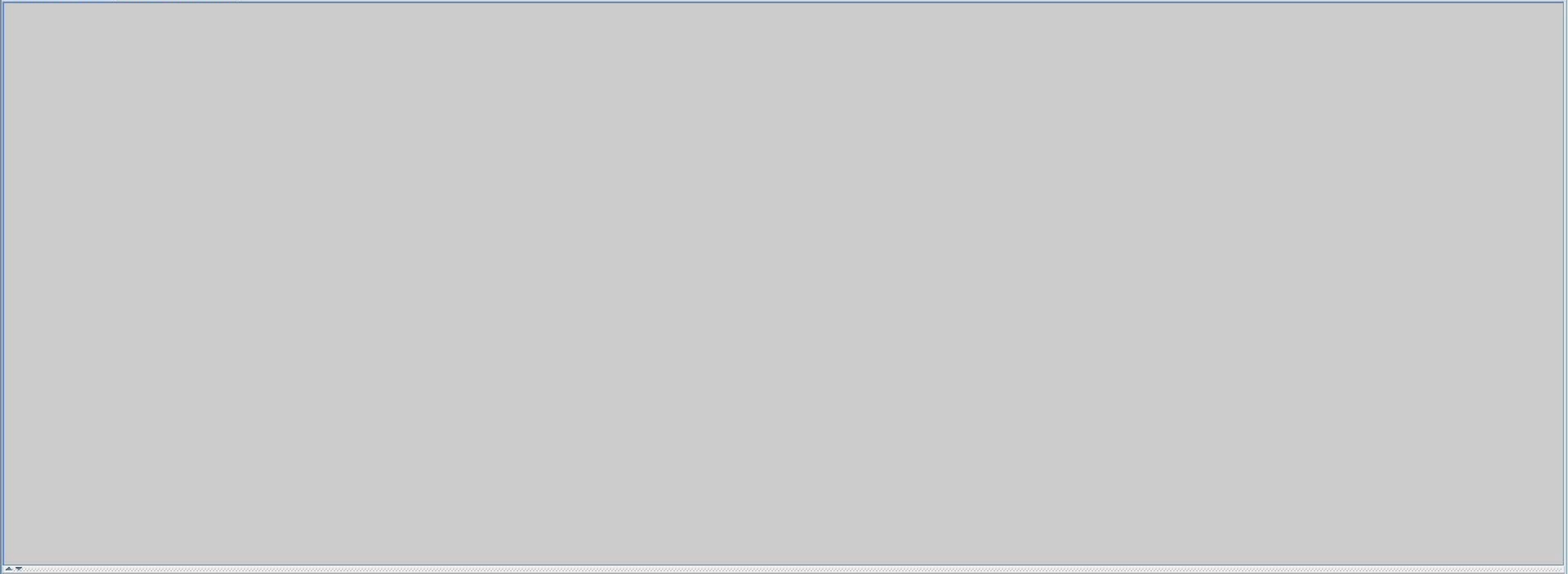
Simulink, DSP System, and Signal Processing Toolboxes (Required)

RF PCB Toolbox

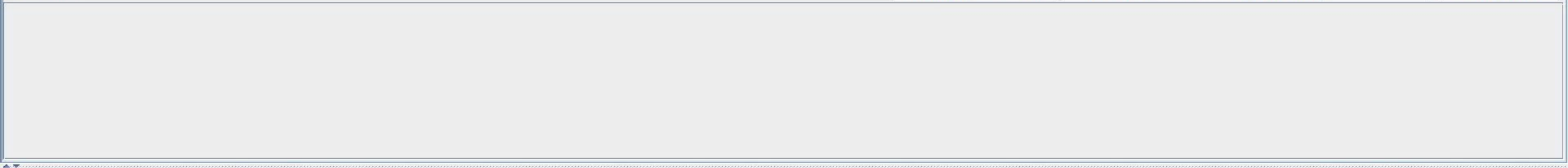
RF Toolbox

Signal Integrity Toolbox

Parallel Computing Toolbox


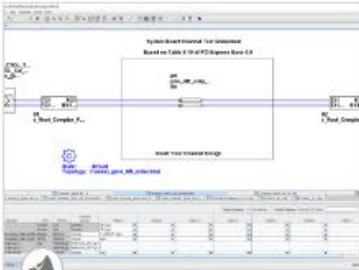

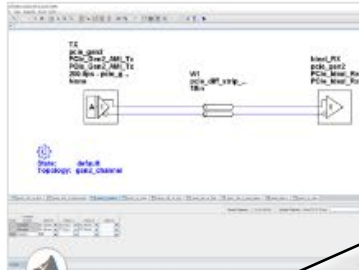
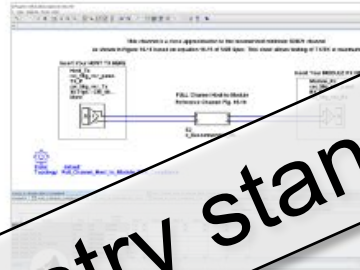
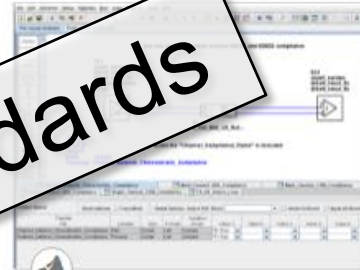

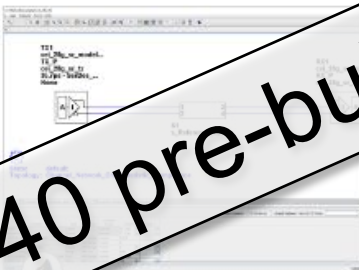

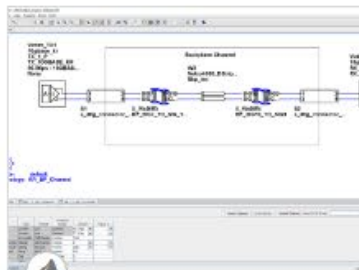
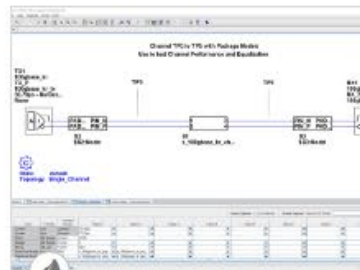
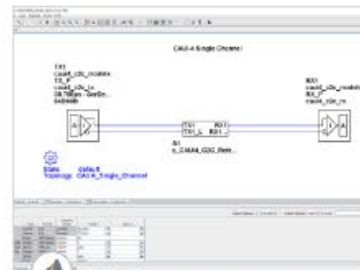


Solution Space: Sheet Options: Case Mode Global Options: Incremental Select DOE Sheet: Show On Board



Signal Integrity Toolbox Features – Standards Compliance

Industry Standard Signal Integrity Kits — Examples

 <p>PCIe-5 Compliance Kit</p> <p>Test the compliance of simulation models and topologies to the PCI Express generation 5 (PCIe-5) specification.</p>	 <p>PCIe-4 Compliance Kit</p> <p>Test the compliance of simulation models and topologies to the PCI Express generation 4 (PCIe-4) specification.</p>	 <p>PCIe-3 Compliance Kit</p> <p>Test the compliance of simulation models and topologies to the PCI Express generation 3 (PCIe-3) specification.</p>	 <p>PCIe-2 Compliance Kit</p> <p>Test the compliance of simulation models and topologies to the PCI Express generation 2 (PCIe-2) specification.</p>	 <p>CEI 56G-VSR Compliance Kit</p> <p>Characterize and validate the performance of a CEI 56G-VSR channel design.</p>	 <p>CEI 56G-LR Compliance Kit</p> <p>Characterize and validate the performance of a CEI 56G-LR channel design.</p>
 <p>CEI 28G-VSR Compliance Kit</p> <p>Characterize and validate the performance of a CEI 28G-VSR channel design.</p>	 <p>CEI 28G-SR Compliance Kit</p> <p>Characterize and validate the performance of a CEI 28G-SR channel design.</p>	 <p>CEI 25G-LR Compliance Kit</p> <p>Characterize and validate the performance of a CEI 25G-LR channel design.</p>	 <p>10GBASE-KR4 Compliance Kit</p> <p>Characterize and validate the performance of a 10GBASE-KR4 channel design.</p>	 <p>100GBASE-KR4 Compliance Kit</p> <p>Characterize and validate the performance of a 100GBASE-KR4 channel design.</p>	 <p>CAUI-4 Chip-to-Chip Compliance Kit</p> <p>Test the compliance of simulation models and topologies to the CAUI-4 C2C specification.</p>

Over 40 pre-built design kits for industry standards

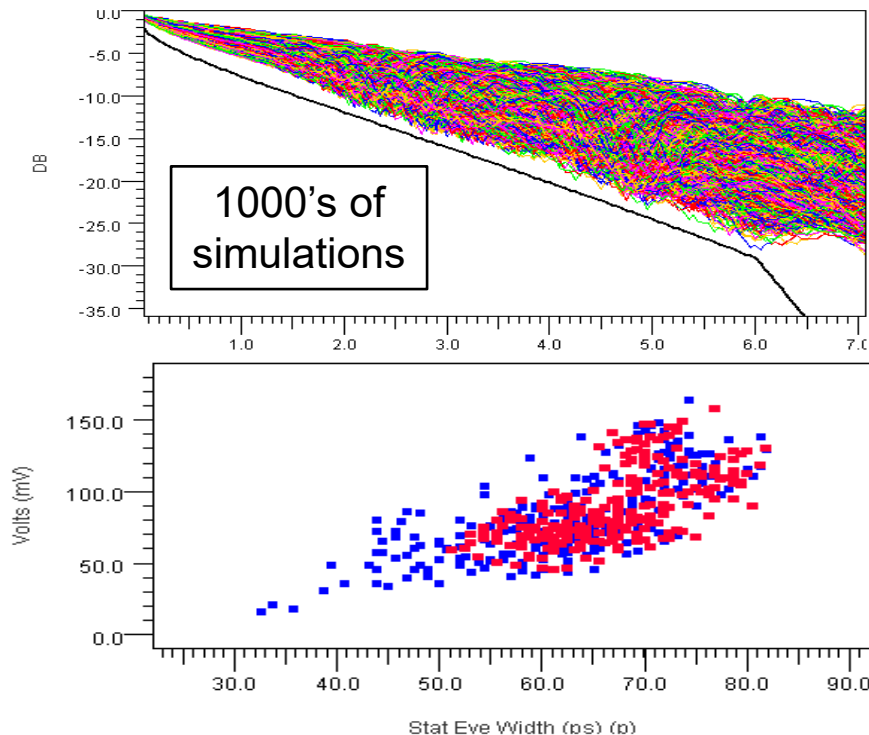
Design Space Exploration

For both Serial and Parallel Designer apps

Solution Space:

Transfer Net	Variable:	Type:	Format:	Variation Group:	Value 1:	Value 2:	Value 3:	Value 4:	Value 5:
channel	Etch	Corner	List	Corners	TE (Typ)				
channel	Process	Corner	List	Corners	TT (Typ)				
channel	\$bp_len	W Length	Soft Range	<none>	16in				
channel	\$connector	Subcircuit Model	List	<none>	s_connector_ab	s_connector_cd	s_connector_ef	s_connector_gh	
channel	\$lc_len	W Length	Soft Range	<none>	3in	2in	4in	5in	
channel	RX1:Rx_Receiver_Sensitivity	Float	AMI Range	<none>	0.025				
channel	RX1:peaking_filter.config	Integer	AMI Range	<none>	0				
channel	RX1:peaking_filter.mode	String	AMI List	<none>	off				
channel	RX1:clock_recovery.ref	Float	AMI Range	<none>	0.0				
channel	RX1:dfc.taps.1	Tap	AMI Range	<none>	0				

4 connectors
 x
 4 line-card lengths
 =
 16 simulations



Interface: 100GBASE_KR
 Reference Schematic: Set: 100GBASE_KR

Process Controls:

Stop On Error Setup Stop Error Conditions

Backup Before Deleting Data Restore

Simulation Options... Simulation Parameters... **Parallel** Configure Parallel...

Channel Analysis Steps:

Validate

Generate Netlists

Include Statistical Analysis

Include Time Domain Analysis

Run SPICE

Perform Channel Analysis

Display Results Spreadsheet

Autoload Results

All Sheets Current Sheet

Channel Analysis Summary

Parallel Computing Toolbox Clusters:

Default Cluster: local

Cluster Selection:

SPICE: <Default Cluster>

Channel Analysis: <Default Cluster>

Number of Simulations Per Task: 1

Channel Analysis: 1

Parallel Help Test... Refresh Clusters

Local to Remote Path Maps:

Local Path	Remote Path
/	/

File Completion Retry:

Completion Retry Count: 3

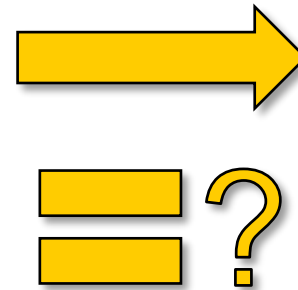
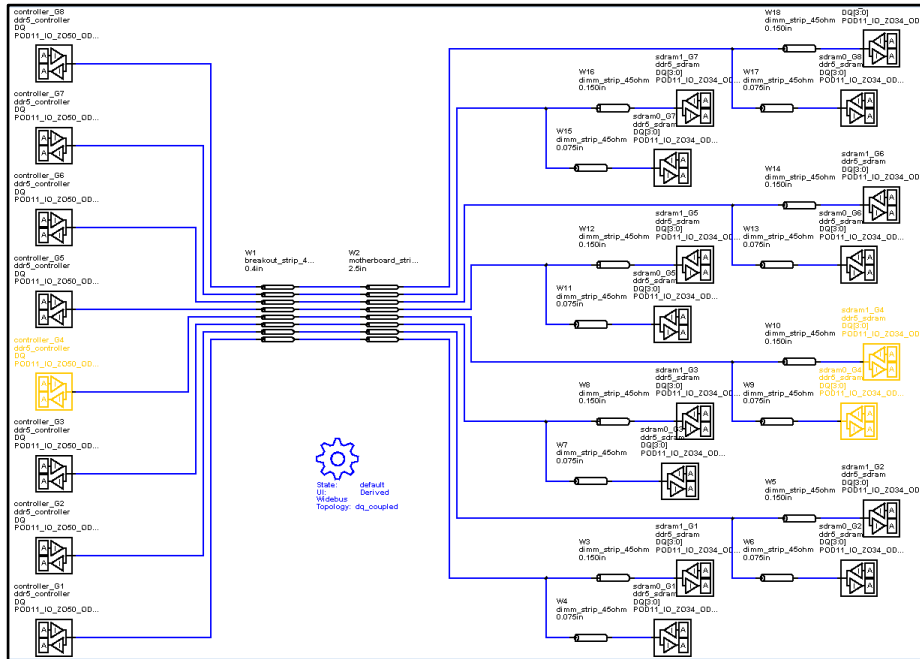
Completion Retry Pause: 3

Run Close Errors & Warnings Autoload Results

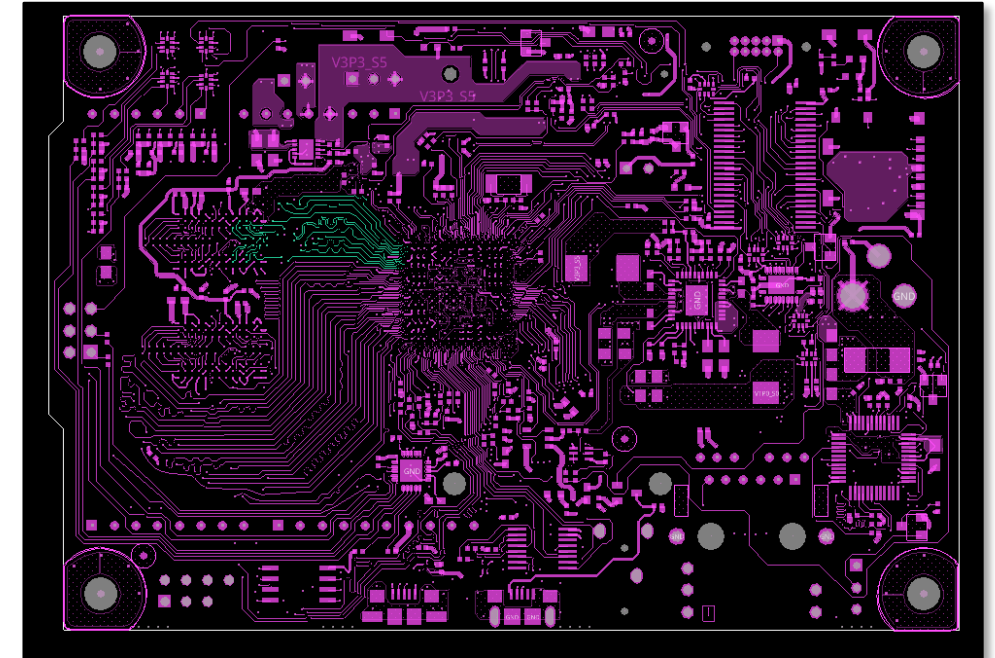
Accelerate with Parallel Computing Toolbox and MATLAB Parallel Server

Signal Integrity Toolbox + RF PCB Toolbox

Pre-layout



Post-layout



- Use RF PCB Toolbox to import PCB files
- Compare pre- and post-layout nets to each other
- Easily identify any issues
- Incorporate fixes and re-simulate

- Cadence Allegro
- Mentor PADS Layout
- Mentor Board Station
- Mentor Expedition PCB
- Cadence APB
- Intercept Pantheon
- Altium Designer
- Altium P-CAD
- IBIS EBD

MATLAB EXPO

Thank you



© 2023 The MathWorks, Inc. MATLAB and Simulink are registered trademarks of The MathWorks, Inc. See [mathworks.com/trademarks](https://www.mathworks.com/trademarks) for a list of additional trademarks. Other product or brand names may be trademarks or registered trademarks of their respective holders.