MATLAB EXPO

MATLAB和Simulink在电路仿真中的应用

周前程

赵晨星

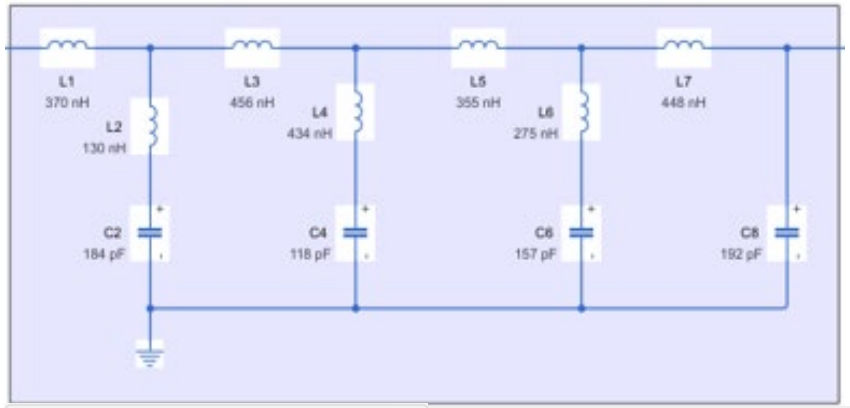
MathWorks®

Agenda

- 基于 Simscape 的电路仿真
- 射频电路仿真
- 高速电路信号完整性仿真

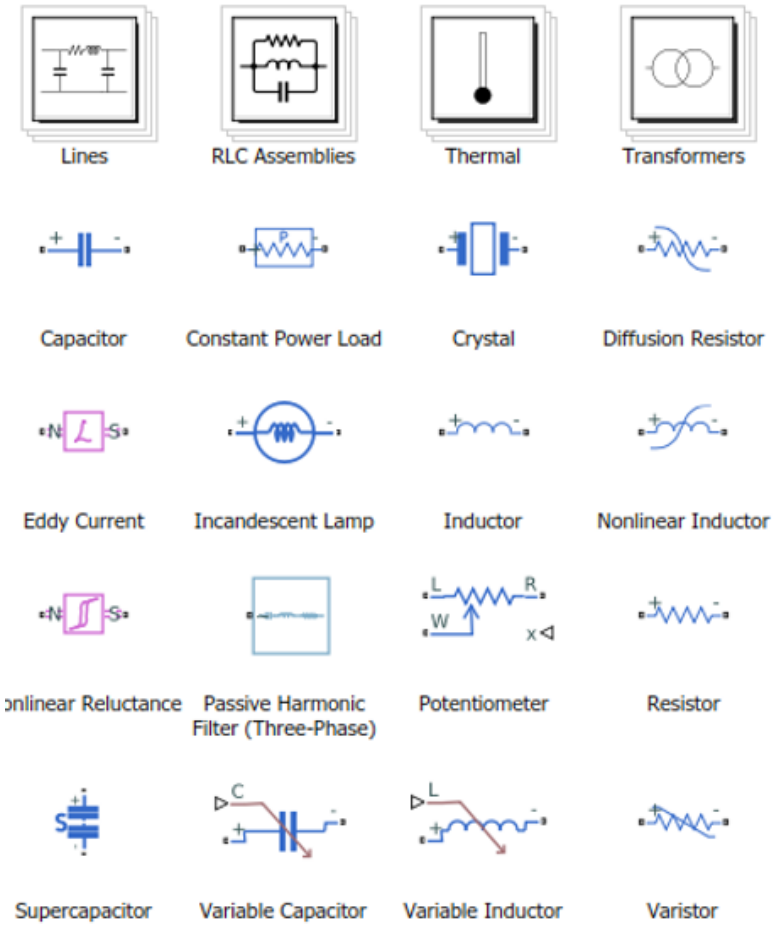
基于 Simscape 的电路仿真

- Simscape 特性
  - 基于原理图建模
  - 时域仿真 + 频域分析
  - 多物理域 + 控制系统仿真
  - 开放的自定义元件与物理域接口

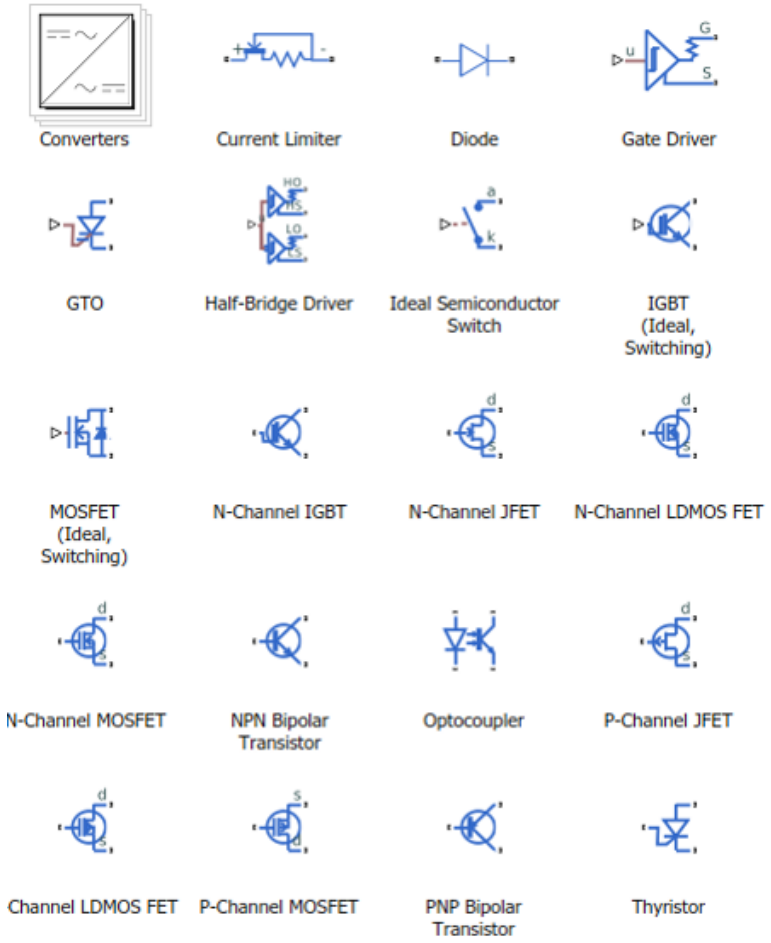


电气元件库

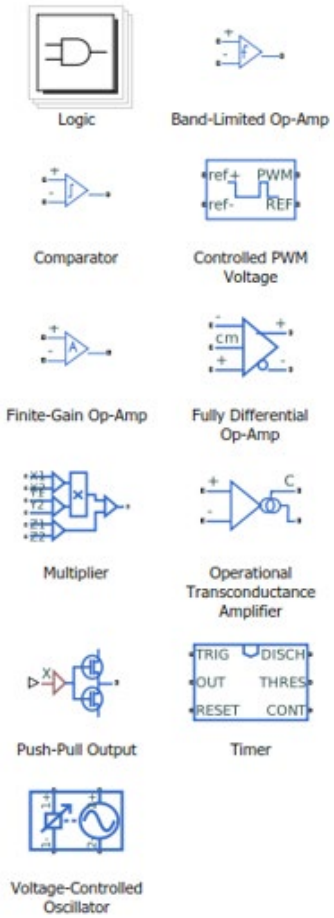
无源器件



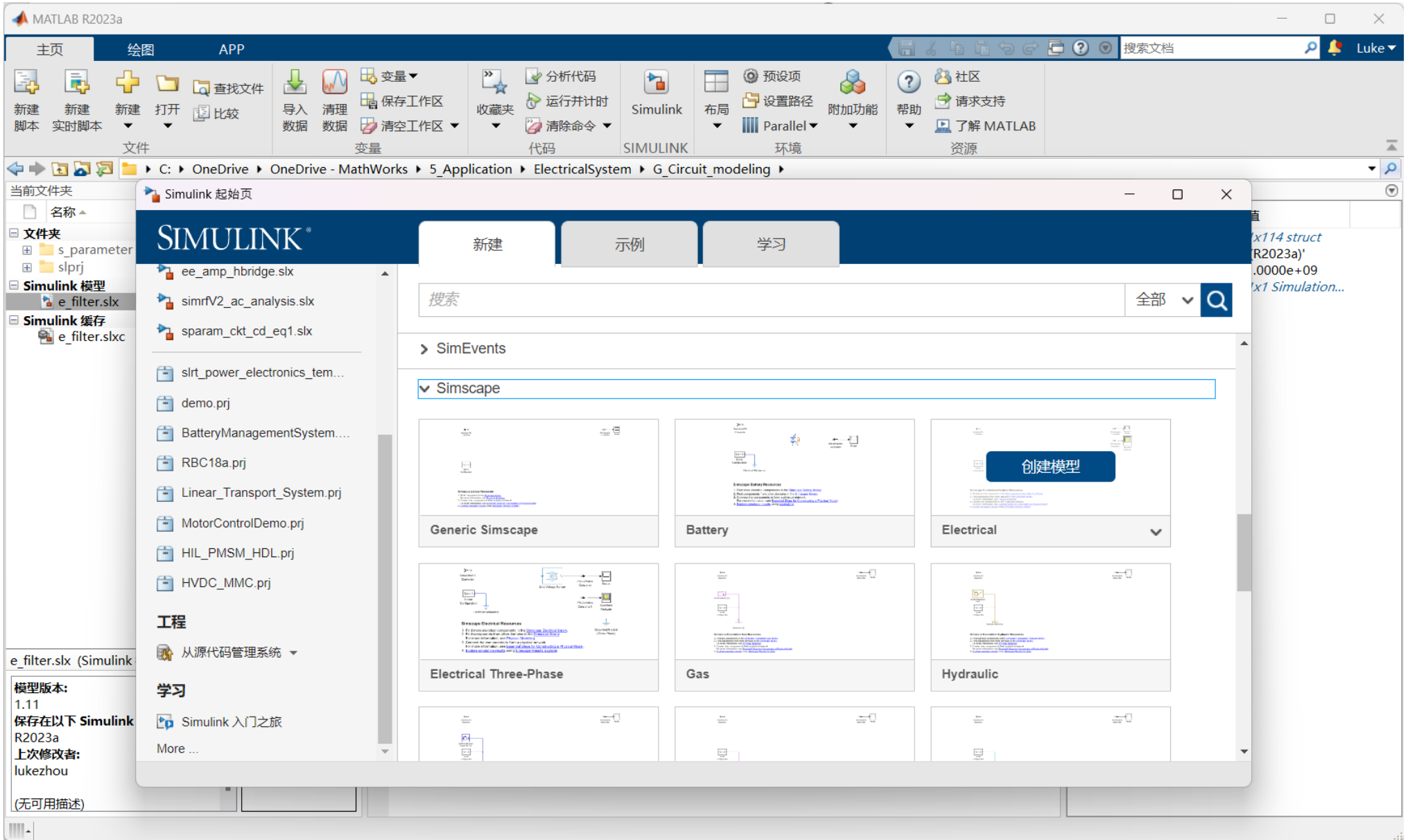
半导体器件



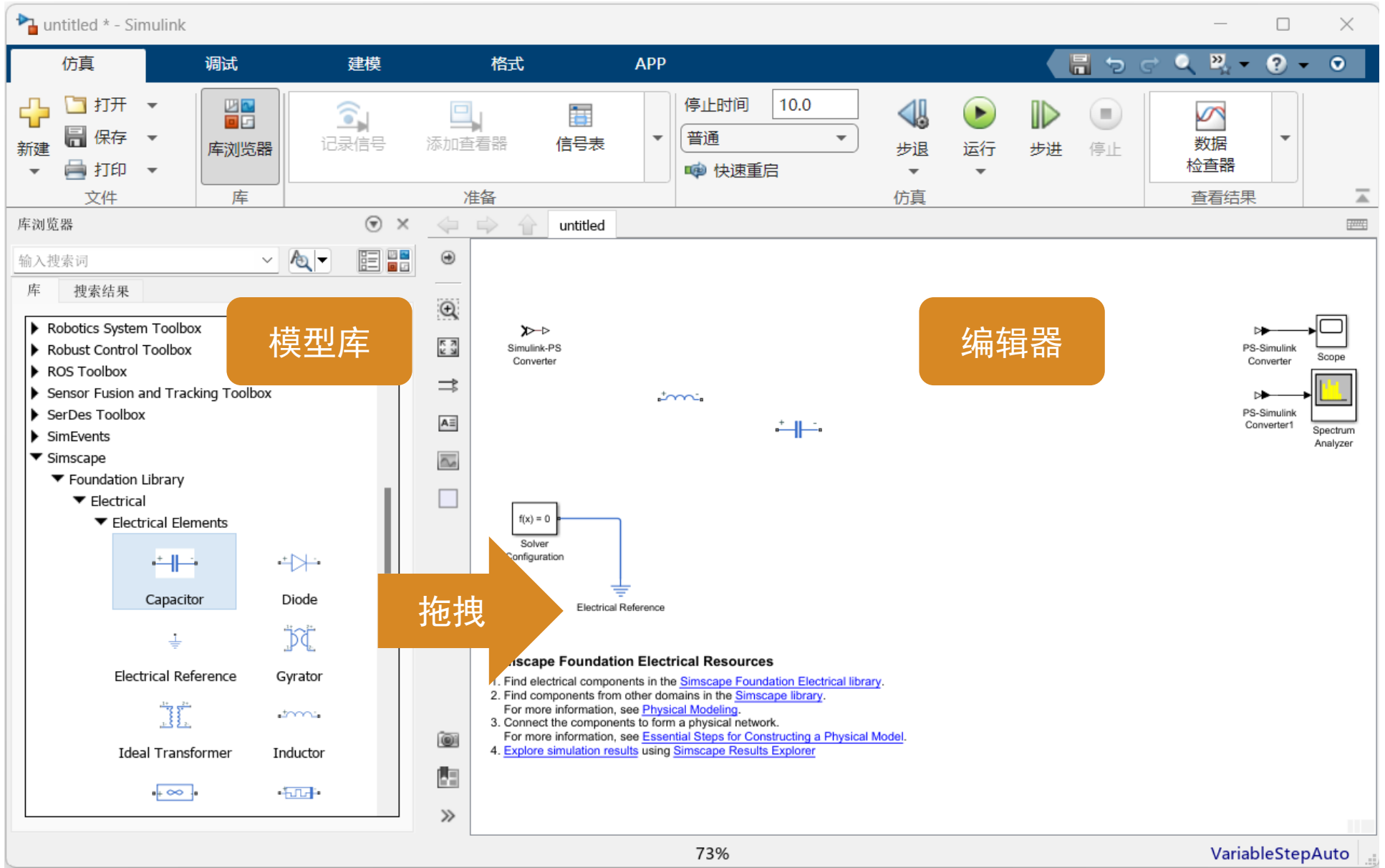
IC



建立电路模型


MATLAB R2023a
主页
绘图
APP
搜索文档
Luke
新建脚本
新建实时脚本
新建
打开
查找文件
比较
文件
导入数据
清理数据
变量
保存工作区
清空工作区
变量
收藏夹
分析代码
运行并计时
清除命令
代码
Simulink
SIMULINK
布局
预设项
设置路径
Parallel
附加功能
环境
帮助
社区
请求支持
了解 MATLAB
资源
C: ▸ OneDrive ▸ OneDrive - MathWorks ▸ 5_Application ▸ ElectricalSystem ▸ G_Circuit_modeling ▸
当前文件夹
名称
文件夹
s_parameter
slprj
Simulink 模型
e_filter.slx
Simulink 缓存
e_filter.slxc
e_filter.slx (Simulink
模型版本:
1.11
保存在以下 Simulink
R2023a
上次修改者:
lukezhou
(无可用描述)
Simulink 起始页
SIMULINK
新建
示例
学习
ee_amp_hbridge.slx
simrfV2_ac_analysis.slx
sparam_ckt_cd_eq1.slx
slrt_power_electronics_tem...
demo.prj
BatteryManagementSystem....
RBC18a.prj
Linear_Transport_System.prj
MotorControlDemo.prj
HIL_PMSM_HDL.prj
HVDC_MMC.prj
工程
从源代码管理系统
学习
Simulink 入门之旅
More ...
搜索
全部
SimEvents
Simscape
Generic Simscape
Battery
Electrical
创建模型
Electrical Three-Phase
Gas
Hydraulic

添加元件到模型中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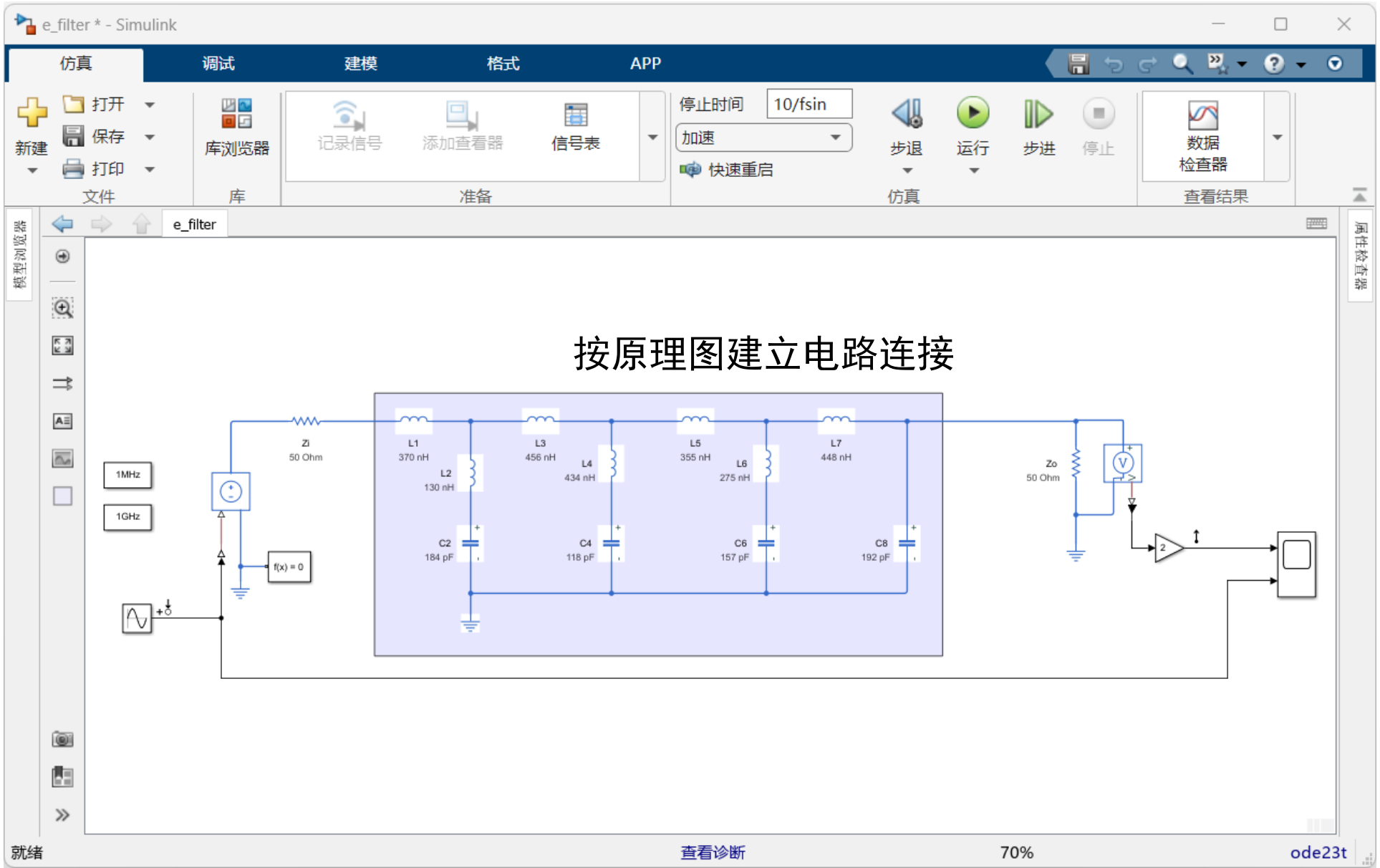
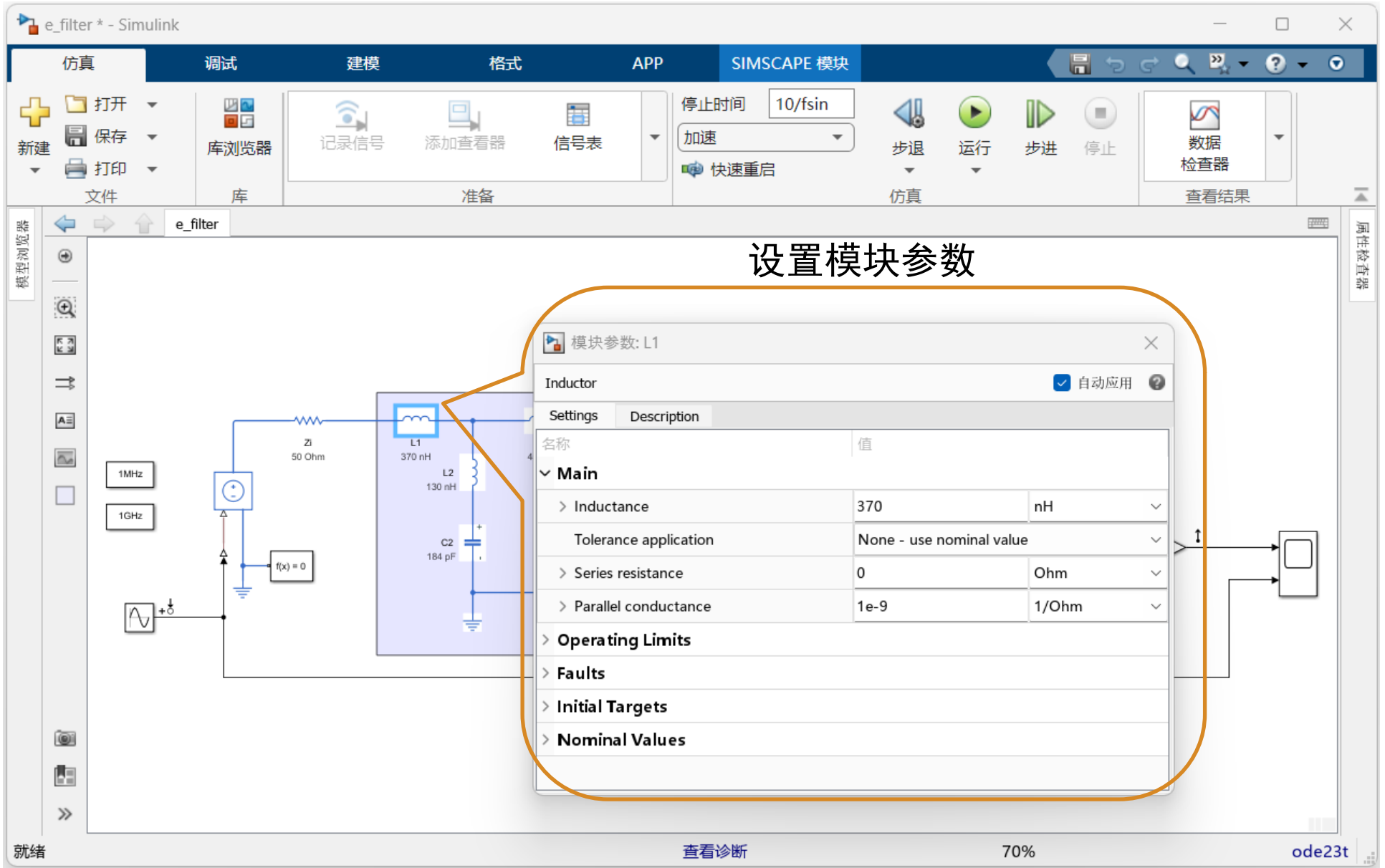
仿真
调试
建模
格式
APP
新建
打开
保存
打印
文件
库浏览器
库
记录信号
添加查看器
信号表
准备
停止时间
10.0
普通
快速重启
步退
运行
步进
停止
仿真
数据检查器
查看结果
库浏览器
输入搜索词
库
搜索结果
Robotics System Toolbox
Robust Control Toolbox
ROS Toolbox
Sensor Fusion and Tracking Toolbox
SerDes Toolbox
SimEvents
Simscape
Foundation Library
Electrical
Electrical Elements
Capacitor
Diode
Electrical Reference
Gyrator
Ideal Transformer
Inductor
模型库
拖拽
untitled
Simulink-PS Converter
f(x) = 0
Solver Configuration
Electrical Reference
编辑器
PS-Simulink Converter
Scope
PS-Simulink Converter1
Spectrum Analyzer
Foundation Electrical Resources
1. Find electrical components in the Simscape Foundation Electrical library.
2. Find components from other domains in the Simscape library.
For more information, see Physical Modeling.
3. Connect the components to form a physical network.
For more information, see Essential Steps for Constructing a Physical Model.
4. Explore simulation results using Simscape Results Explorer
73%
VariableStepAuto

建立元件连接关系

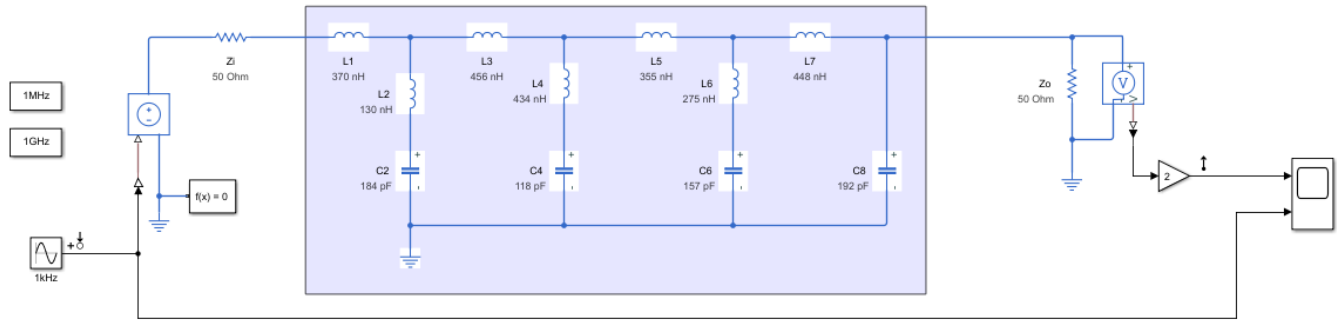

e_filter * - Simulink
仿真
调试
建模
格式
APP
新建
打开
保存
打印
文件
库浏览器
库
记录信号
添加查看器
信号表
准备
停止时间
10/fsin
加速
快速重启
步退
运行
步进
停止
仿真
数据
检查器
查看结果
e_filter
模型浏览器
属性检查器
按原理图建立电路连接
Zi
50 Ohm
L1
370 nH
L2
130 nH
L3
456 nH
L4
434 nH
L5
355 nH
L6
275 nH
L7
448 nH
C2
184 pF
C4
118 pF
C6
157 pF
C8
192 pF
Zo
50 Ohm
1MHz
1GHz
f(x) = 0
2
就绪
查看诊断
70%
ode23t

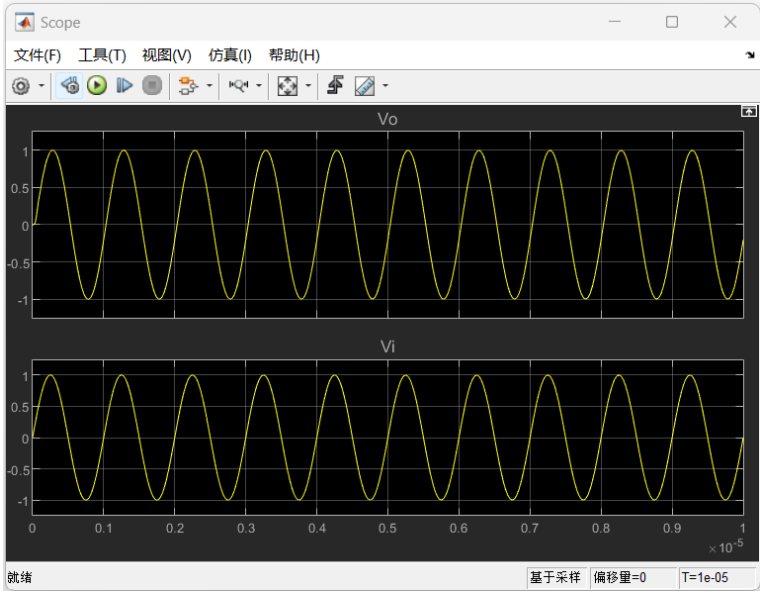
设置模块参数

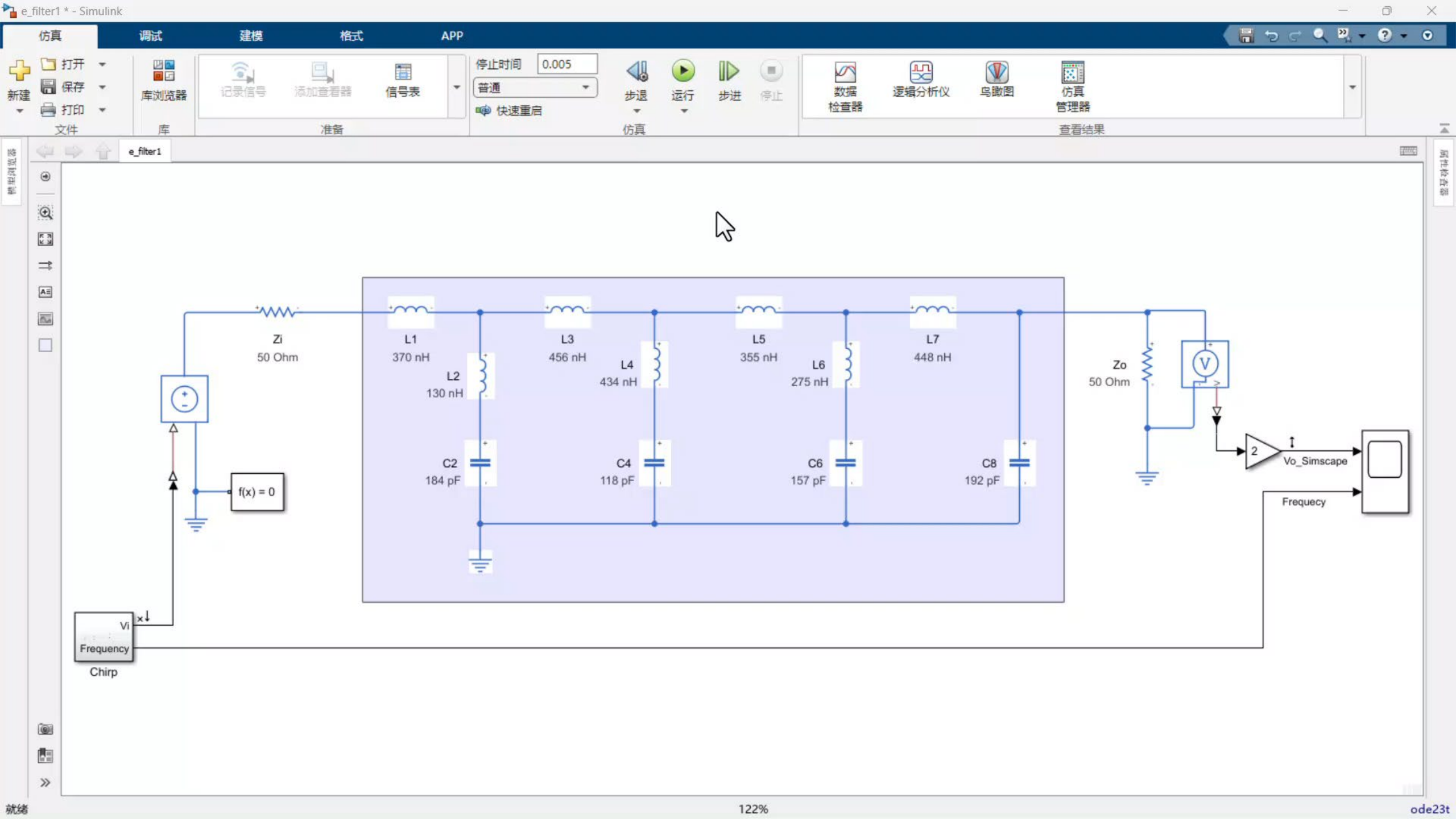

e_filter * - Simulink
仿真
调试
建模
格式
APP
SIMSCAPE 模块
新建
打开
保存
打印
文件
库浏览器
库
记录信号
添加查看器
信号表
准备
停止时间
10/fsin
加速
快速重启
步退
运行
步进
停止
仿真
数据
检查器
查看结果
e_filter
模型浏览器
属性检查器
设置模块参数
模块参数: L1
Inductor
自动应用
Settings
Description
名称
值
Main
Inductance
370
nH
Tolerance application
None - use nominal value
Series resistance
0
Ohm
Parallel conductance
1e-9
1/Ohm
Operating Limits
Faults
Initial Targets
Nominal Values
Zi
50 Ohm
L1
370 nH
L2
130 nH
C2
184 pF
1MHz
1GHz
f(x) = 0
就绪
查看诊断
70%
ode23t

电路分析

- 在Simulink中进行电路分析

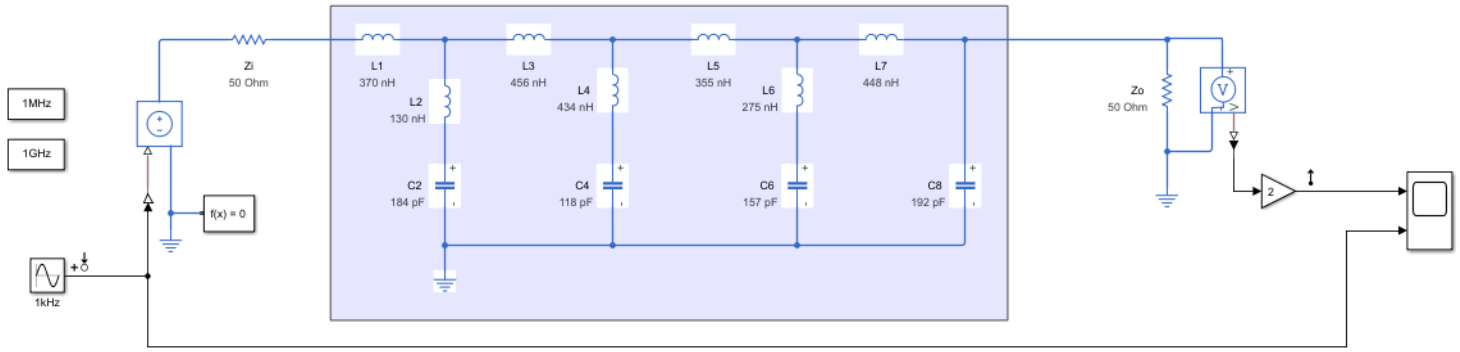




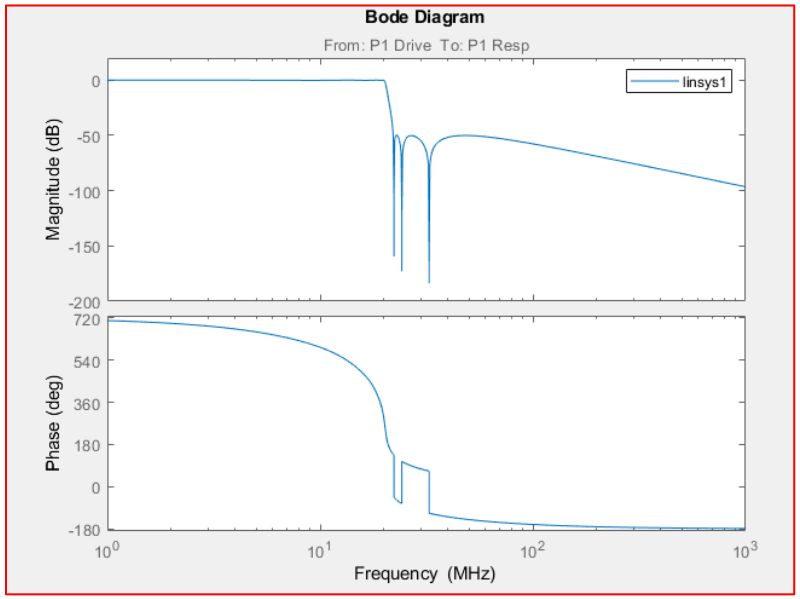

e_filter1 * - Simulink
仿真
调试
建模
格式
APP
新建
打开
保存
打印
文件
库浏览器
库
记录信号
添加查看器
信号表
准备
停止时间
0.005
普通
快速重启
步退
运行
步进
停止
仿真
数据检查器
逻辑分析仪
乌瞰图
仿真管理器
查看结果
e_filter1
Zi
50 Ohm
L1
370 nH
L2
130 nH
L3
456 nH
L4
434 nH
L5
355 nH
L6
275 nH
L7
448 nH
C2
184 pF
C4
118 pF
C6
157 pF
C8
192 pF
Zo
50 Ohm
f(x) = 0
2
Vo_Simscape
Frequecy
Vi
Frequency
Chirp
就绪
122%
ode23t

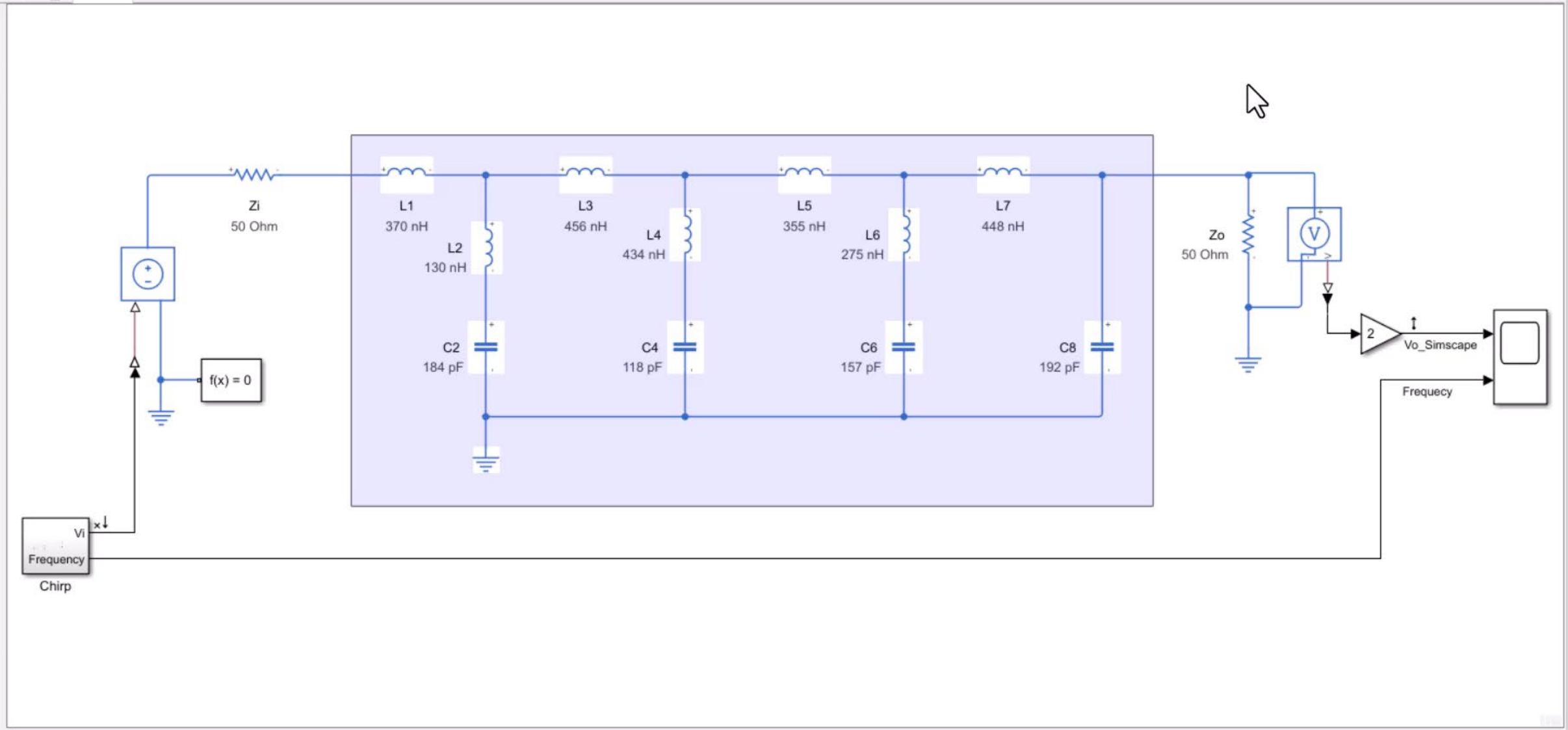
电路分析

- 在Simulink中进行电路分析



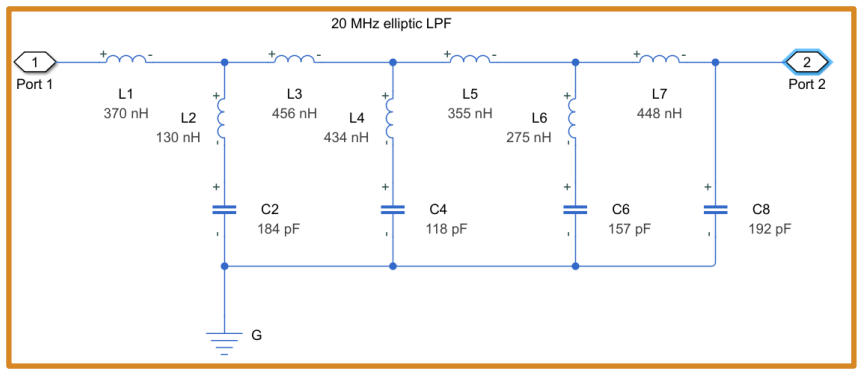

```
io     = getlinio(bdroot);
op     = operpoint(bdroot);
sys    = linearize(bdroot,io,op);

sys contains  A,B,C,D state-space matrices
```

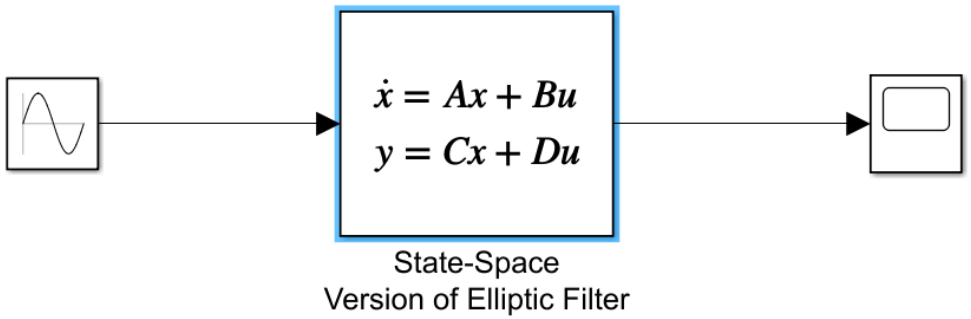


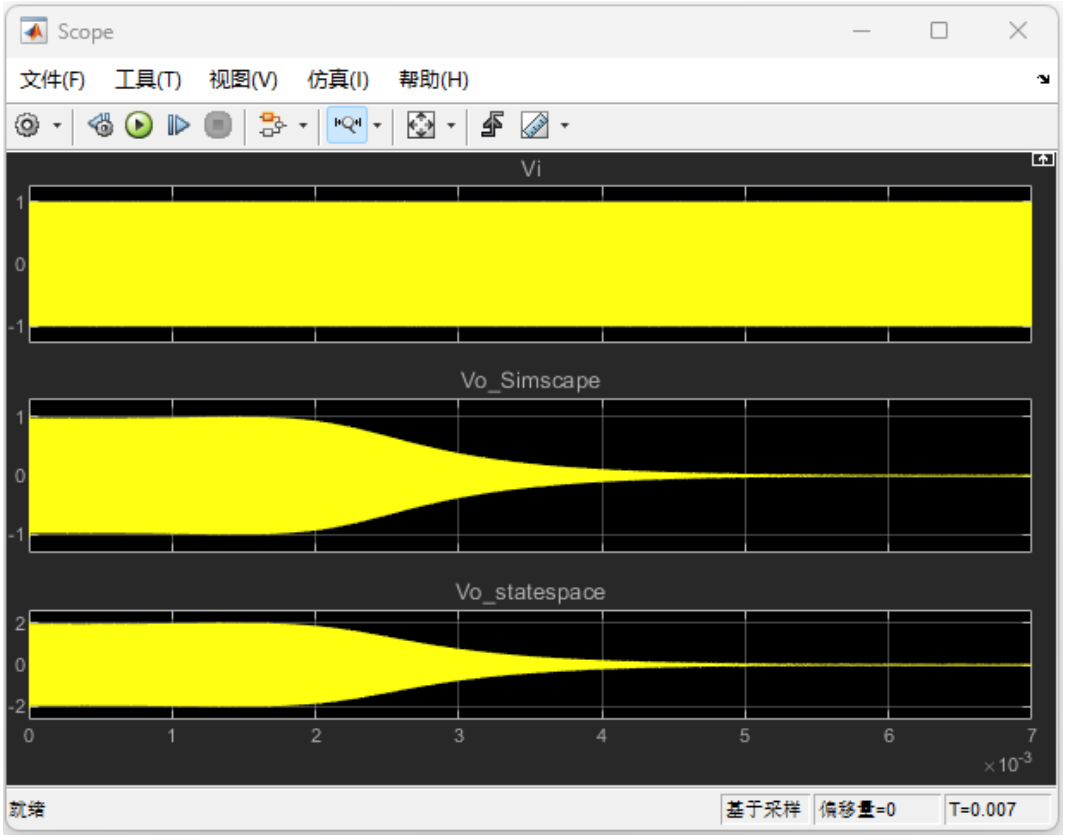

Zi
50 Ohm
L1
370 nH
L2
130 nH
L3
456 nH
L4
434 nH
L5
355 nH
L6
275 nH
L7
448 nH
C2
184 pF
C4
118 pF
C6
157 pF
C8
192 pF
Zo
50 Ohm
f(x) = 0
Vi
Frequency
Chirp
2
Vo_Simscape
Frequecy

电路分析

频域与时域仿真对比



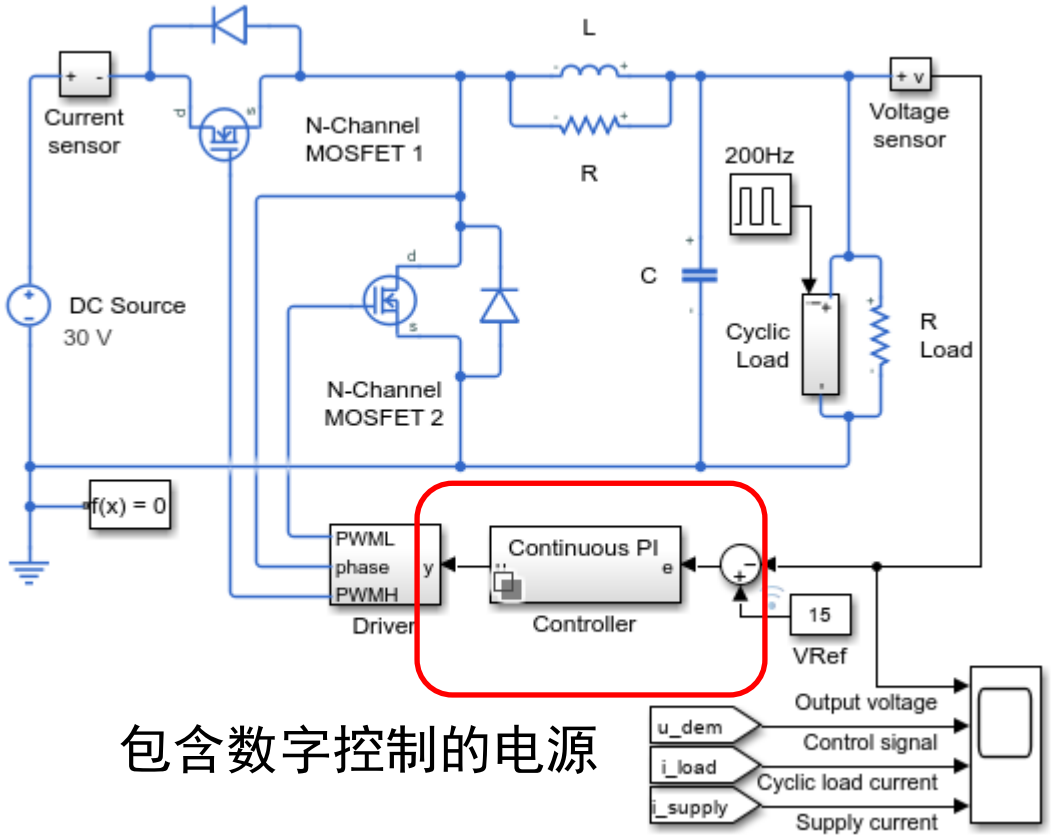




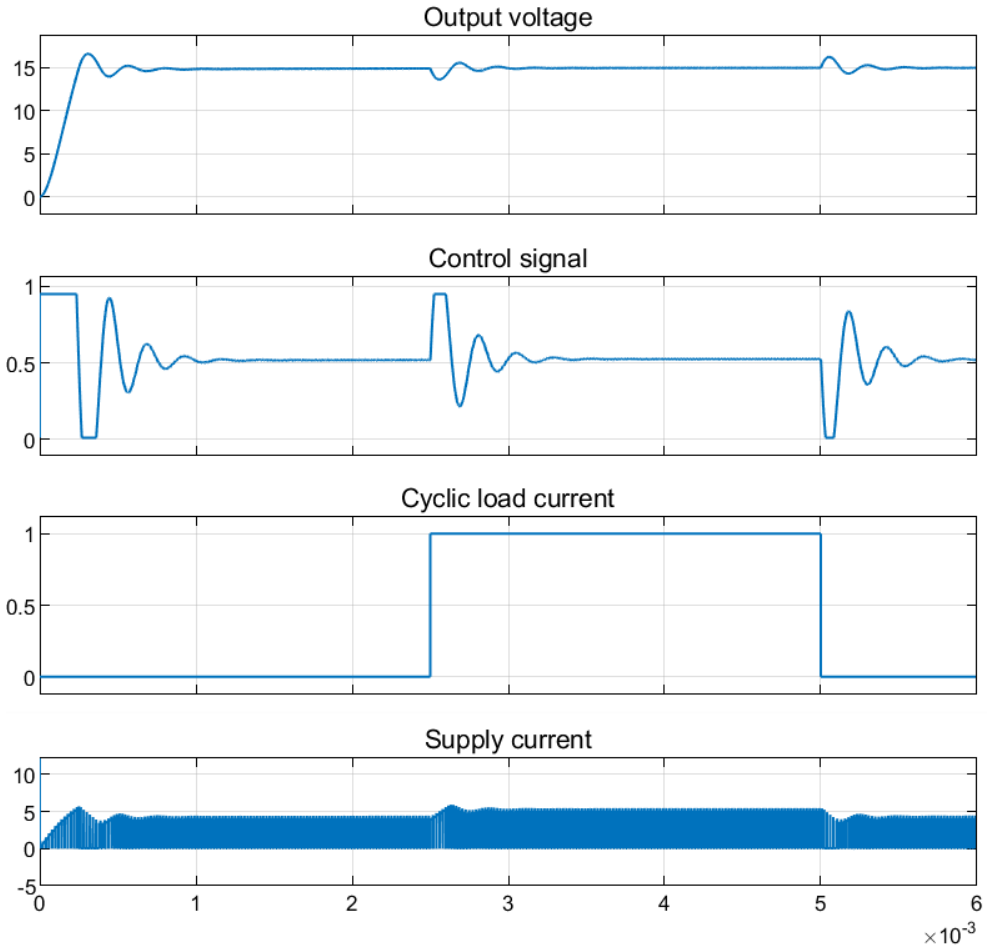
状态方程模型

电源系统设计

闭环仿真

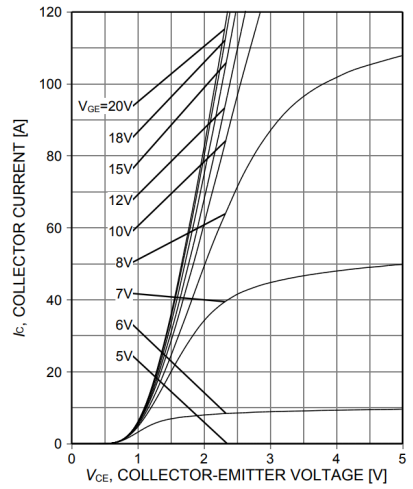


包含数字控制的电源

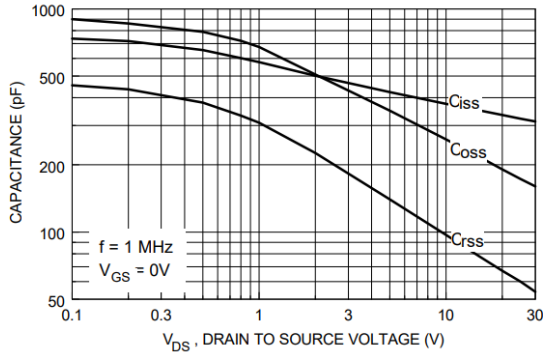


电源系统设计

精细化器件建模



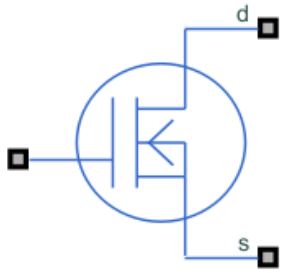
导通特性



开关断特性

从datasheet建模

动态、静态、温升



N-Channel MOSFET 1

暂态开关断性能
损耗与温升

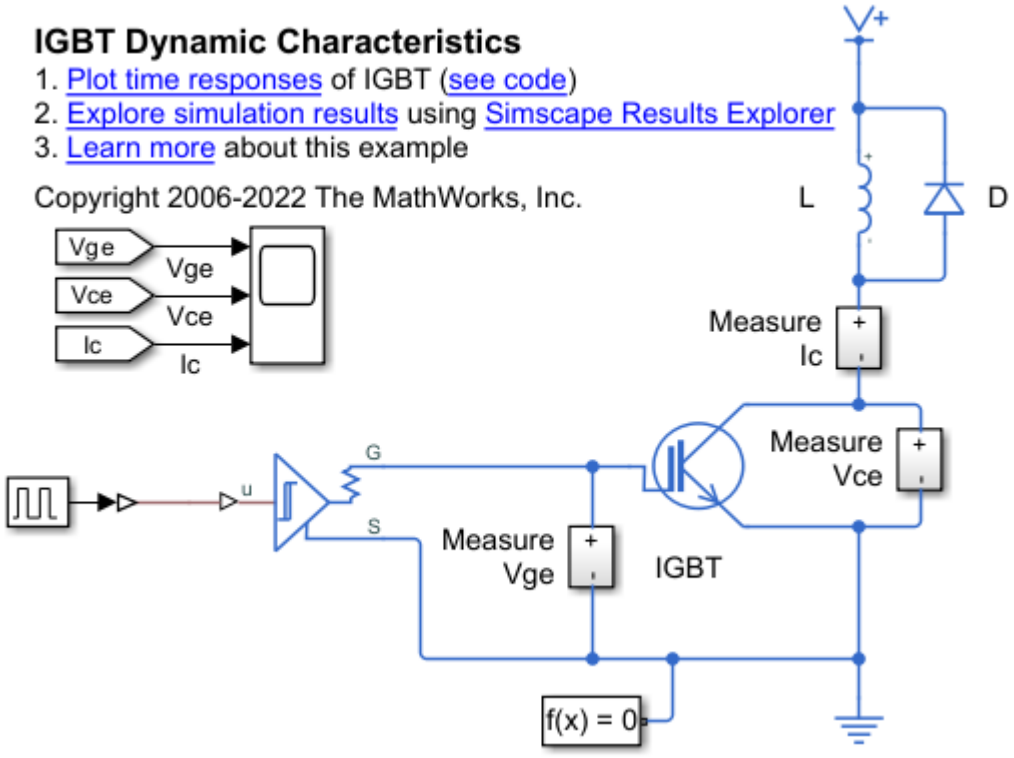
SPICE Simulator

利用SPICE Netlist

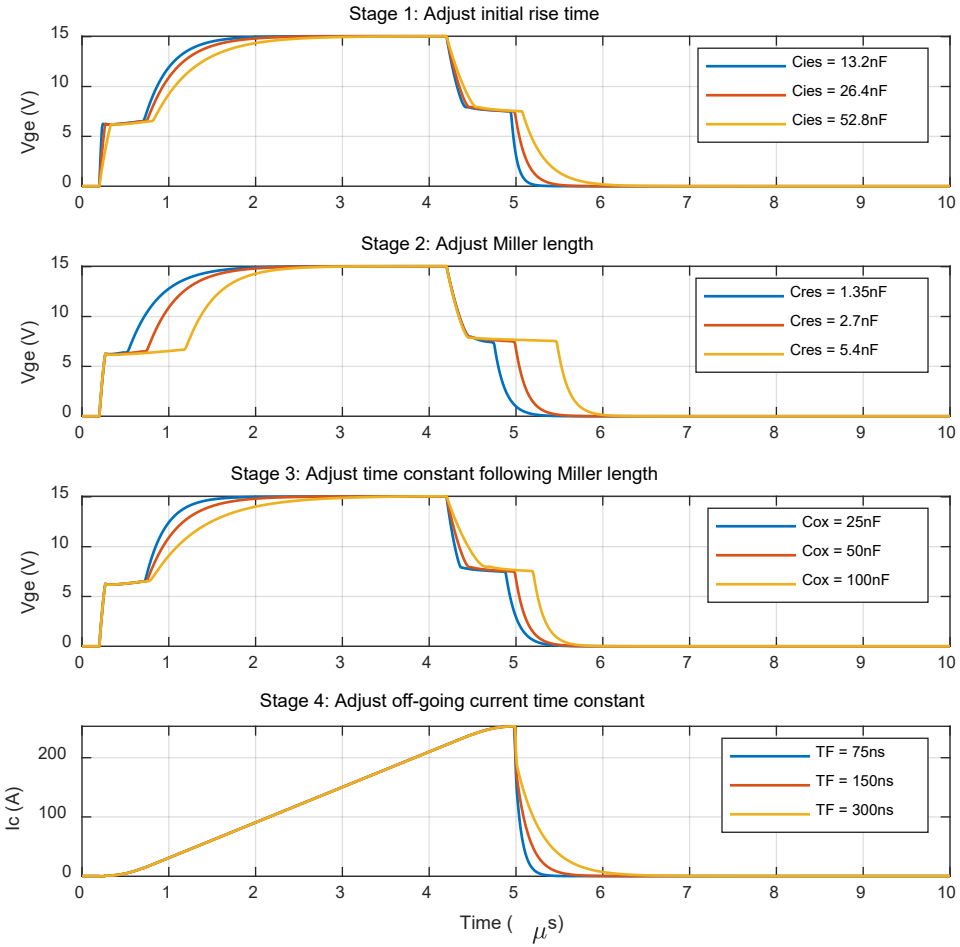
电源系统设计

功率器件特性模拟 - 双脉冲测试

驱动与功率器件



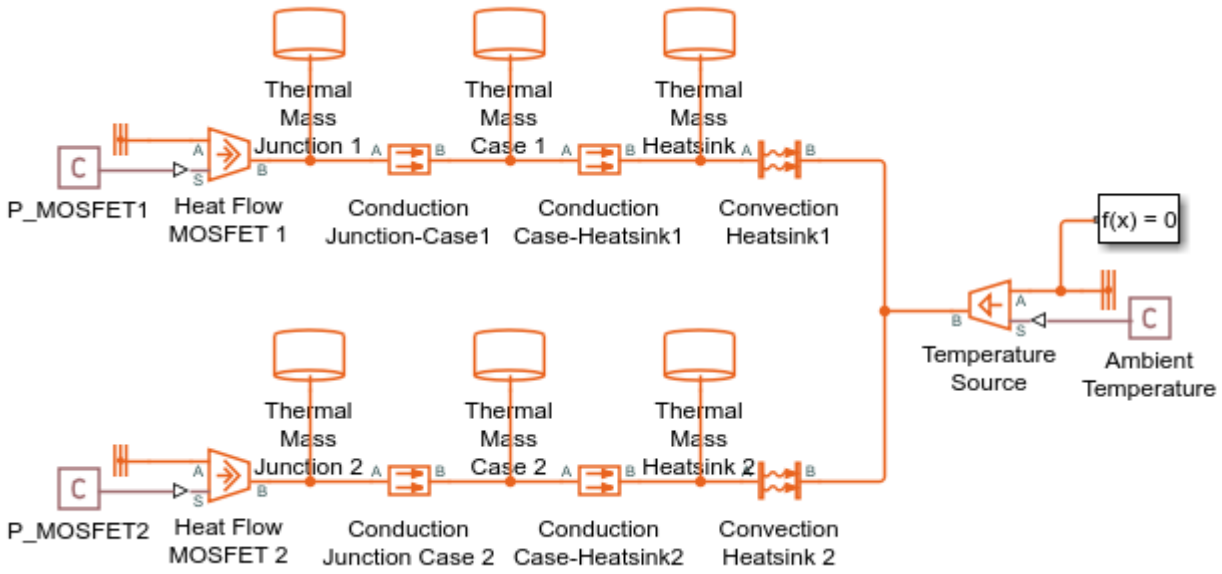
暂态仿真



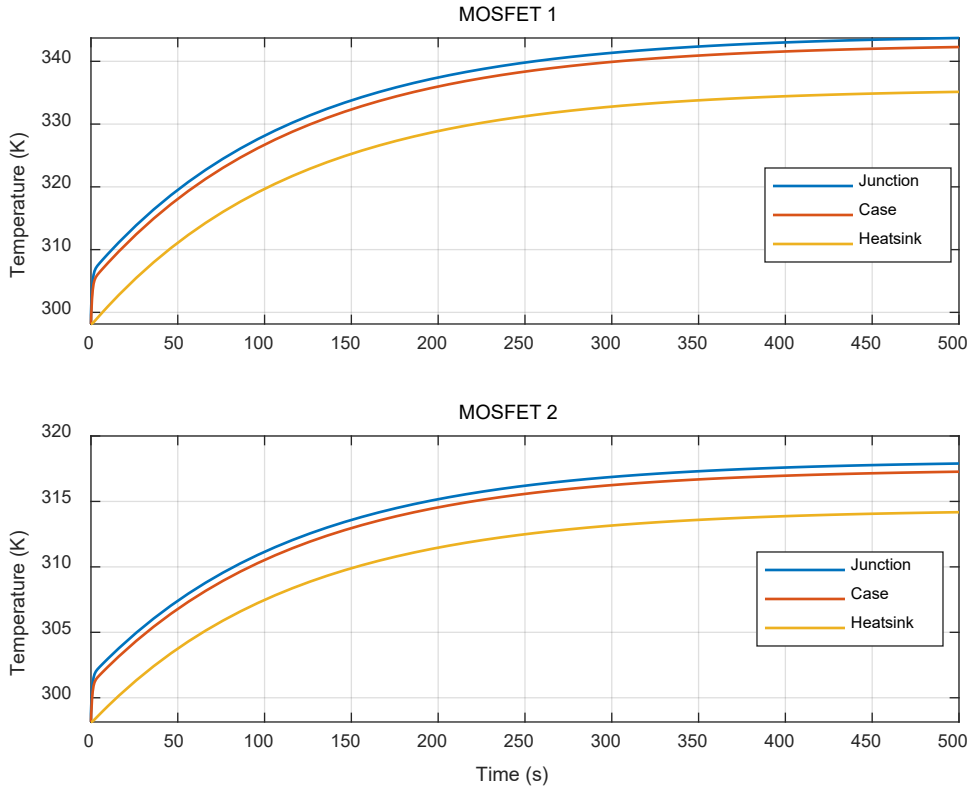
电源系统设计

电源温升建模

散热模型

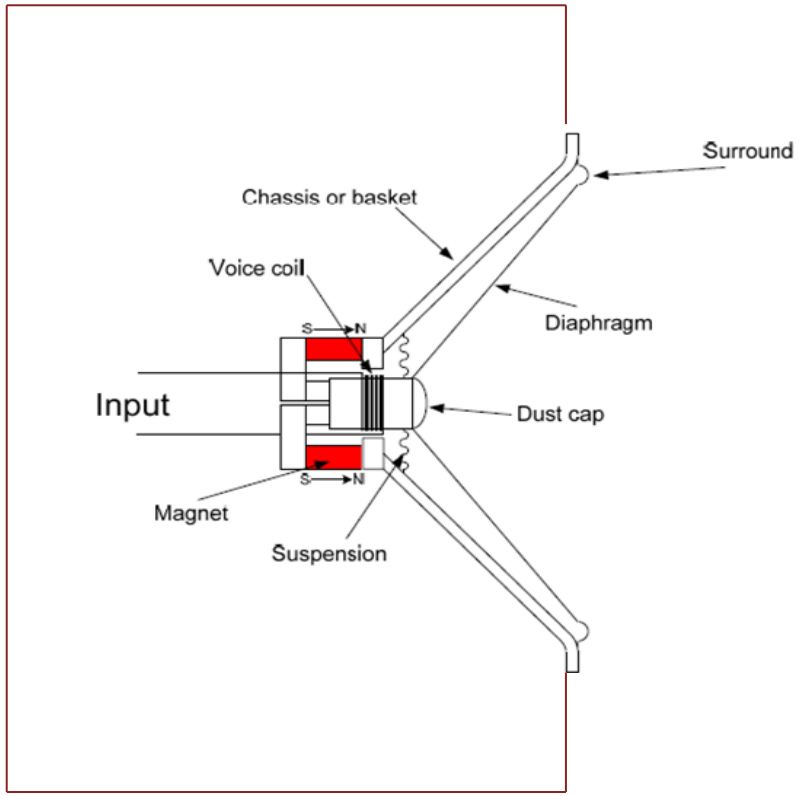


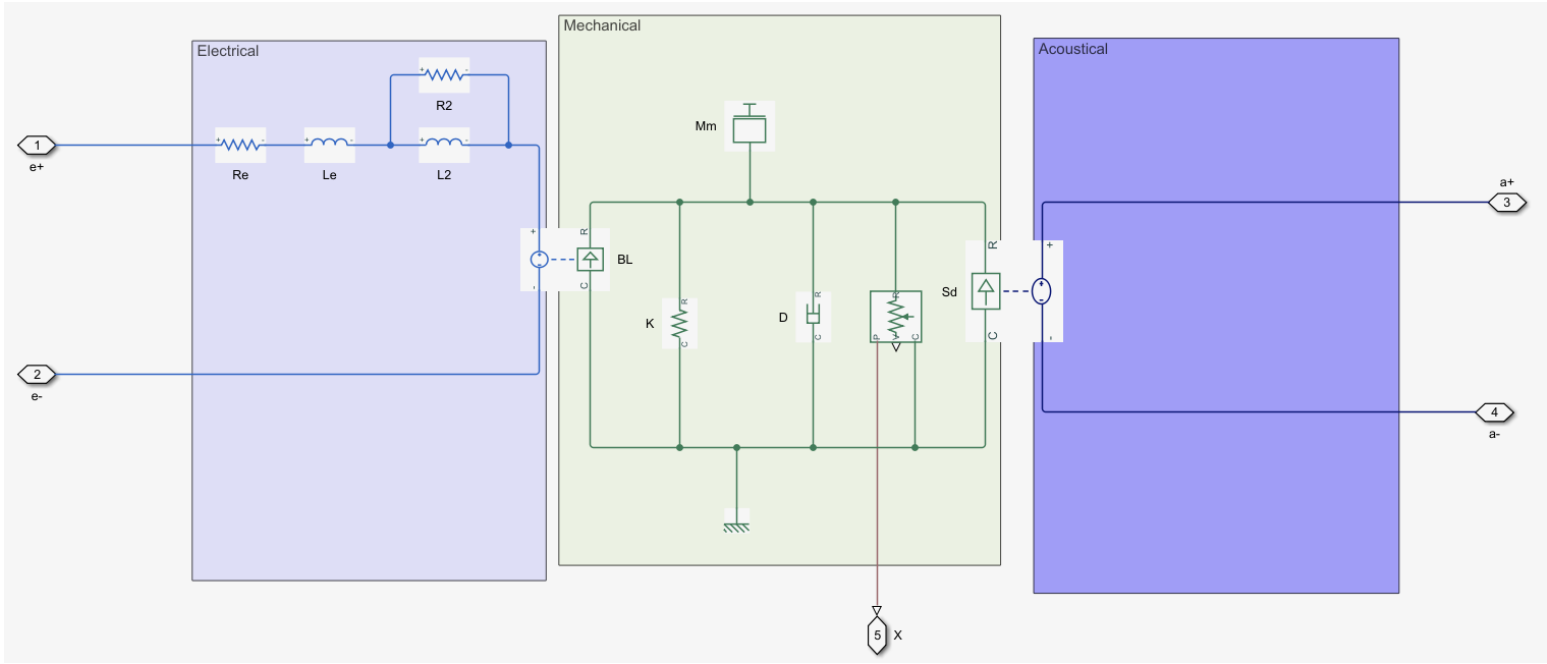
温升仿真



多物理域系统

扬声器





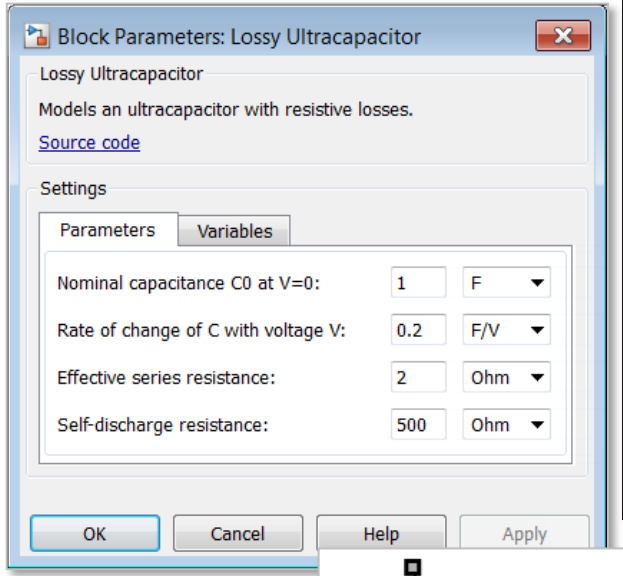
Electric circuit ↔ **Mechanic Movement** ↔ **Acoustic Domain**

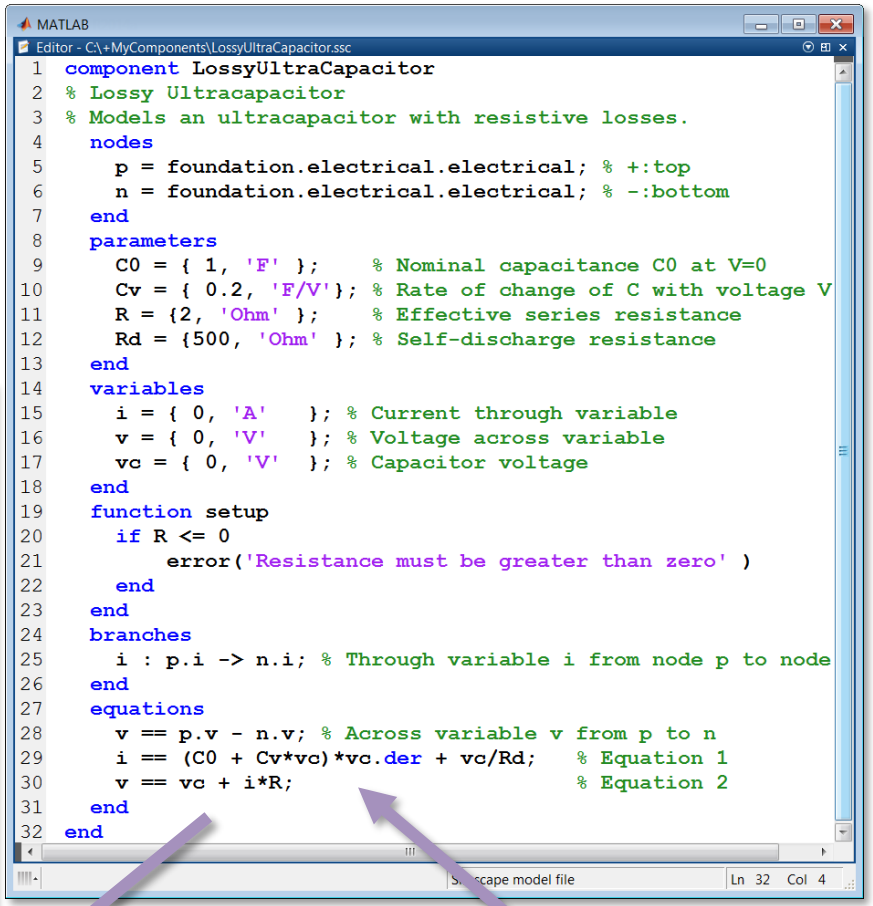
原生支持

Simscape Language 自定义

基于 Simscape Language 自定义元件

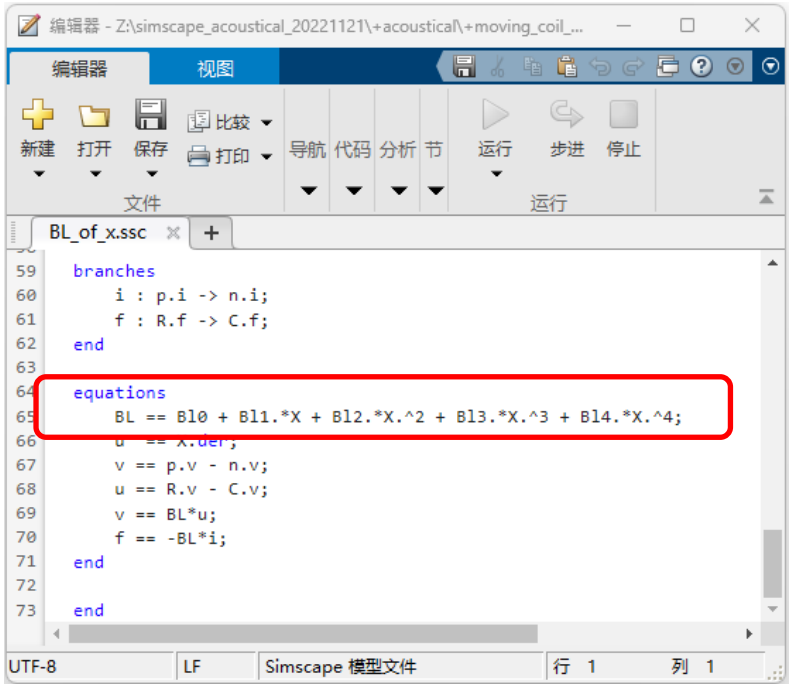
- 类MATLAB语言，定义物理域、元件和库
  - 基于MATLAB
  - 面型对象，方便重用
  - 生成Simulink模块
  - 支持二进制 IP 保护





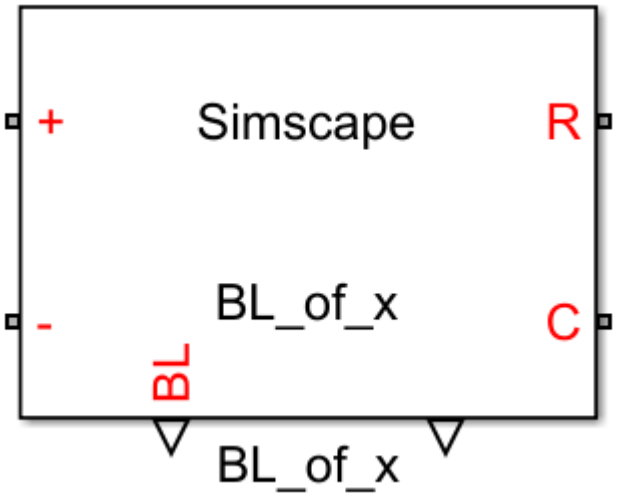
$$i = (C_0 + C_v v)\frac{dv}{dt} + \frac{v}{r_d}$$

自定义非线性互感元件



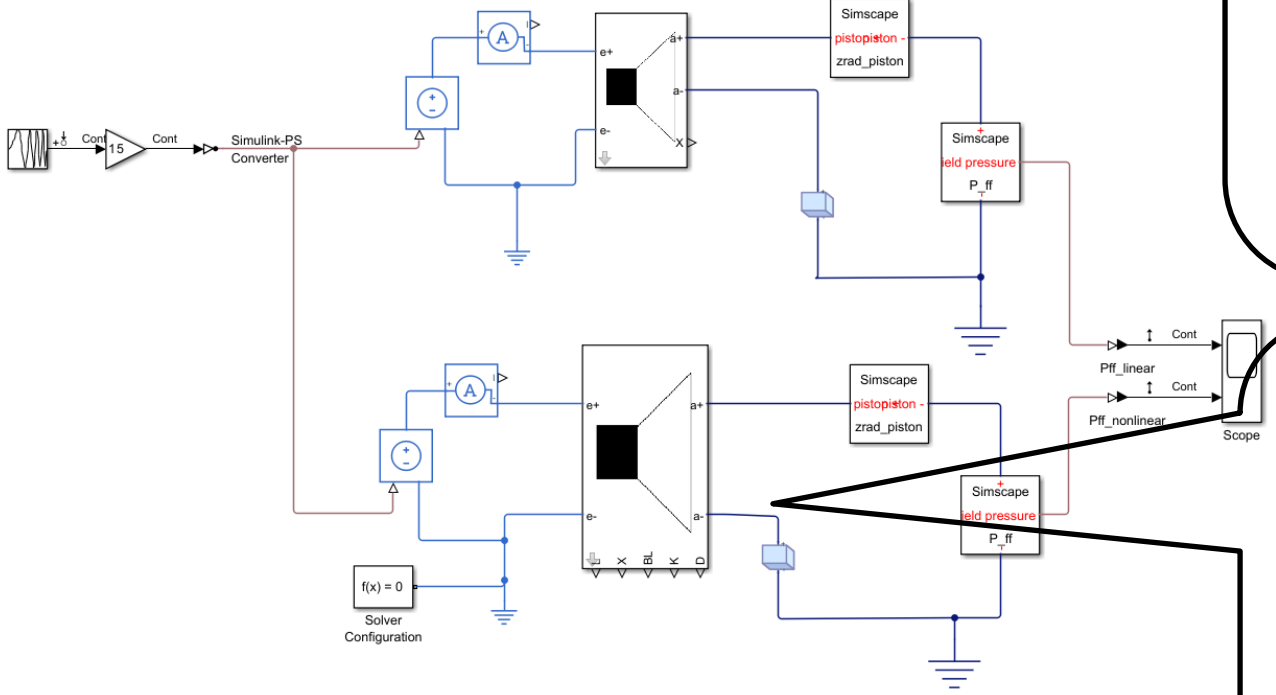
Simscape 语言定义模块方程

ssc_build

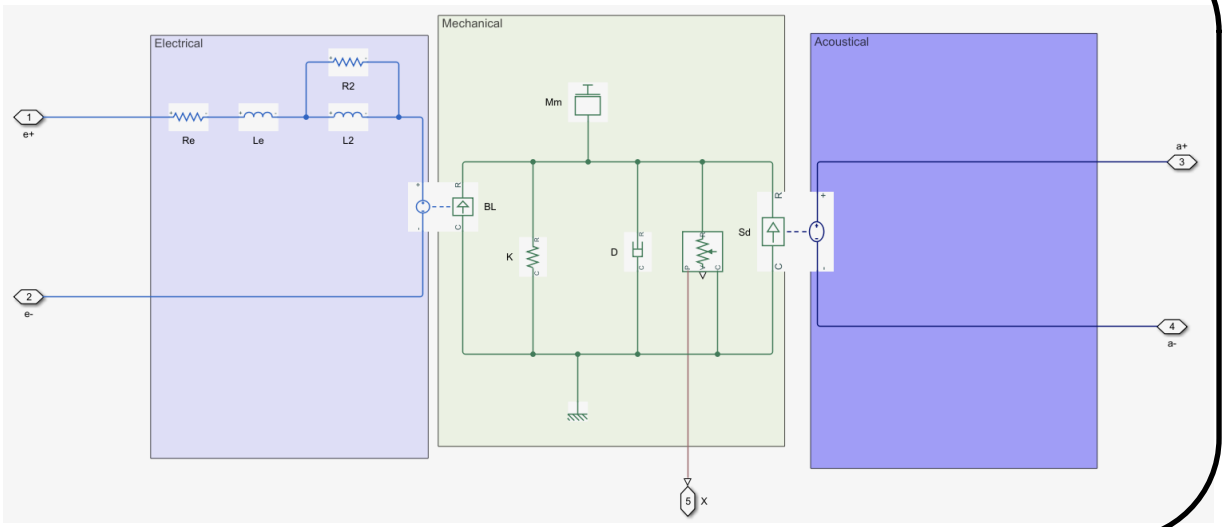


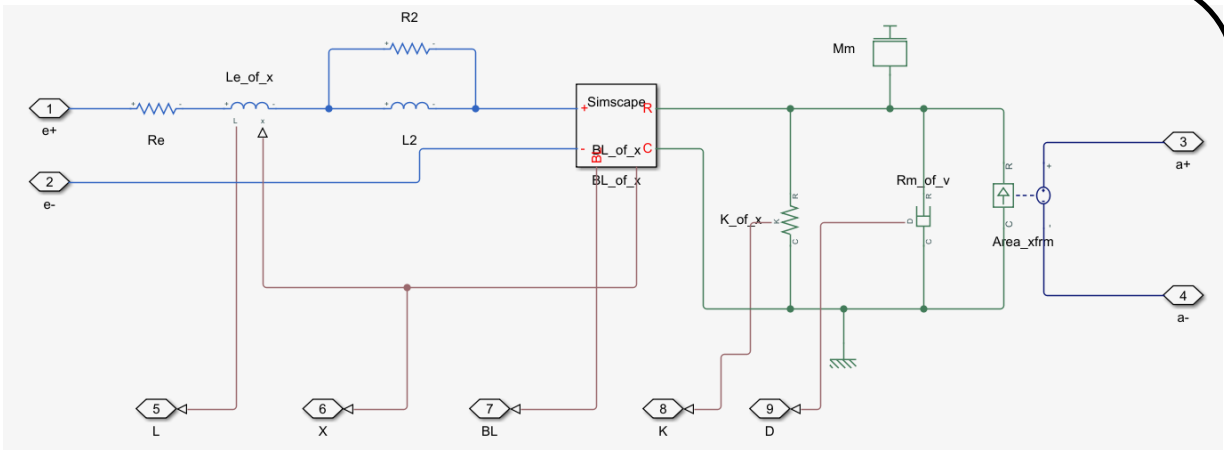
生成自定义互感模块

线性模型与非线性模型对比



线性模型

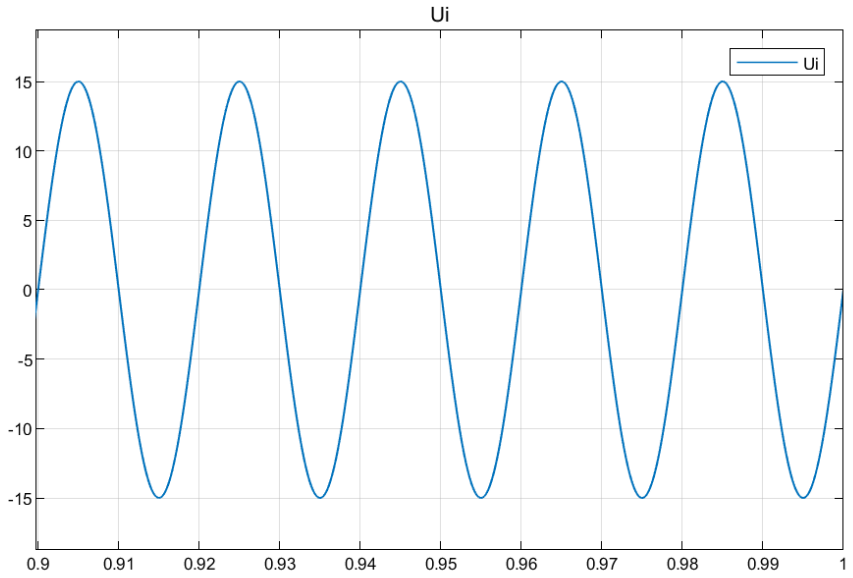


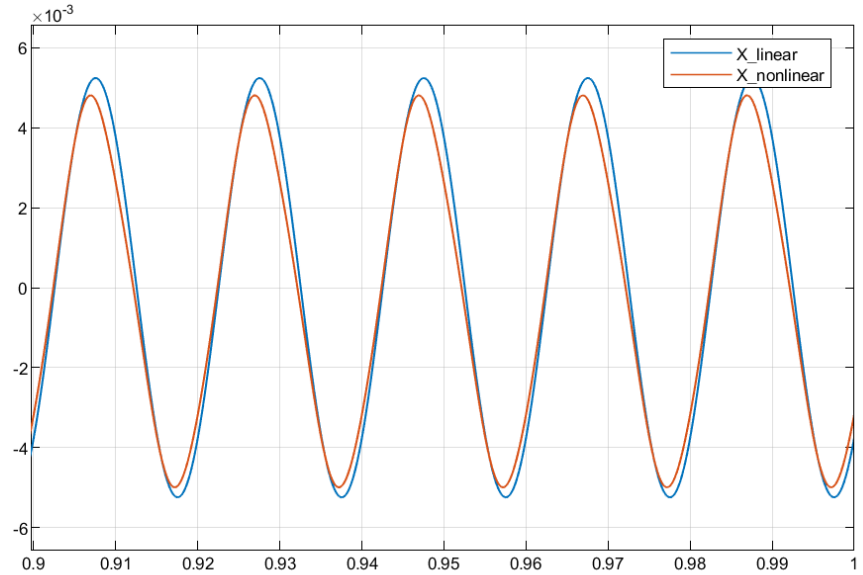


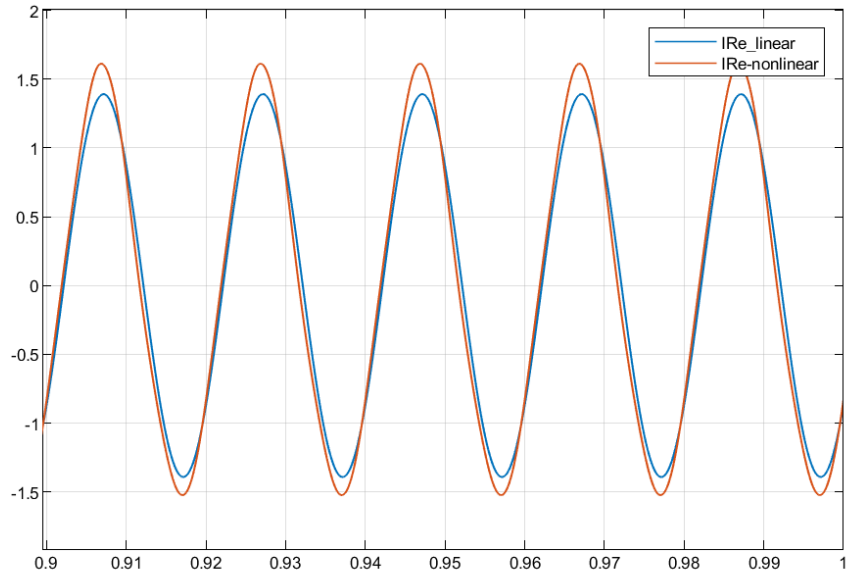
非线性模型

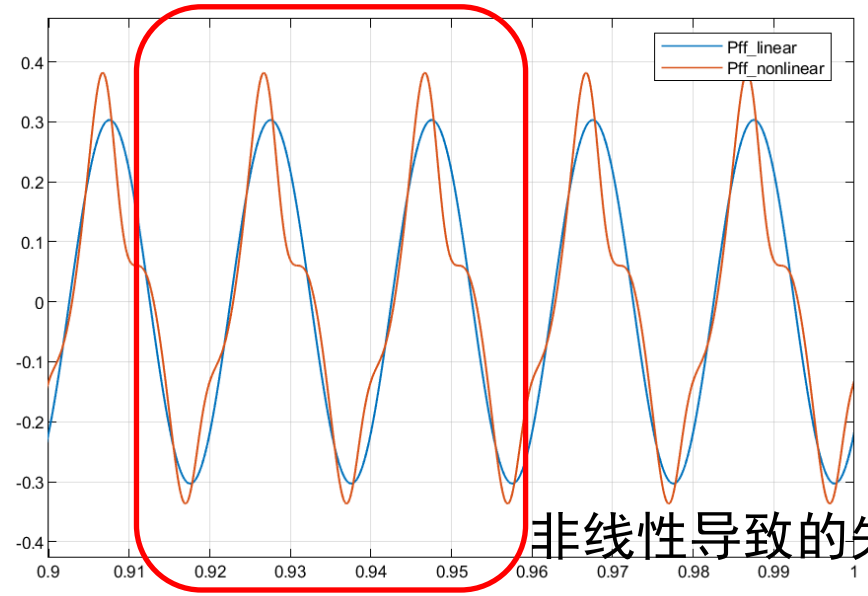
线性模型与非线性模型对比

- 非线性模型相对线性模型，在同样输入情况下电流、膜片位移和声压都有不同程度的失真









非线性导致的失真

Agenda

- 基于 Simscape 的电路仿真
- 射频电路仿真
- 高速电路信号完整性仿真

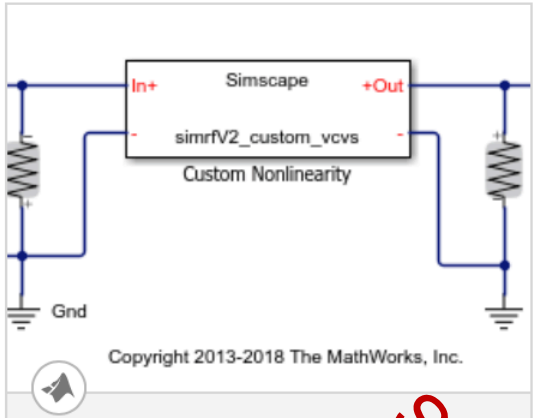
MathWorks 射频电路设计应用的四个特点：

- ✓ MATLAB& Simulink强大的建模能力：数学公式级/数据拟合行为级
- ✓ 灵活的系统链路实现方式
- ✓ 与通信算法的总体考量
- ✓ 独立小程序的开发及发布

- ➢ 模块/芯片厂家的模型简单或者难以获取，传统工具提供的库或者PDK有限
- ➢ 传统工具只能采用传统的拖拽方式搭建链路，不方便在不同版本间设计迭代和共享
- ➢ 传统工具很难提供和算法的统一考量
- ➢ 传统工具无法支持独立应用程序开发

案例1 使用Simscape创建模型

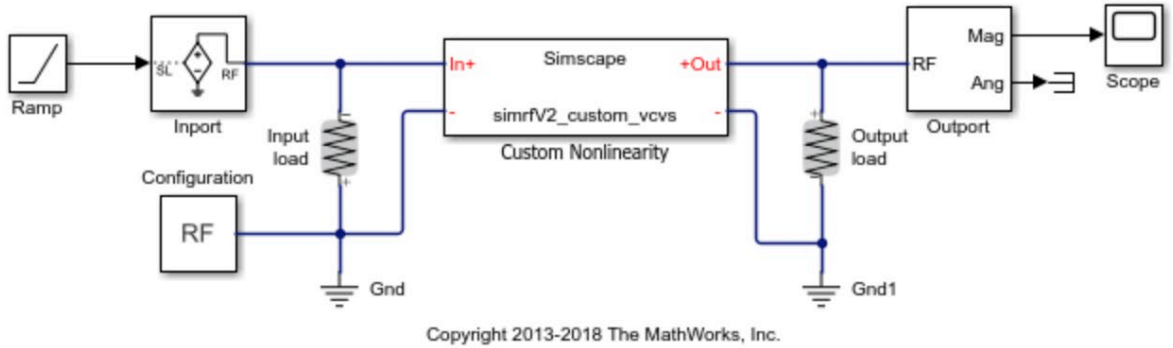
Featured Examples



Create Custom RF Blockset Models

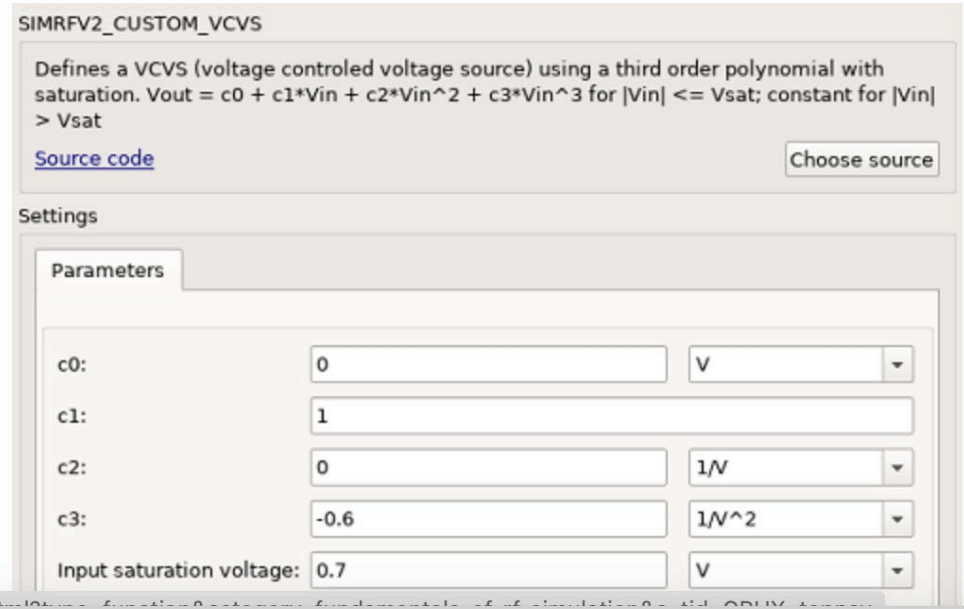
Write your own RF Blockset™ Circuit Envelope model in Simscape® language for complex baseband simulation.

Shipping Demo



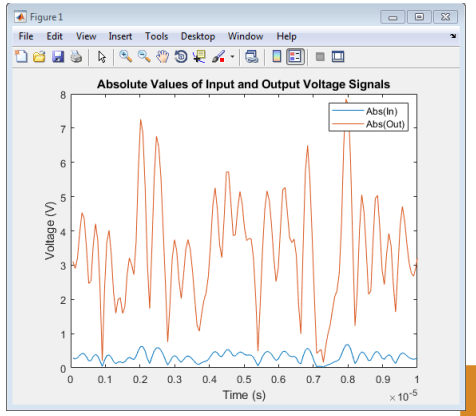
Examine the Model

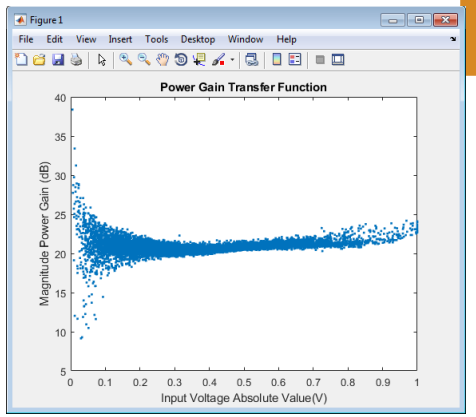
Double-click the "Custom Nonlinearity" block or type `open_system([model '/Custom Nonlinearity'])` in the commar



案例2 PA 模型的创建

PA Data

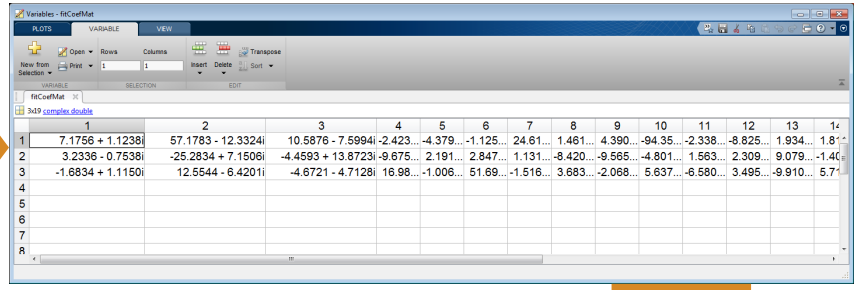




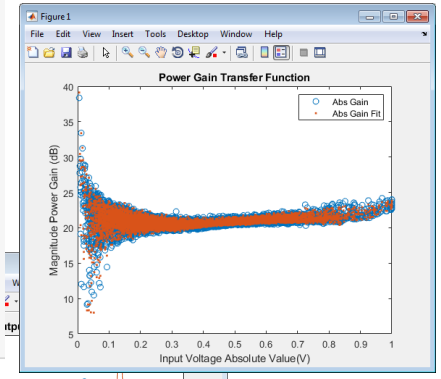
MATLAB fitting procedure (White box)

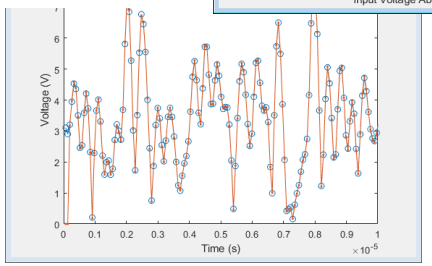
```
function a_coef = fit_memory_poly_model(x,y,memLen,degLen,modType)
% FIT_MEMORY_POLY_MODEL
%   Procedure to compute a coefficient matrix given input and output
%   signals, memory length, nonlinearity degree, and model type.
%
%   Copyright 2017 MathWorks, Inc.

x = x(:);
y = y(:);
xLen = length(x);

switch modType
  case 'memPoly'  % Memory polynomial
    xrow = reshape((memLen:-1:1)' + (0:xLen:xLen*(degLen-1)),1,[]);
    xVec = (0:xLen-memLen)' + xrow;
    xPow = x.*(abs(x).^(0:degLen-1));
    xVec = xPow(xVec);
  case 'ctMemPoly'  % Cross-term memory polynomial
    absPow = (abs(x).^(1:degLen-1));
    partTop1 = reshape((memLen:-1:1)'+(0:xLen:xLen*(degLen-2)),1,[]);
    topPlane = reshape(                                              ...
        [ones(xLen-memLen+1,1),absPow((0:xLen-memLen)' + partTop1)].',  ...
        1,memLen*(degLen-1)+1,xLen-memLen+1);
    sidePlane = reshape(x((0:xLen-memLen)' + (memLen:-1:1)).',       ...
        memLen,1,xLen-memLen+1);
    cube = sidePlane.*topPlane;
    xVec = reshape(cube,memLen*(memLen*(degLen-1)+1),xLen-memLen+1).';
end

coef = xVec\y(memLen:xLen);
a_coef = reshape(coef,memLen,numel(coef)/memLen);
```

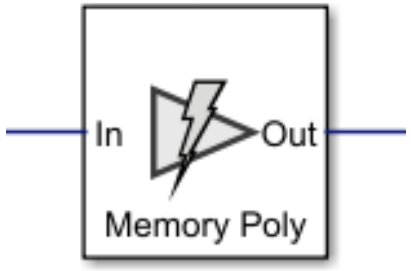
PA model coefficients



	1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	7.1756 + 1.1238i	57.1783 - 12.3324i	10.5876 - 7.5994i	-2.423...	-4.379...	-1.125...	24.61...	1.461...	4.390...	-94.35...	-2.338...	-8.825...	1.934...	1.8...
2	3.2336 - 0.7538i	-25.2834 + 7.1506i	-4.4593 + 13.8723i	-9.675...	2.191...	2.847...	1.131...	-8.420...	-9.565...	-4.801...	1.563...	2.309...	9.079...	-1.4...
3	-1.6834 + 1.1150i	12.5544 - 6.4201i	-4.6721 - 4.7128i	16.98...	-1.006...	51.69...	-1.516...	3.683...	-2.068...	5.637...	-6.580...	3.495...	-9.910...	5.7...
4														
5														
6														
7														
8														







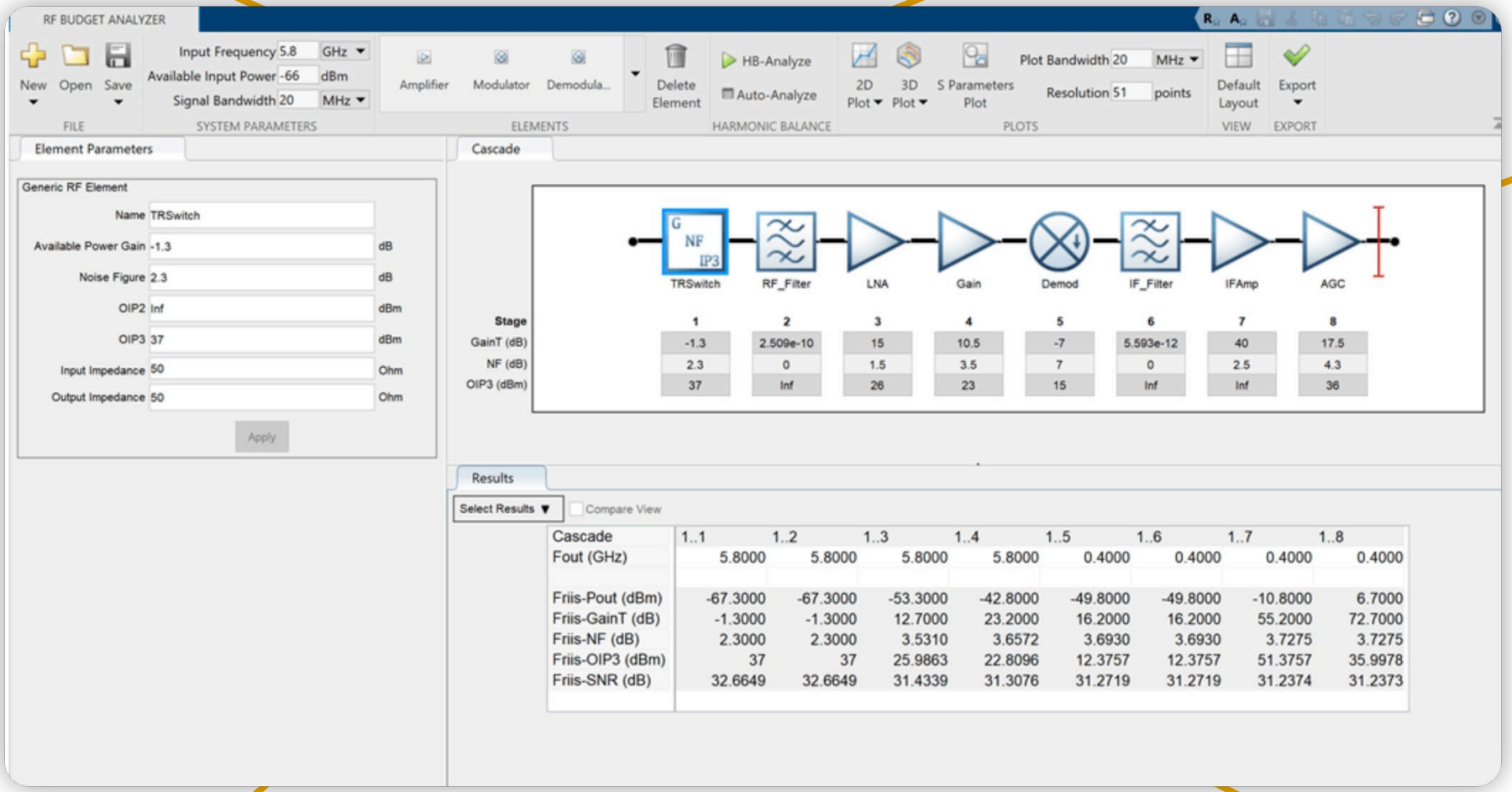
PA model for circuit envelope simulation

案例3： 利用RF Budget Analyzer快速创建RF系统链路

Add RF components

Export to MATLAB / RF Blockset

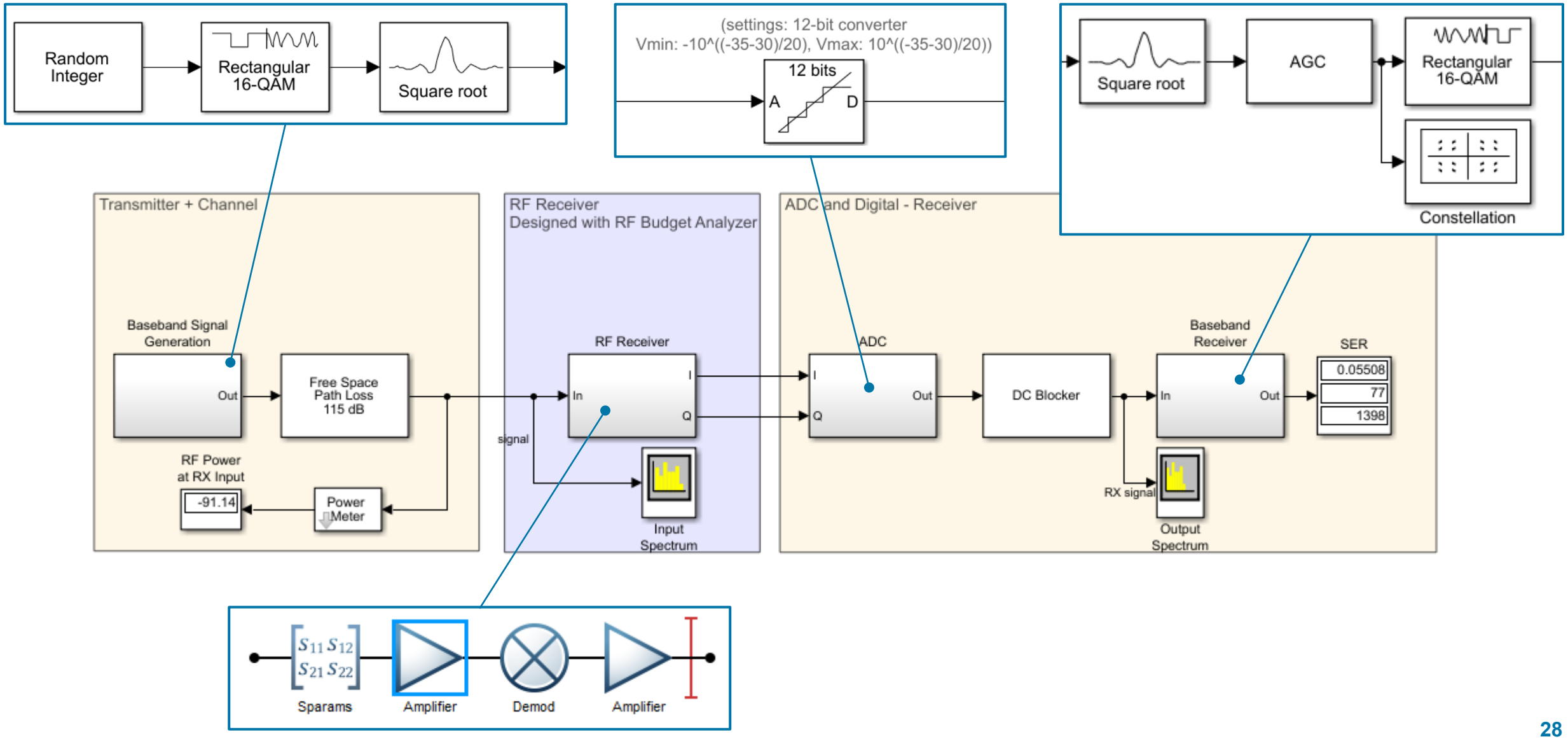
RF Cascade



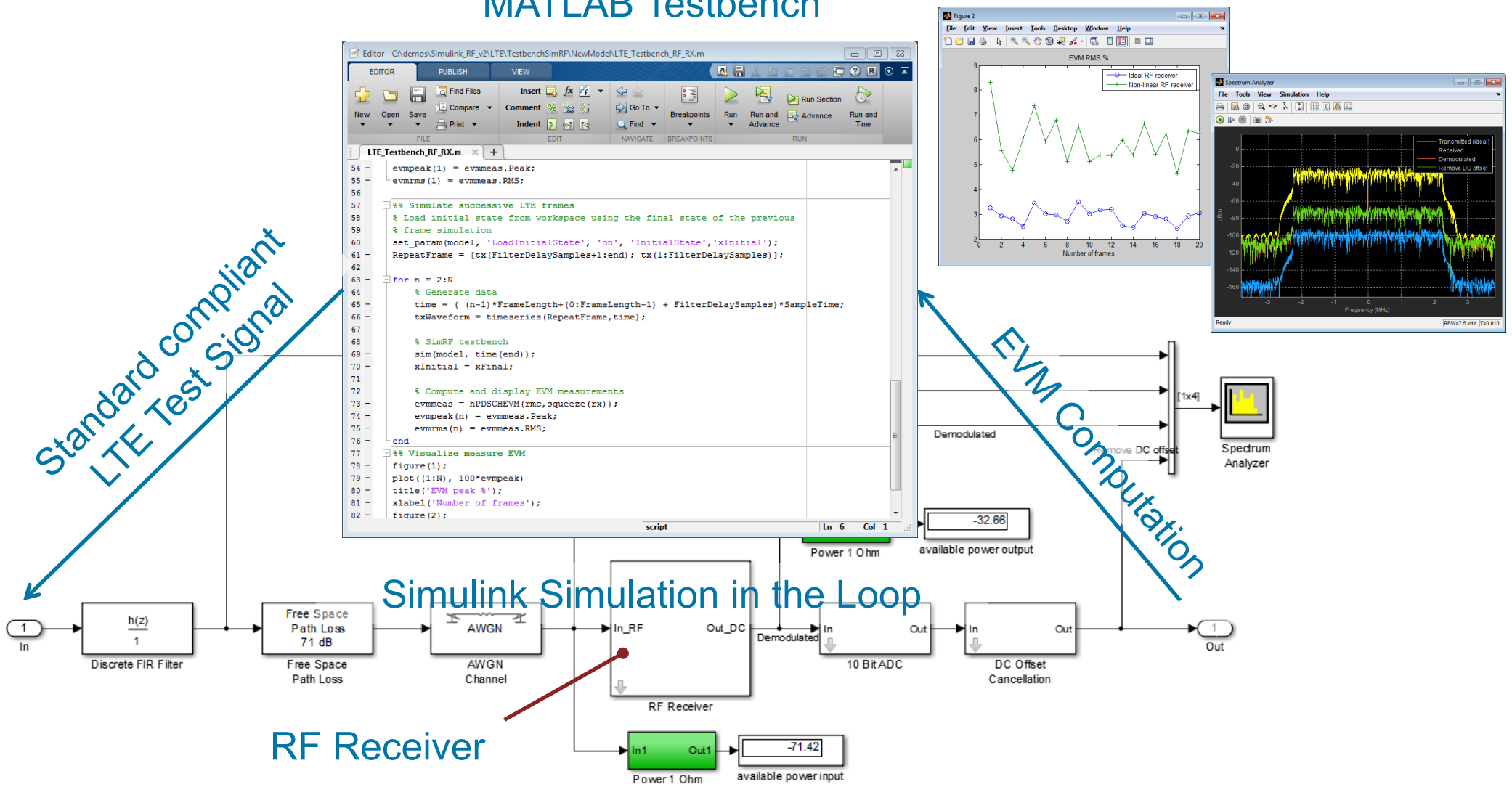
Component specifications

Cascade Budget Analysis

案例3： 利用RF Budget Analyzer快速创建RF系统链路



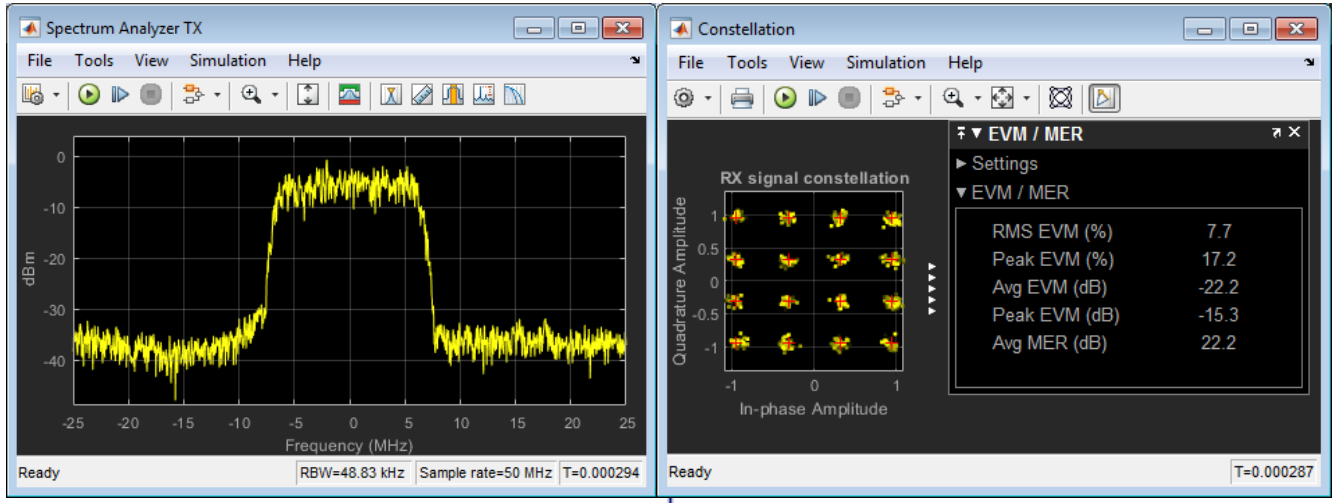
案例3 RF Receiver Integrated in MATLAB Testbench

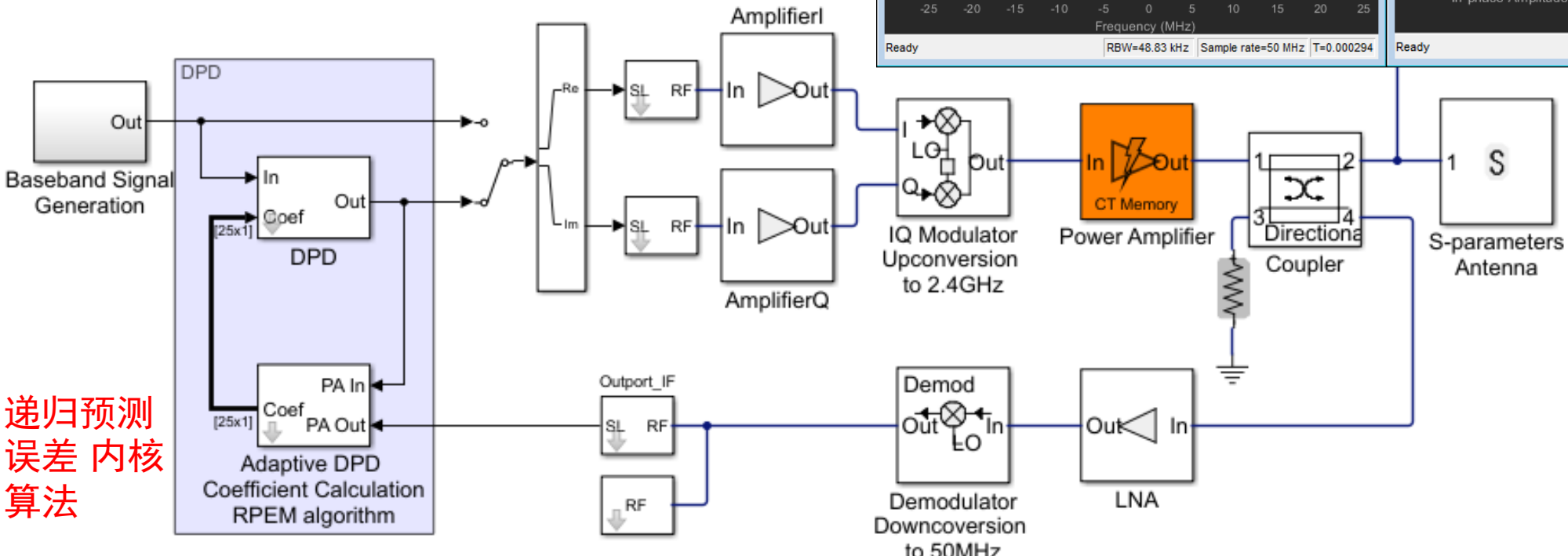


https://www.mathworks.com/help/lte/examples/modeling-and-testing-an-lte-rf-receiver.html

案例4 PA + DPD Simulation

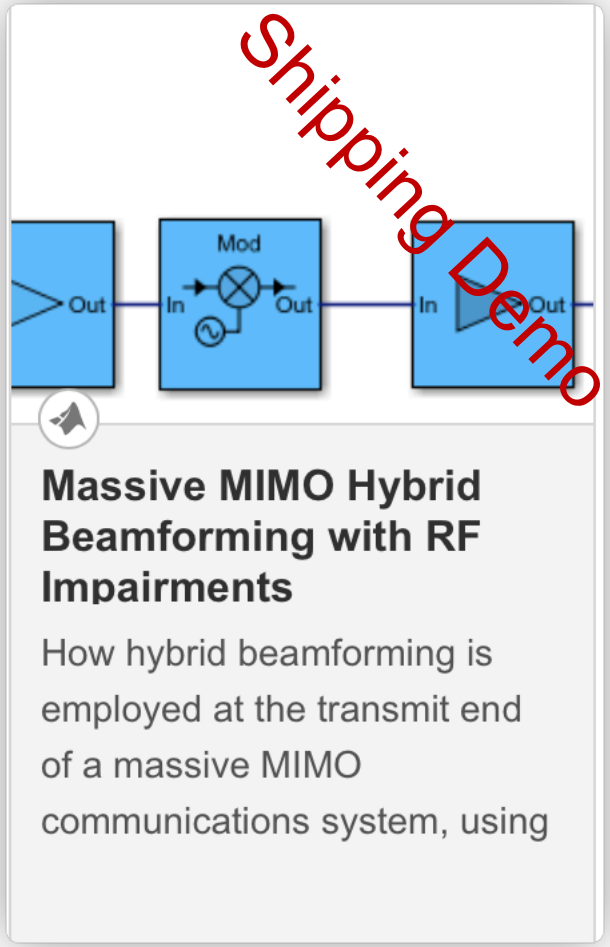
- Circuit Envelope for fast RF simulation
- Low-power RF and analog components
  - Up-conversion / down-conversion
  - Antenna load
- Digital signal processing algorithm: DPD

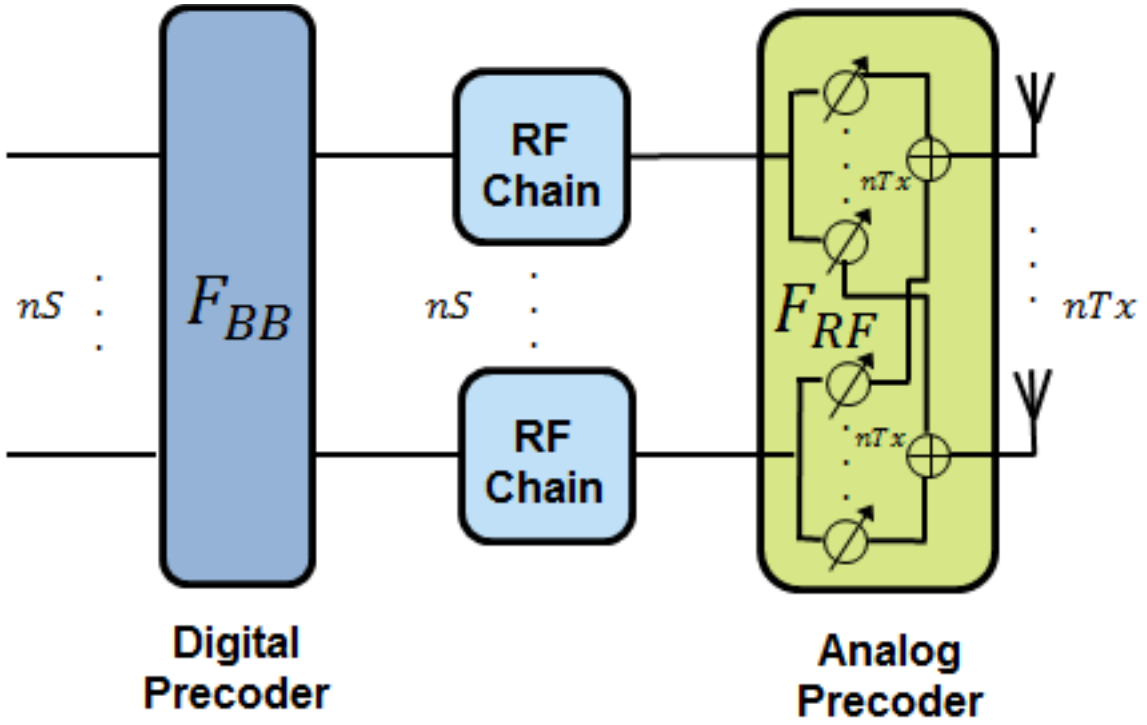




递归预测误差 内核算法

案例5 混合波束成形算法和RF链路的集成

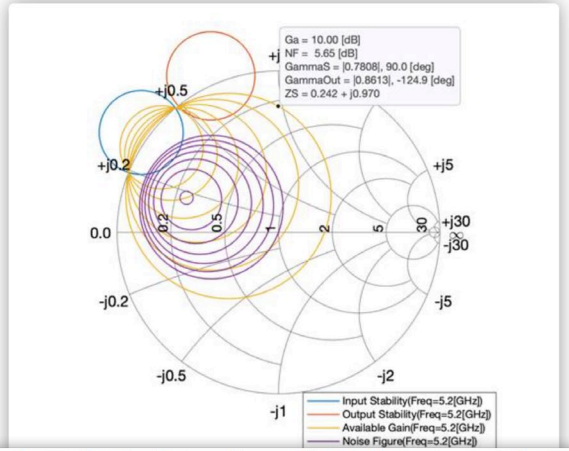




其他电路层面的应用

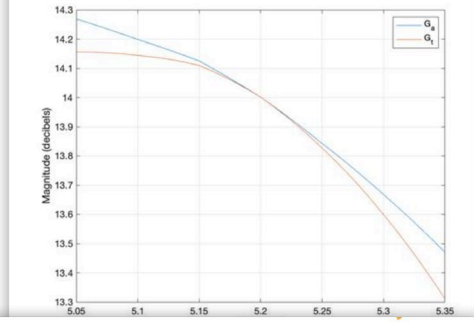
LNA阻抗匹配网络

Demo：RF Toolbox “Designing Matching Networks (Part 1: Networks with an LNA and Lumped Elements)"

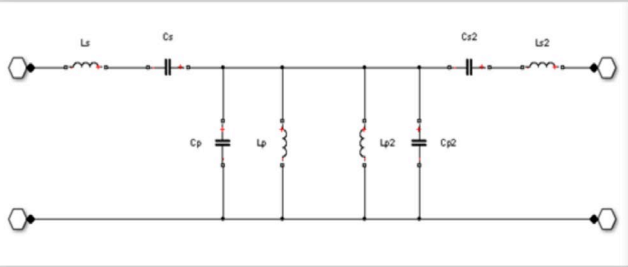



```
input_match = rfckt.cascade('Ckts', ...
    {rfckt.shuntrlc('C',Cin),rfckt.seriesrlc('L',Lin)});
output_match = rfckt.cascade('Ckts', ...
    {rfckt.seriesrlc('L',Lout),rfckt.shuntrlc('C',Cout)});
LNA = rfckt.cascade('ckts', ...
    {input_match,unmatched_amp,shunt_r,output_match});
```

```
analyze(LNA,5.05e9:10e6:5.35e9);
plot(LNA,'Ga','Gt','dB');
```

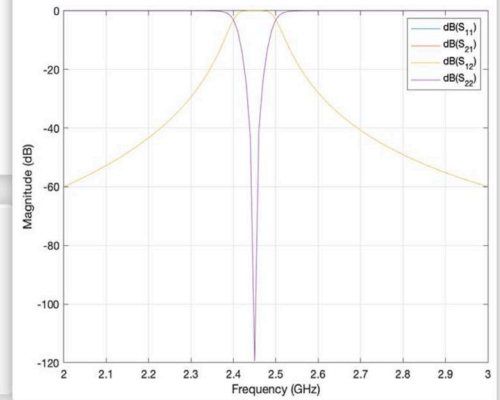


滤波器设计

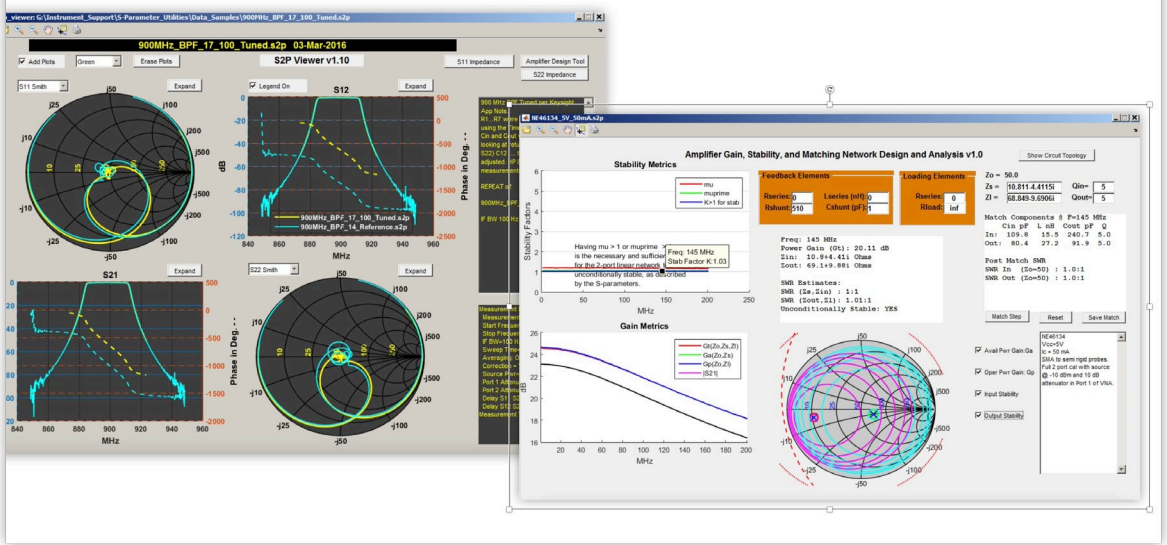



```
Ro = 50;
f1C = 2400e6;
f2C = 2500e6;

Ls = (Ro / (pi*(f2C - f1C)))/2;
Cs = 2*(f2C - f1C)/(4*pi*Ro*f2C*f1C);

Lp = 2*Ro*(f2C - f1C)/(4*pi*f2C*f1C);
Cp = (1/(pi*Ro*(f2C - f1C)))/2;
```

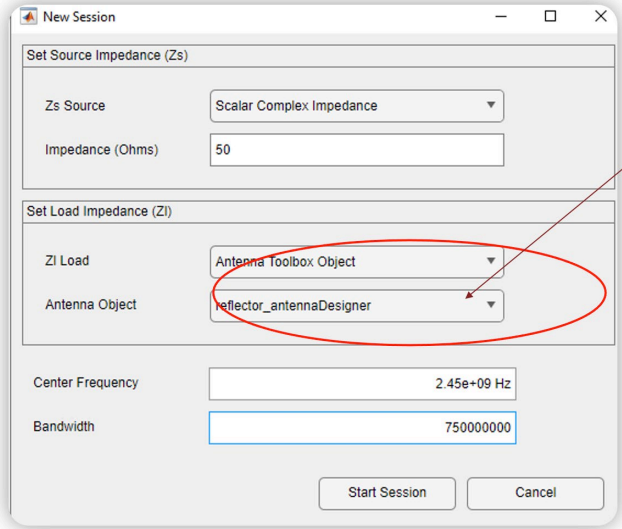
```
freq = linspace(2e9,3e9,101);
setports(ckt,[2 1],[6 1])
S = sparameters(ckt,freq);
rfplot(S)
```

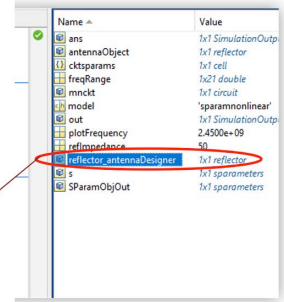


独立应用程序的开发，满足内部不同应用



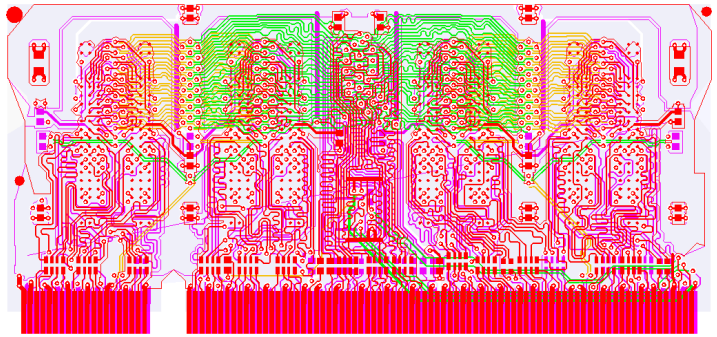
天线匹配网络设计



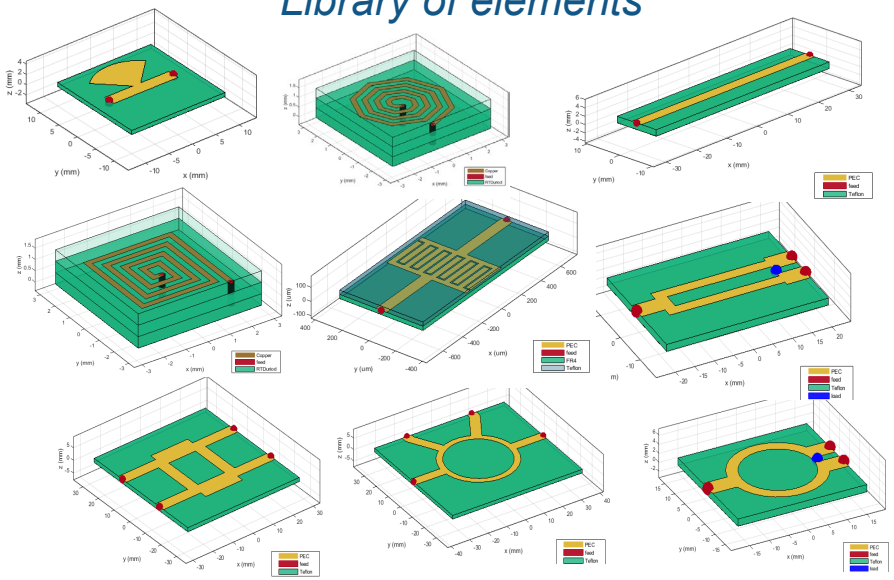


R2022a新功能：射频PCB板分析

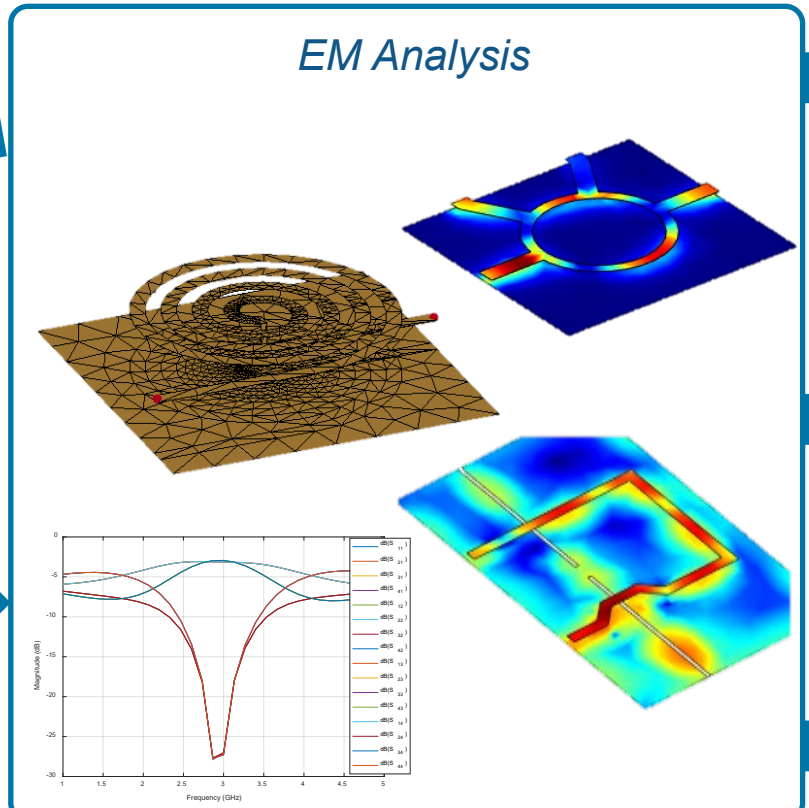
PCB database import



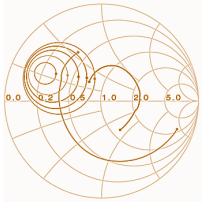
Library of elements



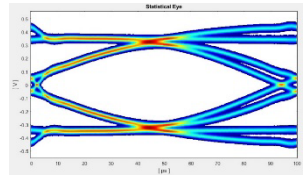
EM Analysis



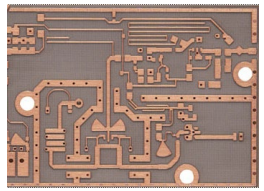
S-parameters



Channel Models



Prototyping (Gerber)

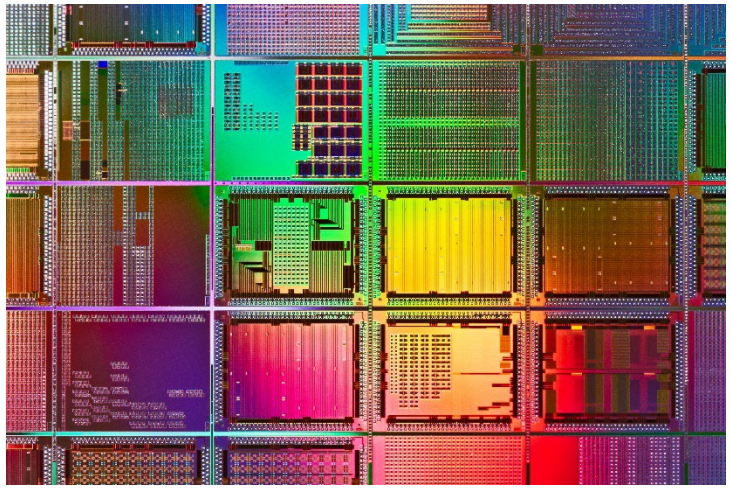


Agenda

- 基于 Simscape 的电路仿真
- 射频电路仿真
- 高速电路信号完整性仿真

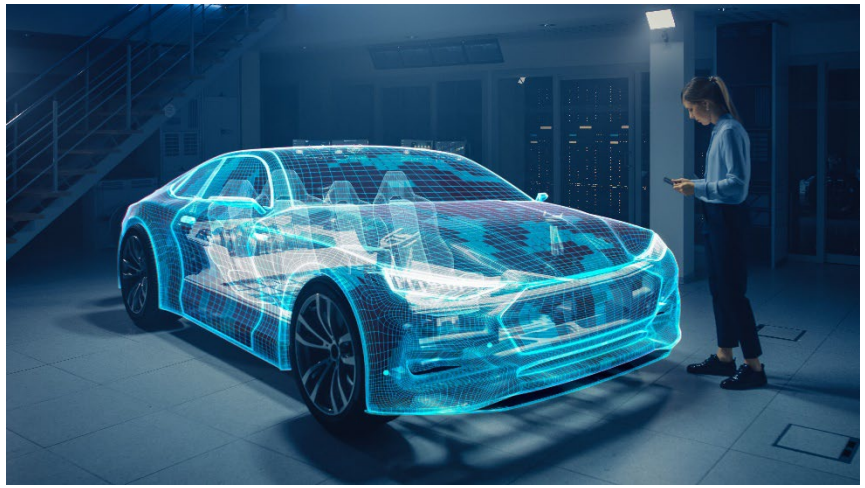
高速设计中信号完整性

Semiconductor

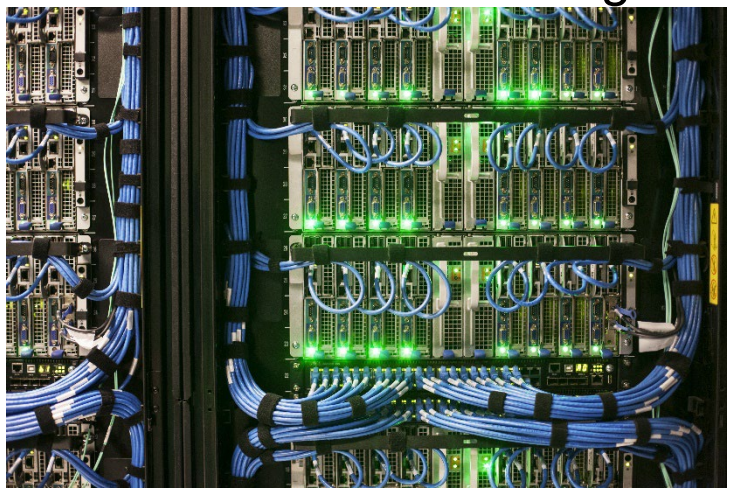


AeroDef

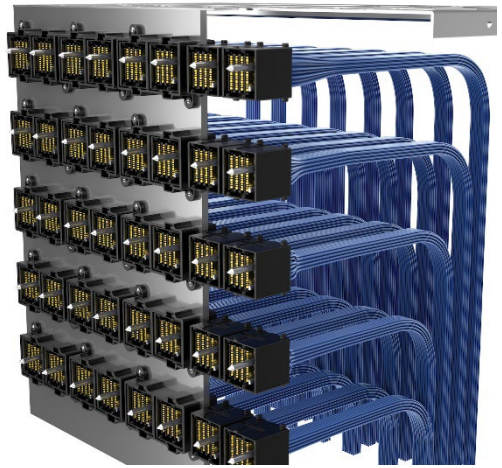
Automotive



Server / Switch / Storage



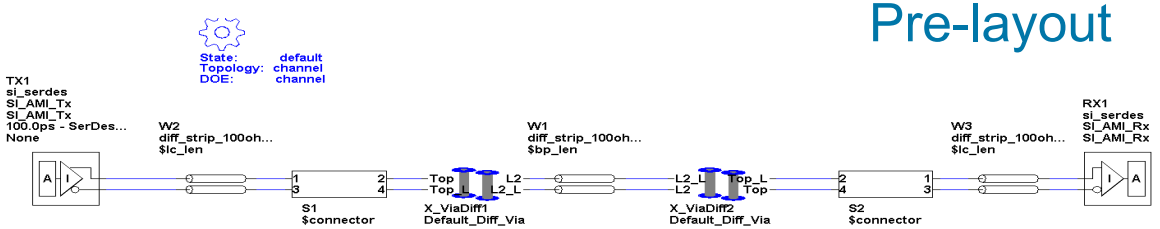
PCB / Connector / Cables

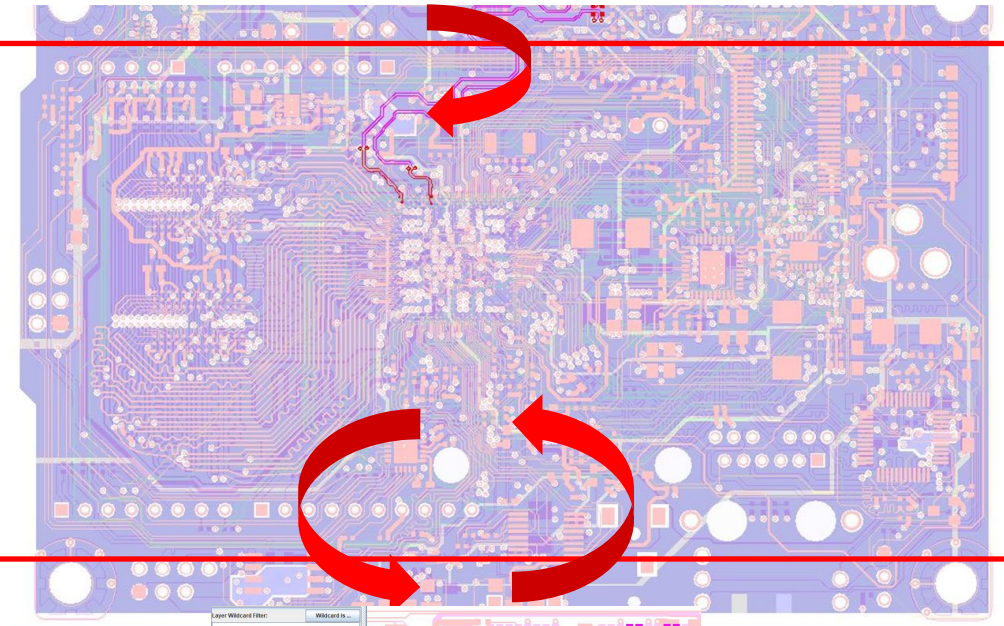


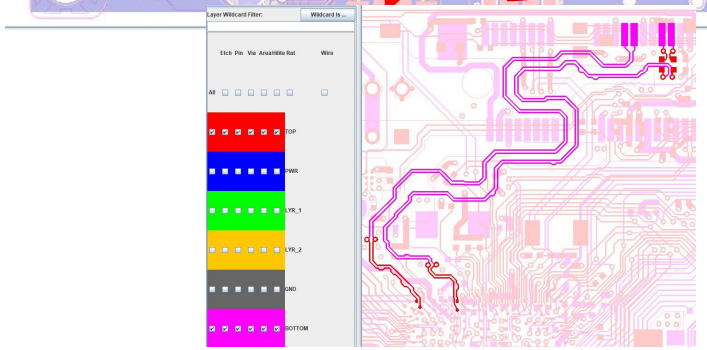
Test & Measurement

MathWorks解决方案

Pre-layout







Post-layout

MATLAB

Signal Integrity Toolbox

RF Toolbox

SerDes Toolbox

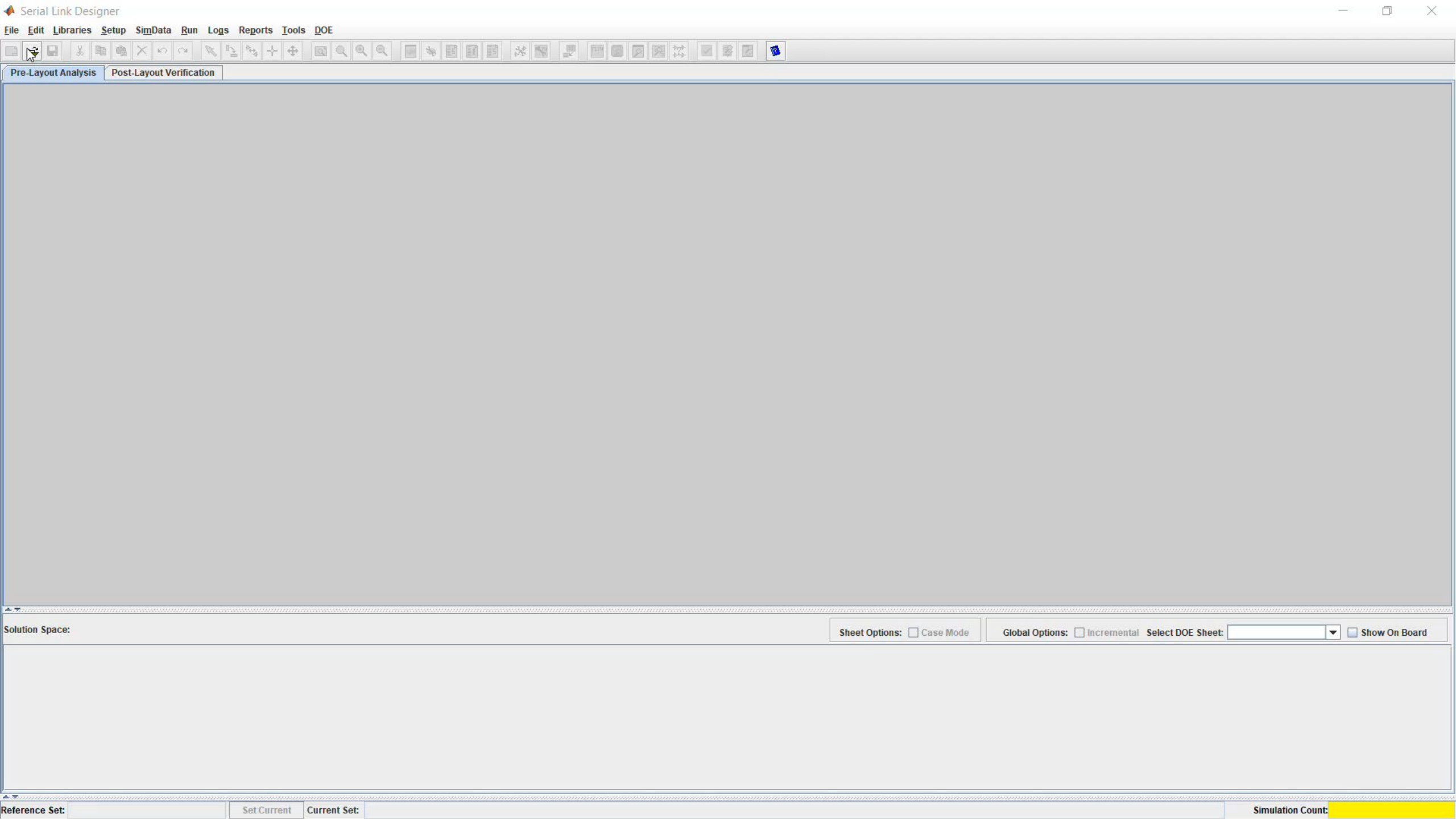
Simulink, DSP System, and Signal Processing Toolboxes (Required)

RF PCB Toolbox

RF Toolbox

Signal Integrity Toolbox

Parallel Computing Toolbox

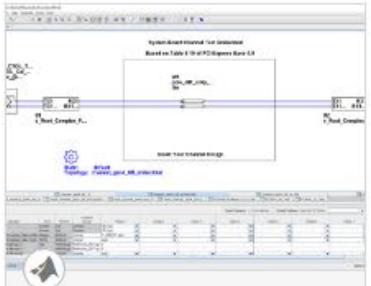

Serial Link Designer
File Edit Libraries Setup SimData Run Logs Reports Tools DOE
Pre-Layout Analysis
Post-Layout Verification
Solution Space:
Sheet Options: Case Mode
Global Options: Incremental
Select DOE Sheet:
Show On Board
Reference Set:
Set Current
Current Set:
Simulation Count:

Signal Integrity Toolbox Features – Standards Compliance

Industry Standard Signal Integrity Kits — Examples

PCIe-5 Compliance Kit

Test the compliance of simulation models and topologies to the PCI Express generation 5 (PCIe-5) specification.

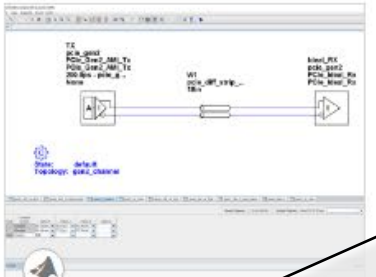


PCIe-4 Compliance Kit

Test the compliance of simulation models and topologies to the PCI Express generation 4 (PCIe-4) specification.

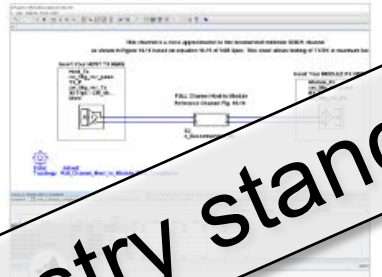
PCIe-3 Compliance Kit

Test the compliance of simulation models and topologies to the PCI Express generation 3 (PCIe-3) specification.



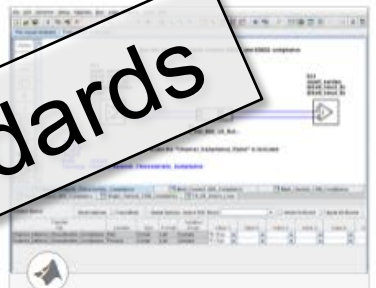
PCIe-2 Compliance Kit

Test the compliance of simulation models and topologies to the PCI Express generation 2 (PCIe-2) specification.



CEI 56G-VSR Compliance Kit

Characterize and validate the performance of a CEI 56G-VSR channel design.

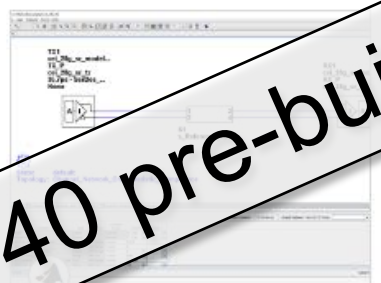


CEI 56G-LR Compliance Kit

Characterize and validate the performance of a CEI 56G-LR channel design.

CEI 28G-VSR Compliance Kit

Characterize and validate the performance of a CEI 28G-VSR channel design.

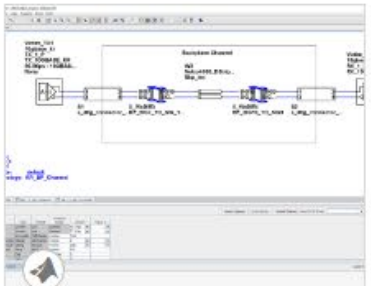


CEI 28G-SR Compliance Kit

Characterize and validate the performance of a CEI 28G-SR channel design.

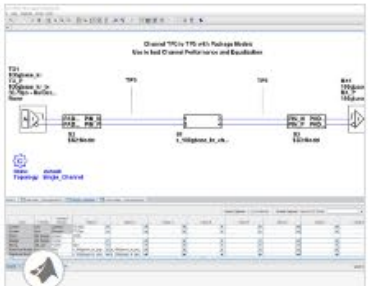
CEI 25G-LR Compliance Kit

Characterize and validate the performance of a CEI 25G-LR channel design.



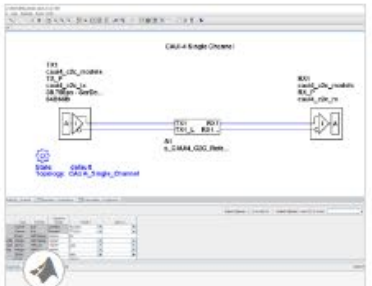
10GBASE-KR4 Compliance Kit

Characterize and validate the performance of a 10GBASE-KR4 channel design.



100GBASE-KR4 Compliance Kit

Characterize and validate the performance of a 100GBASE-KR4 channel design.



CAUI-4 Chip-to-Chip Compliance Kit

Test the compliance of simulation models and topologies to the CAUI-4 C2C specification.

Over 40 pre-built design kits for industry standards

Design Space Exploration

For both Serial and Parallel Designer apps

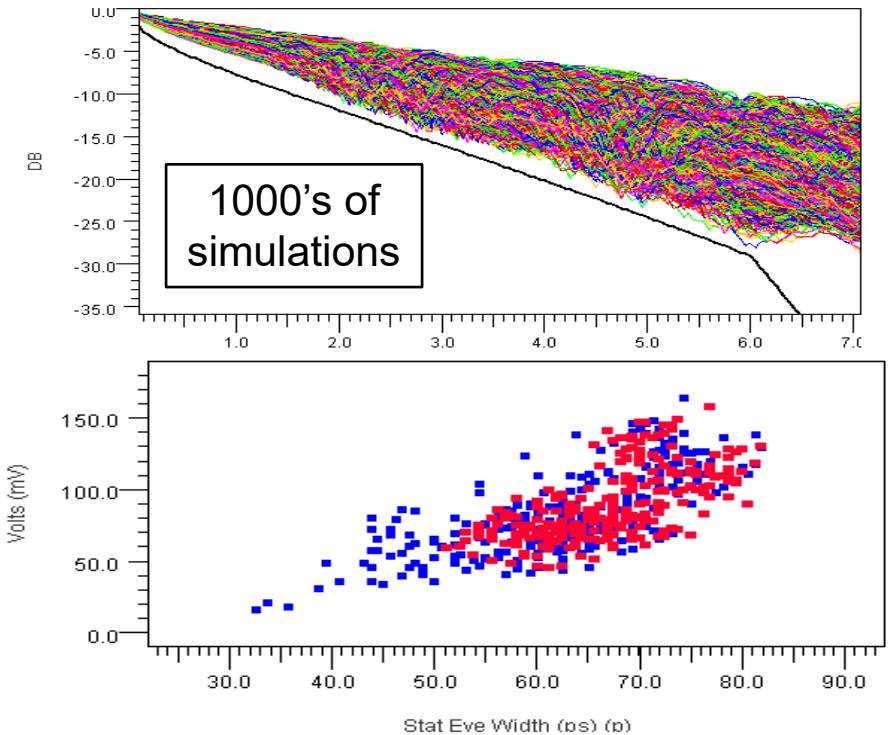
Solution Space:

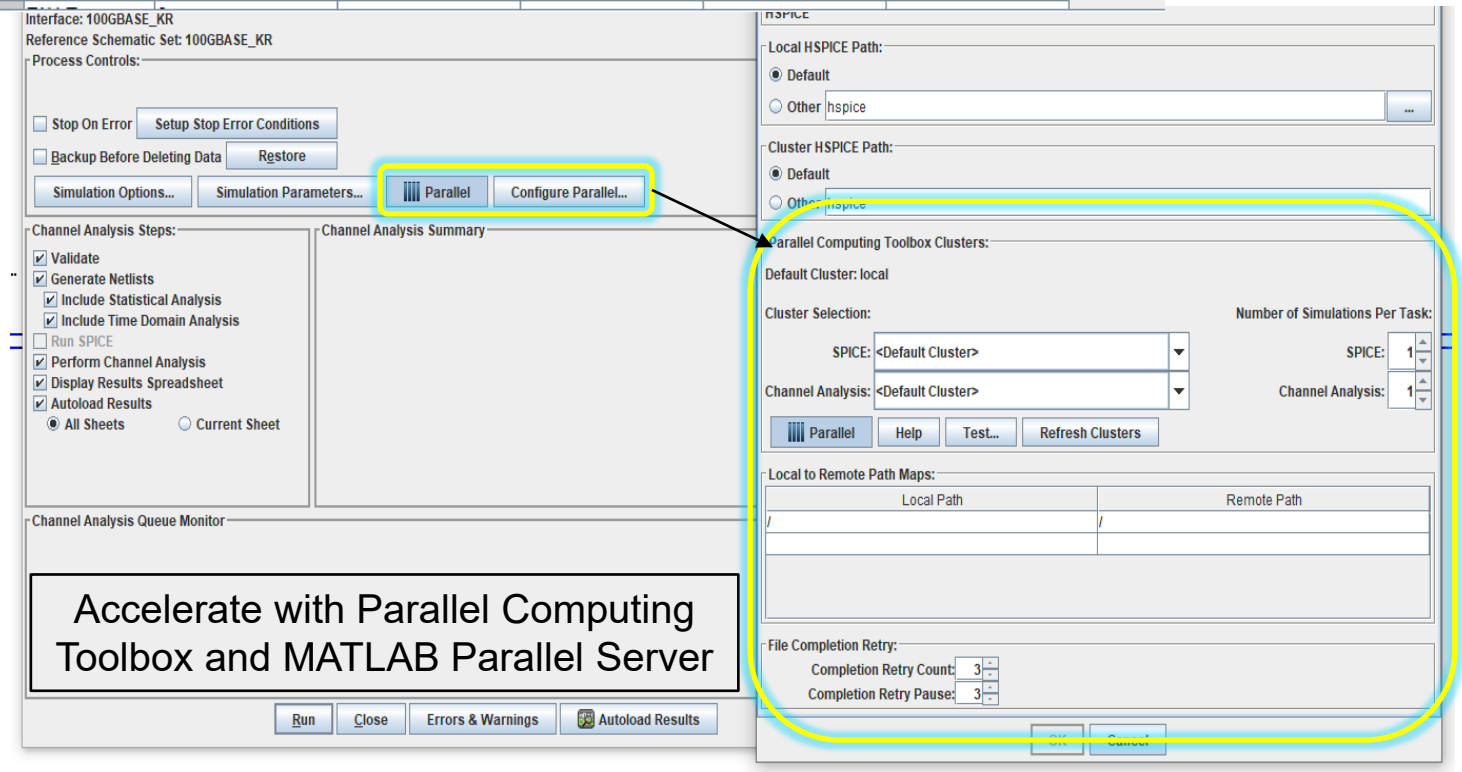
Sheet Options: Case Mode

Global Options: Select DOE Sh

Transfer Net	Variable:	Type:	Format:	Variation Group:	Value 1:	Value 2:	Value 3:	Value 4:	Value 5:
channel	Etch	Corner	List	Corners	TE (Typ)				
channel	Process	Corner	List	Corners	TT (Typ)				
channel	$bp_len	W Length	Soft Range	<none>	16in				
channel	$connector	Subcircuit Model	List	<none>	s_connector_ab	s_connector_cd	s_connector_ef	s_connector_gh	
channel	$lc_len	W Length	Soft Range	<none>	3in	2in	4in	5in	
channel	RX1:Rx_Receiver_Sensitivity	Float	AMI Range	<none>	0.025				
channel	RX1:peaking_filter.config	Integer	AMI Range	<none>	0				
channel	RX1:peaking_filter.mode	String	AMI List	<none>	off				
channel	RX1:clock_recovery.ref	Float	AMI Range	<none>	0.0				
channel	RX1:dfe.taps.1	Tap	AMI Range	RX1:Tap	0				

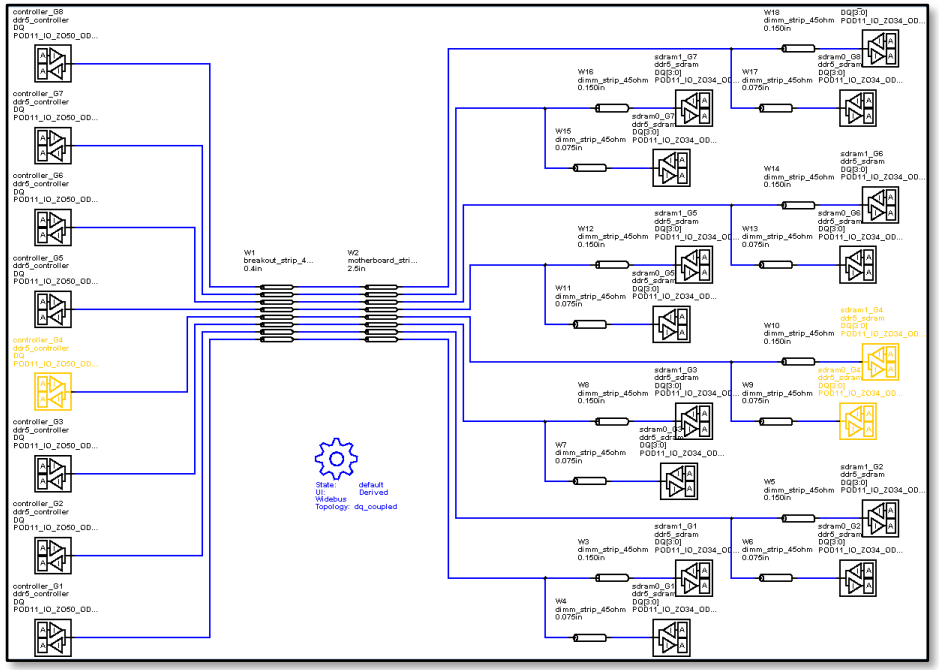
4 connectors
x
4 line-card lengths
=
16 simulations



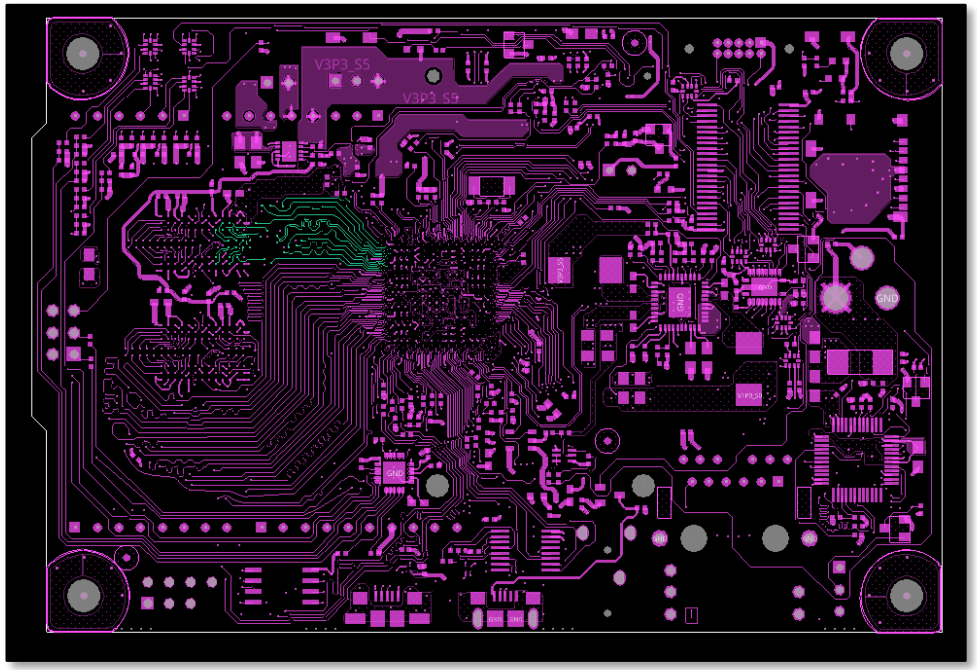


Signal Integrity Toolbox + RF PCB Toolbox

Pre-layout



Post-layout



- Use RF PCB Toolbox to import PCB files
- Compare pre- and post-layout nets to each other
- Easily identify any issues
- Incorporate fixes and re-simulate

- Cadence Allegro
- Mentor PADS Layout
- Mentor Board Station
- Mentor Expedition PCB
- Cadence APB
- Intercept Pantheon
- Altium Designer
- Altium P-CAD
- IBIS EBD

MATLAB EXPO

Thank you