ZTE中兴

5G全光承载网高速数据链路--从设计到实现

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MATLAB EXPO

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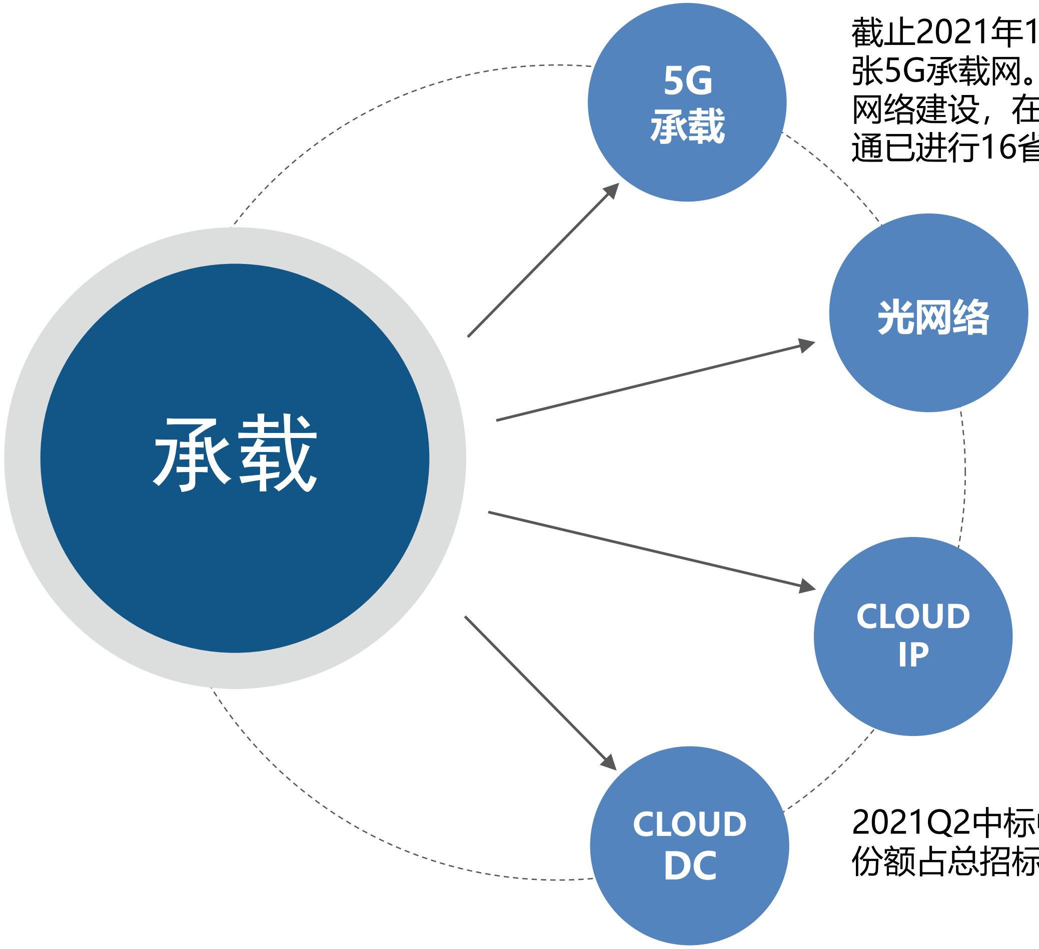
1 中兴通讯承载网介绍
2 SerDes架构设计和系统开发
3 SerDes仿真验证
4 IBIS-AMI模型建立
5 系统链路SI仿真
6 总结

中兴通讯承载网介绍



截止2021年11月累计发货近14万端，建设超400张5G承载网。2021年全年，在中移已进行30省5G网络建设，在电信已进行22省5G网络建设，在联通已进行16省5G网络建设

截止2021年11月，全球100G/超100G OTN光网络数量超过600个

核心路由器ZXR10 T8000在中国（26个省），国际（埃塞俄比亚、印度尼西亚、巴基斯坦等七个国家）运营商骨干网广泛应用

2021Q2中标中国移动网络云三期SDN标段第一名，份额占总招标规模的50%

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5 系统链路SI仿真

6 总结

Serializer/Deserializer（SerDes）系统越来越复杂

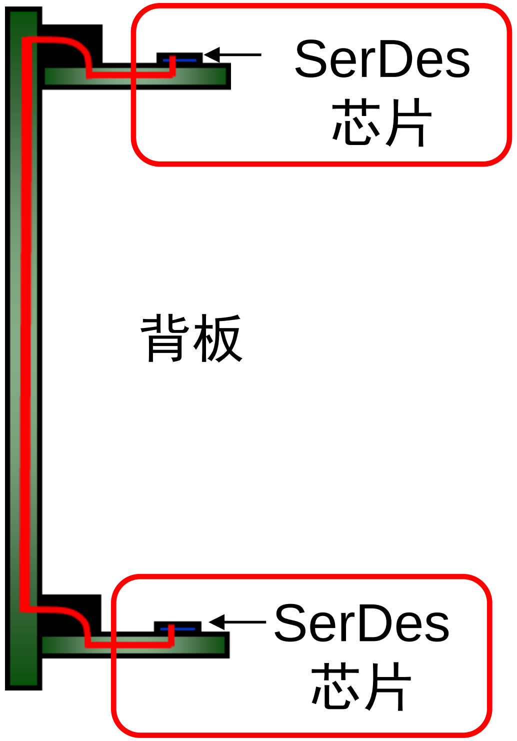
- 高速数据通信系统越来越多
  - 数据中心：板件、设备间高速数据交换
  - 电脑：CPU/GPU/内存/网络间高速数据交换
  - 消费电子：手机基带/内存
  - 汽车电子：车联网
- 主流高速通信协议数据速率越来越高
  - PCI-E
  - Ethernet
  - SAS
  - HDMI
  - MIPI
- SerDes：数字和模拟模块的复杂组合
  - PLL/CDR
  - CTLE
  - DFE/FFE

- 数据中心（服务器）

- 数据中心（存储器）

- 无线通信（RRU, BBU）

- 网络通信（交换机、路由器）

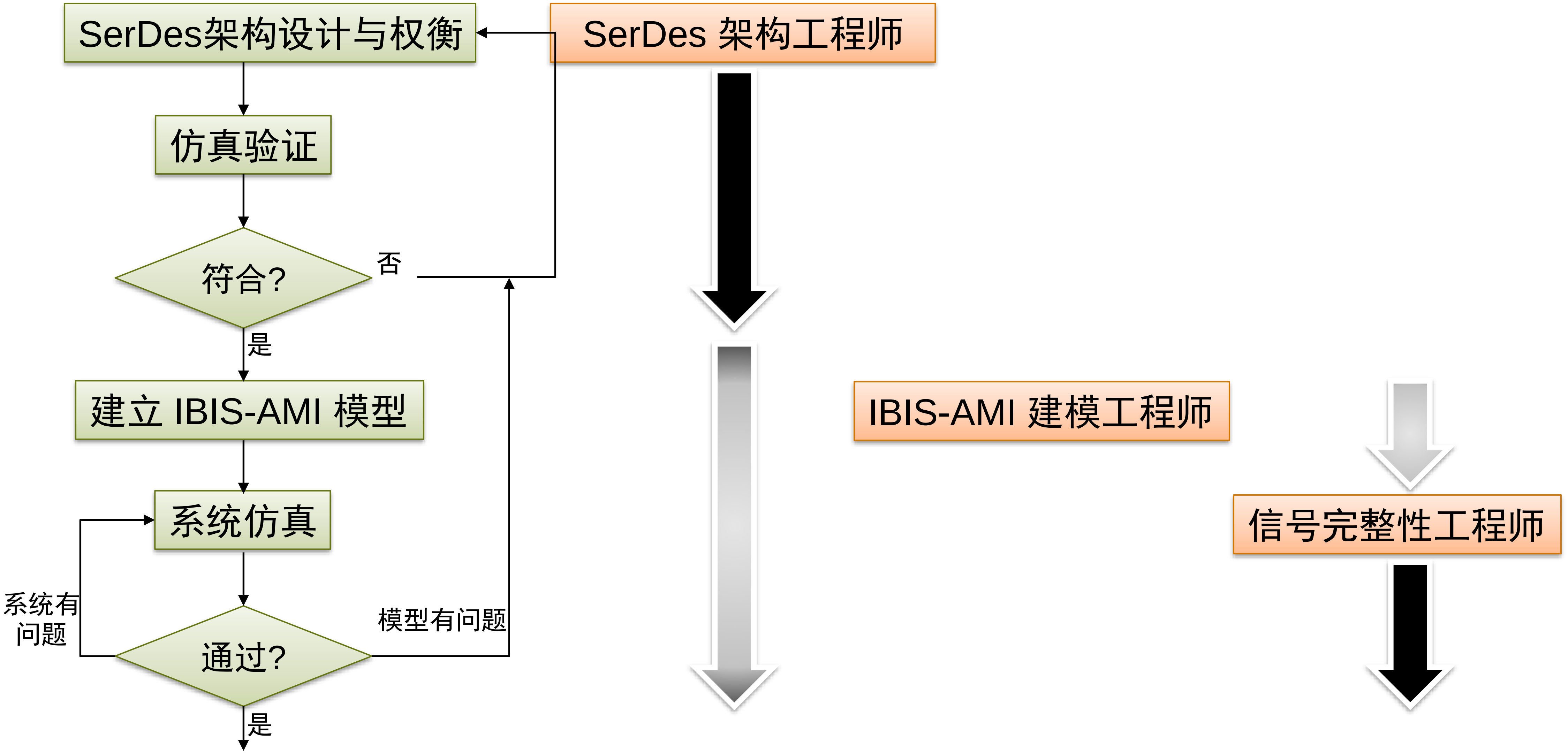


SerDes
芯片

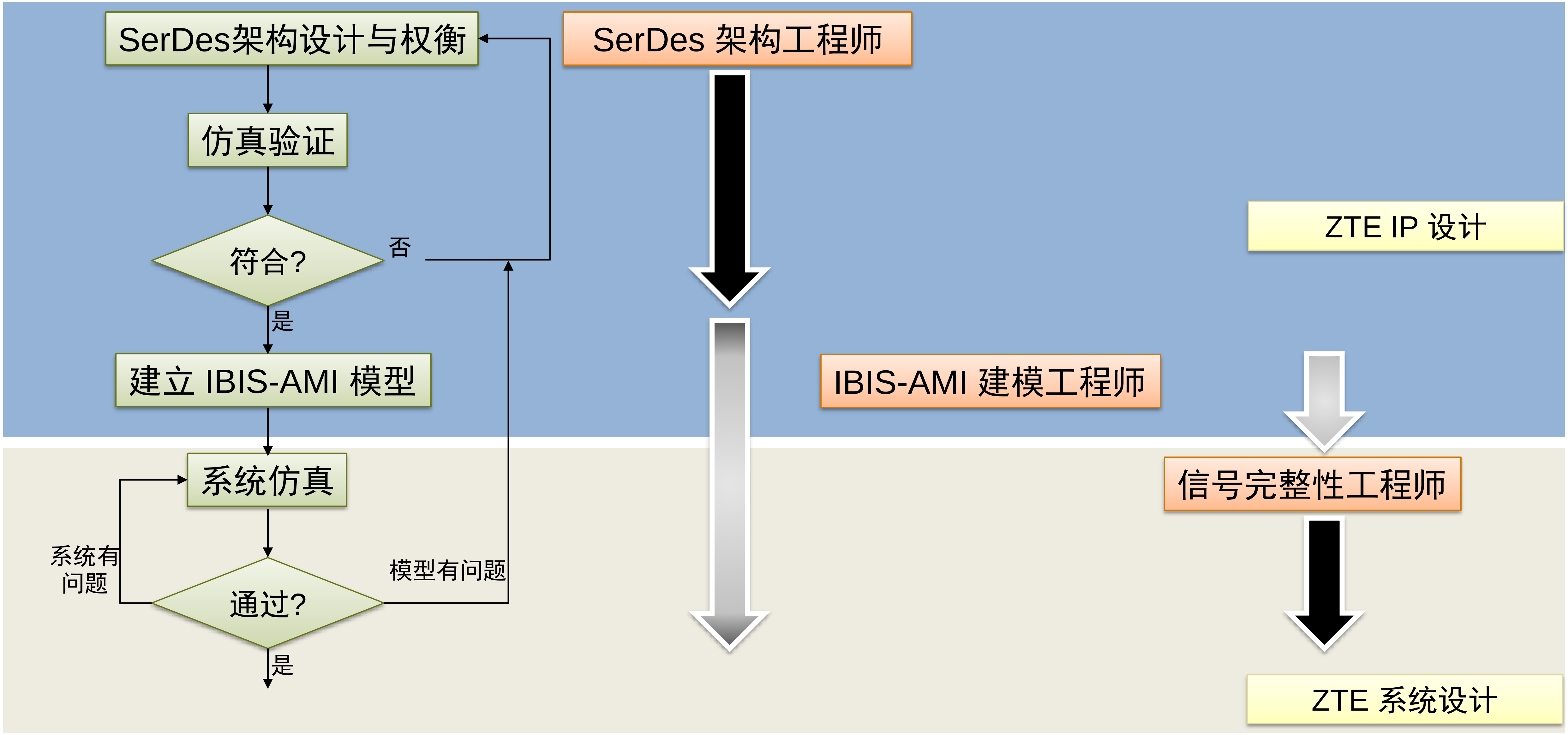
背板

SerDes
芯片

SerDes系统开发流程


SerDes架构设计与权衡
仿真验证
符合?
否
是
建立 IBIS-AMI 模型
系统仿真
系统有问题
通过?
模型有问题
是
SerDes 架构工程师
IBIS-AMI 建模工程师
信号完整性工程师

SerDes系统开发流程



SerDes架构设计与权衡

仿真验证

符合?

否

是

建立 IBIS-AMI 模型

系统仿真

通过?

系统有问题

模型有问题

是

SerDes 架构工程师

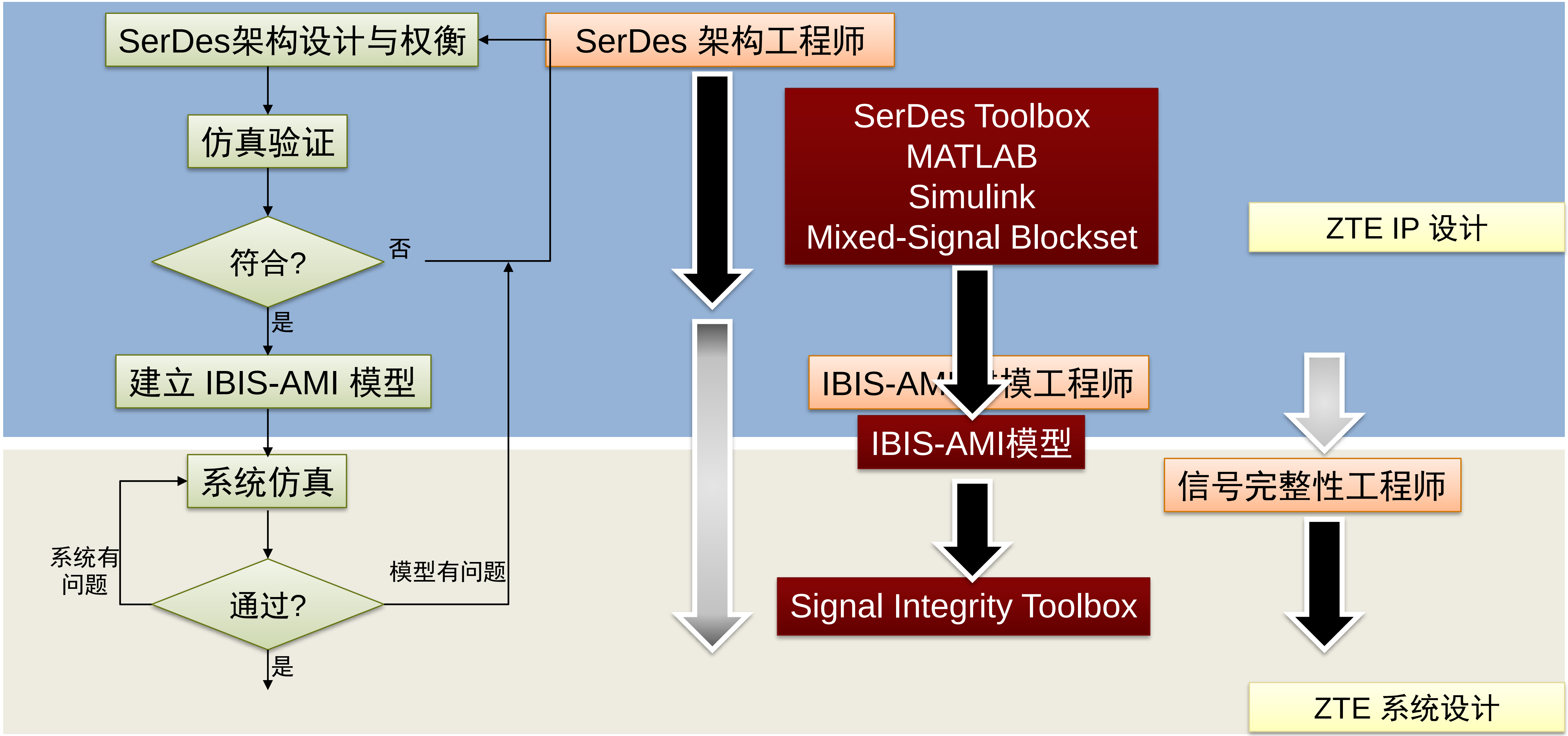
IBIS-AMI 建模工程师

ZTE IP 设计

信号完整性工程师

ZTE 系统设计

SerDes系统开发流程



SerDes架构设计与权衡

仿真验证

符合?

否

是

建立 IBIS-AMI 模型

系统仿真

系统有问题

通过?

模型有问题

是

SerDes 架构工程师

SerDes Toolbox
MATLAB
Simulink
Mixed-Signal Blockset

IBIS-AMI 建模工程师

IBIS-AMI模型

Signal Integrity Toolbox

ZTE IP 设计

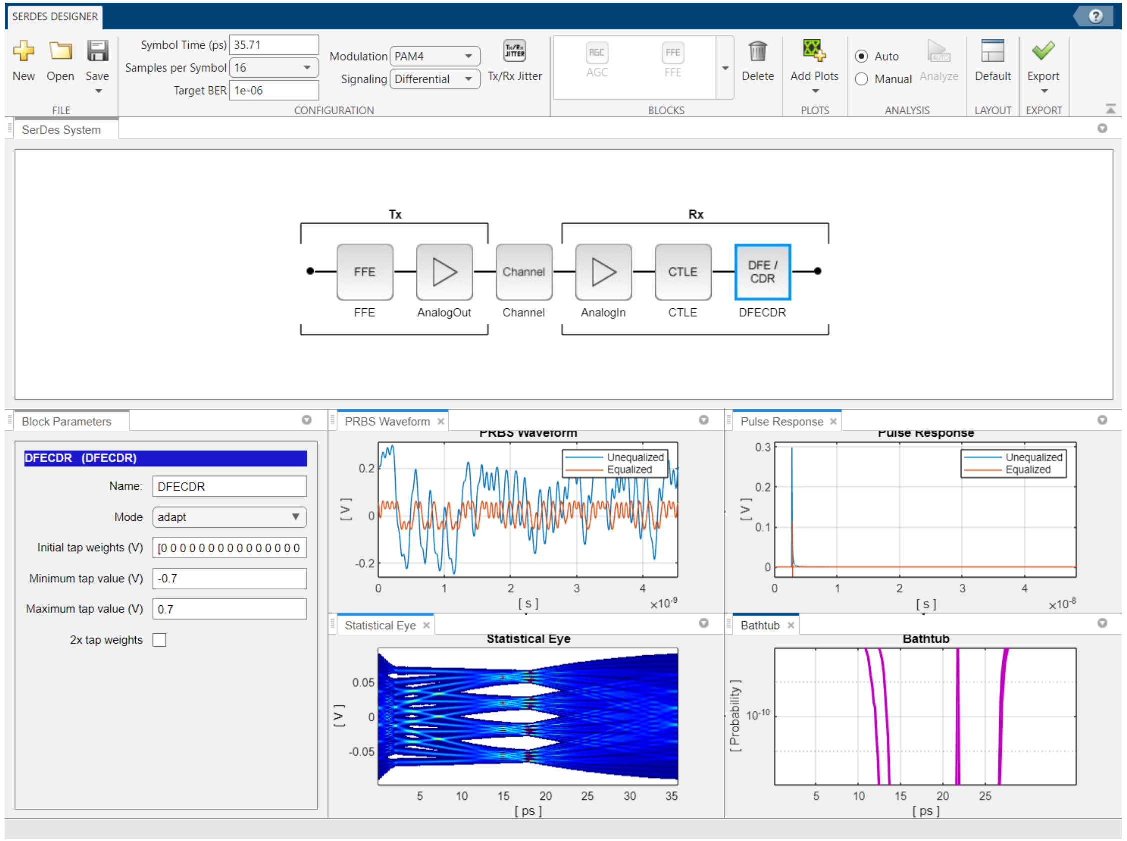
信号完整性工程师

ZTE 系统设计

SerDes构架设计 – 56G LR SerDes设计

- CEI-56G-LR 技术指标：
  - 调制方式（Modulation）： PAM4
  - 符号时间（Symbol Time）： 35.71ps
  - 误码率目标（Target BER）： 1e-6
  - 符号形式（Signaling）： 差分（ Differential ）
  - 均衡：
    - FFE ： 4 taps （2 pre-tap，1 post-tap）
    - DFE：12-18 taps

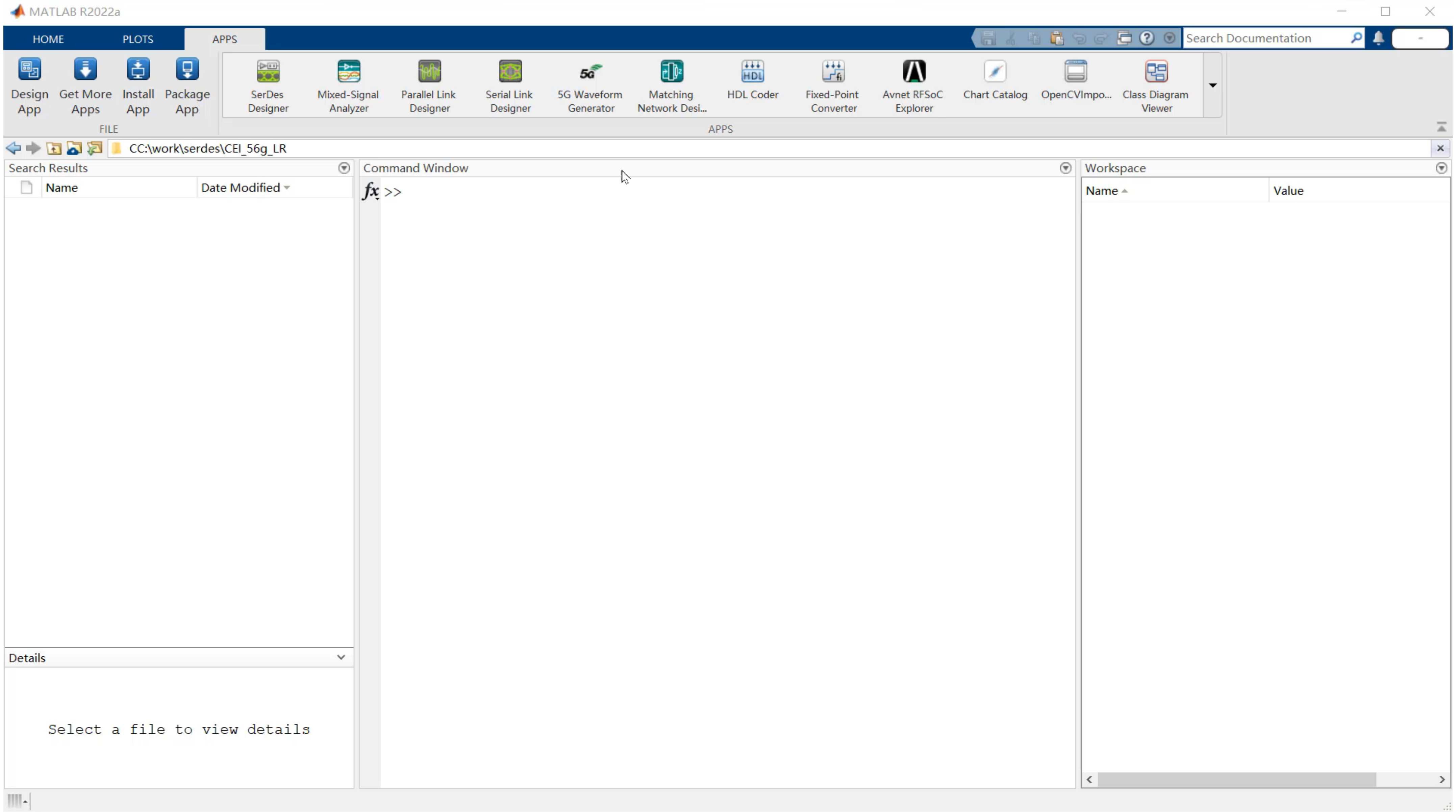
- 快速构架设计 -- SerDes Designer


SERDES DESIGNER
New
Open
Save
FILE
CONFIGURATION
Tx/Rx Jitter
AGC
FFE
BLOCKS
Delete
Add Plots
PLOTS
Analyze
ANALYSIS
Default
LAYOUT
Export
EXPORT
SerDes System
Tx
Rx
FFE
AnalogOut
Channel
AnalogIn
CTLE
DFE / CDR
DFECDR
Block Parameters
PRBS Waveform
Unequalized
Equalized
[V]
[s]
Pulse Response
Statistical Eye
[ps]
Bathtub
[Probability]

Symbol Time (ps) 35.71
Samples per Symbol 16
Target BER 1e-06
Modulation PAM4
Signaling Differential
● Auto
○ Manual

DFECDR (DFECDR)
Name: DFECDR
Mode adapt
Initial tap weights (V) [0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Minimum tap value (V) -0.7
Maximum tap value (V) 0.7
2x tap weights ☐

SerDes架构设计 – SerDes Designer


MATLAB R2022a
HOME
PLOTS
APPS
Search Documentation
Design App
Get More Apps
Install App
Package App
FILE
SerDes Designer
Mixed-Signal Analyzer
Parallel Link Designer
Serial Link Designer
5G Waveform Generator
Matching Network Desi...
HDL Coder
Fixed-Point Converter
Avnet RFSoC Explorer
Chart Catalog
OpenCVImpo...
Class Diagram Viewer
APPS
CC:\work\serdes\CEI_56g_LR
Search Results
Name
Date Modified
Command Window
fx >>
Workspace
Name
Value
Details
Select a file to view details

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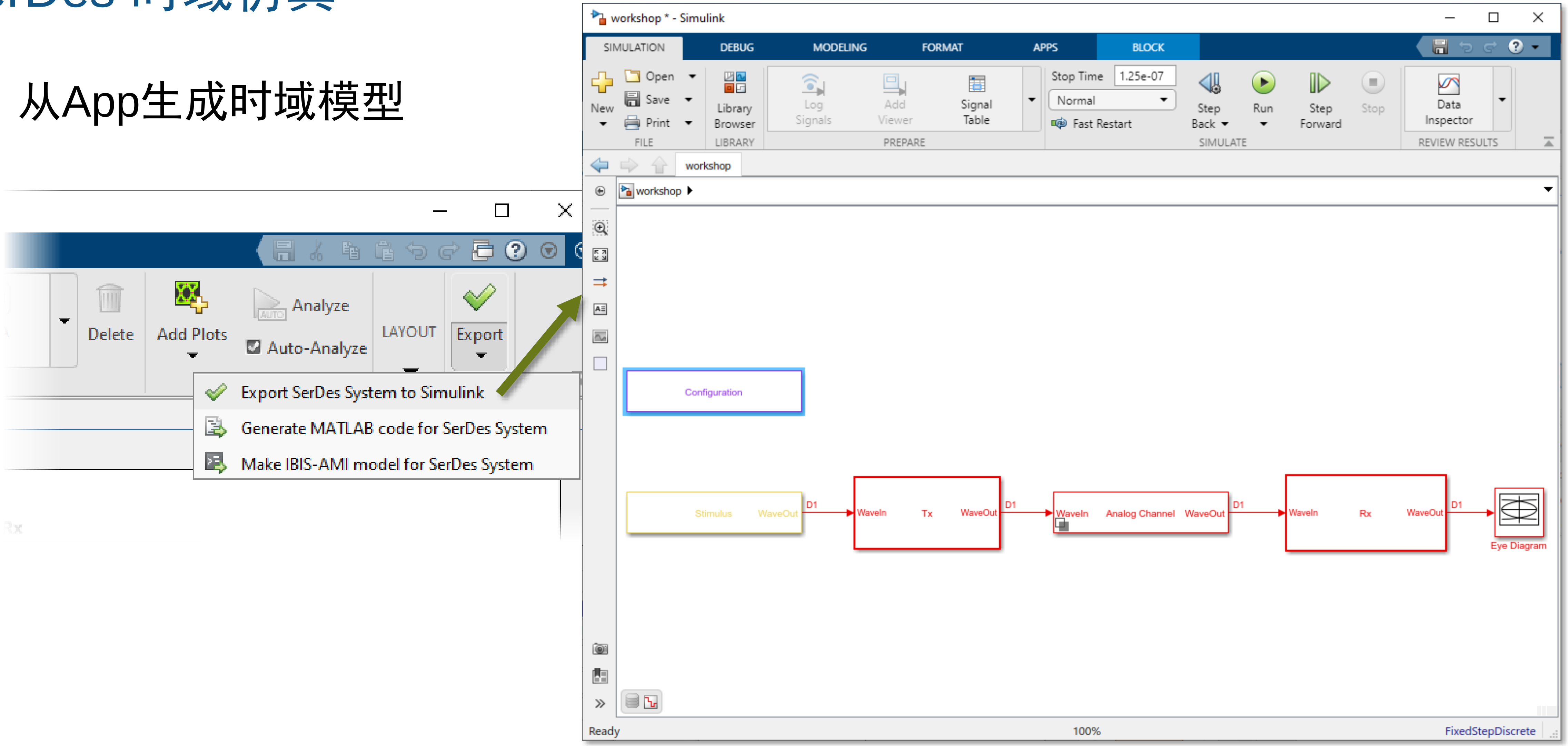
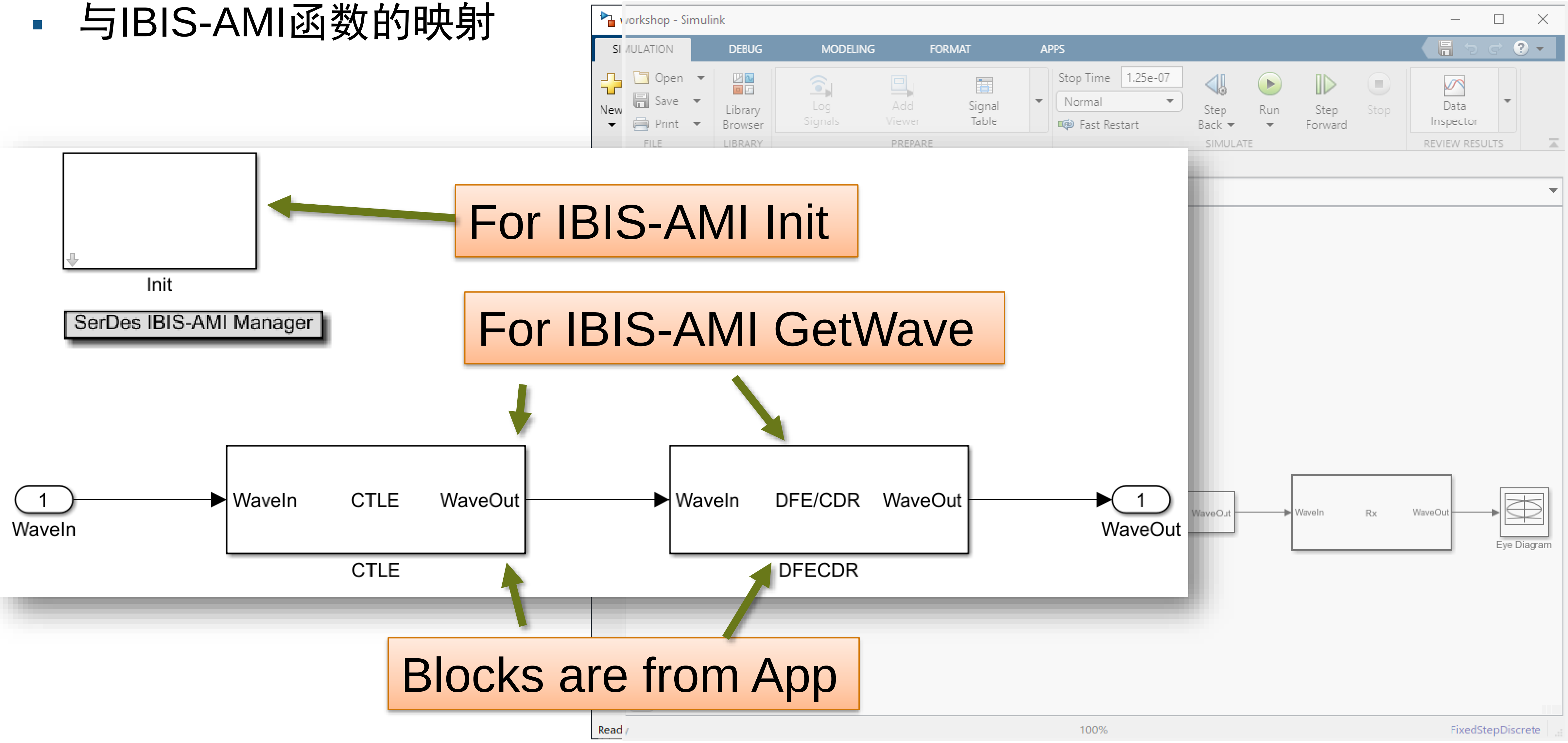
SerDes 时域仿真

- 从App生成时域模型


Delete
Add Plots
Analyze
Auto-Analyze
LAYOUT
Export
Export SerDes System to Simulink
Generate MATLAB code for SerDes System
Make IBIS-AMI model for SerDes System
workshop * - Simulink
SIMULATION
DEBUG
MODELING
FORMAT
APPS
BLOCK
New
Open
Save
Print
FILE
Library Browser
LIBRARY
Log Signals
Add Viewer
Signal Table
PREPARE
Stop Time
1.25e-07
Normal
Fast Restart
Step Back
Run
Step Forward
Stop
SIMULATE
Data Inspector
REVIEW RESULTS
workshop
Configuration
Stimulus
WaveOut
D1
WaveIn
Tx
Analog Channel
Rx
Eye Diagram
Ready
100%
FixedStepDiscrete

SerDes 时域仿真

- 与IBIS-AMI函数的映射



For IBIS-AMI Init

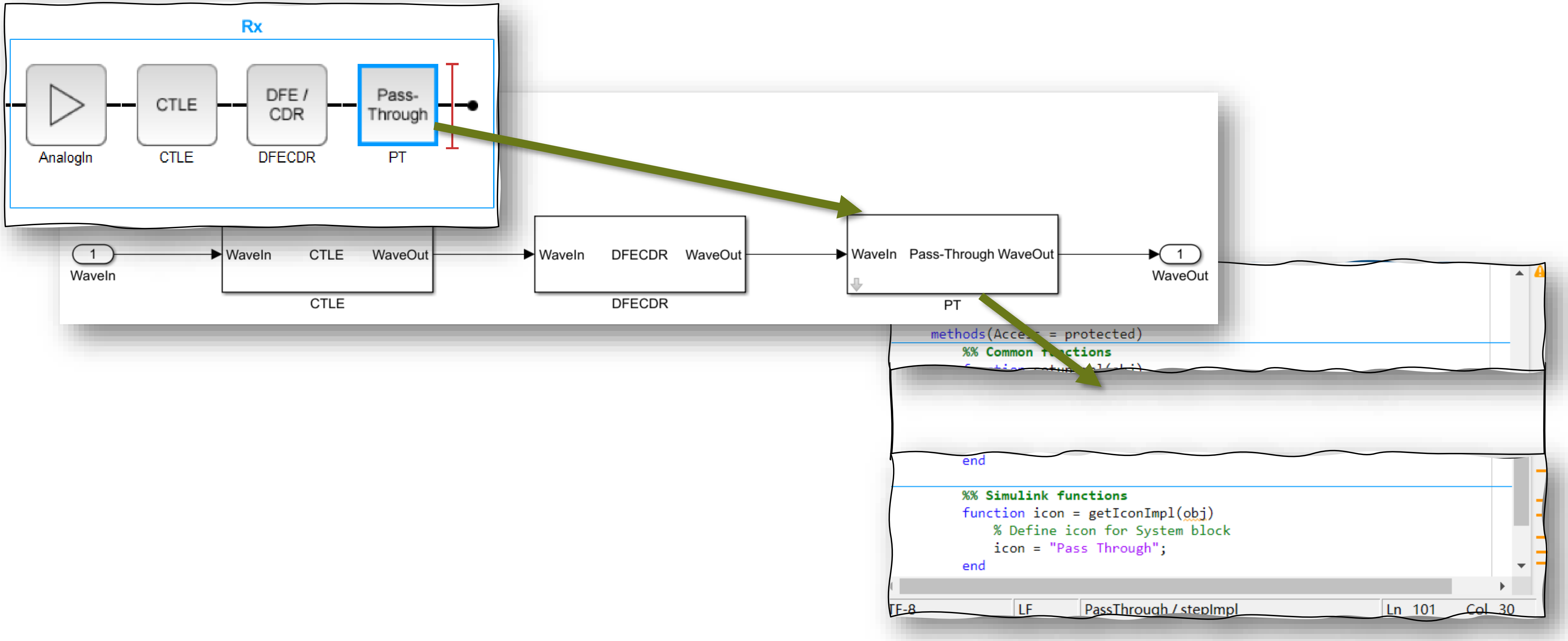
For IBIS-AMI GetWave

Blocks are from App

workshop - Simulink
SIMULATION
DEBUG
MODELING
FORMAT
APPS
New
Open
Save
Print
FILE
Library Browser
LIBRARY
Log Signals
Add Viewer
Signal Table
PREPARE
Stop Time
1.25e-07
Normal
Fast Restart
Step Back
Run
Step Forward
Stop
SIMULATE
Data Inspector
REVIEW RESULTS
Init
SerDes IBIS-AMI Manager
1
WaveIn
WaveIn
CTLE
WaveOut
CTLE
WaveIn
DFE/CDR
WaveOut
DFECDR
1
WaveOut
WaveOut
WaveIn
Rx
WaveOut
Eye Diagram
Read
100%
FixedStepDiscrete

SerDes 时域仿真

- 自有算法开发


Rx
CTLE
DFE / CDR
Pass-Through
AnalogIn
CTLE
DFECDR
PT
1
WaveIn
WaveIn CTLE WaveOut
CTLE
WaveIn DFECDR WaveOut
DFECDR
WaveIn Pass-Through WaveOut
PT
1
WaveOut

```
methods(Acce   = protected)
    %% Common f      ctions
```

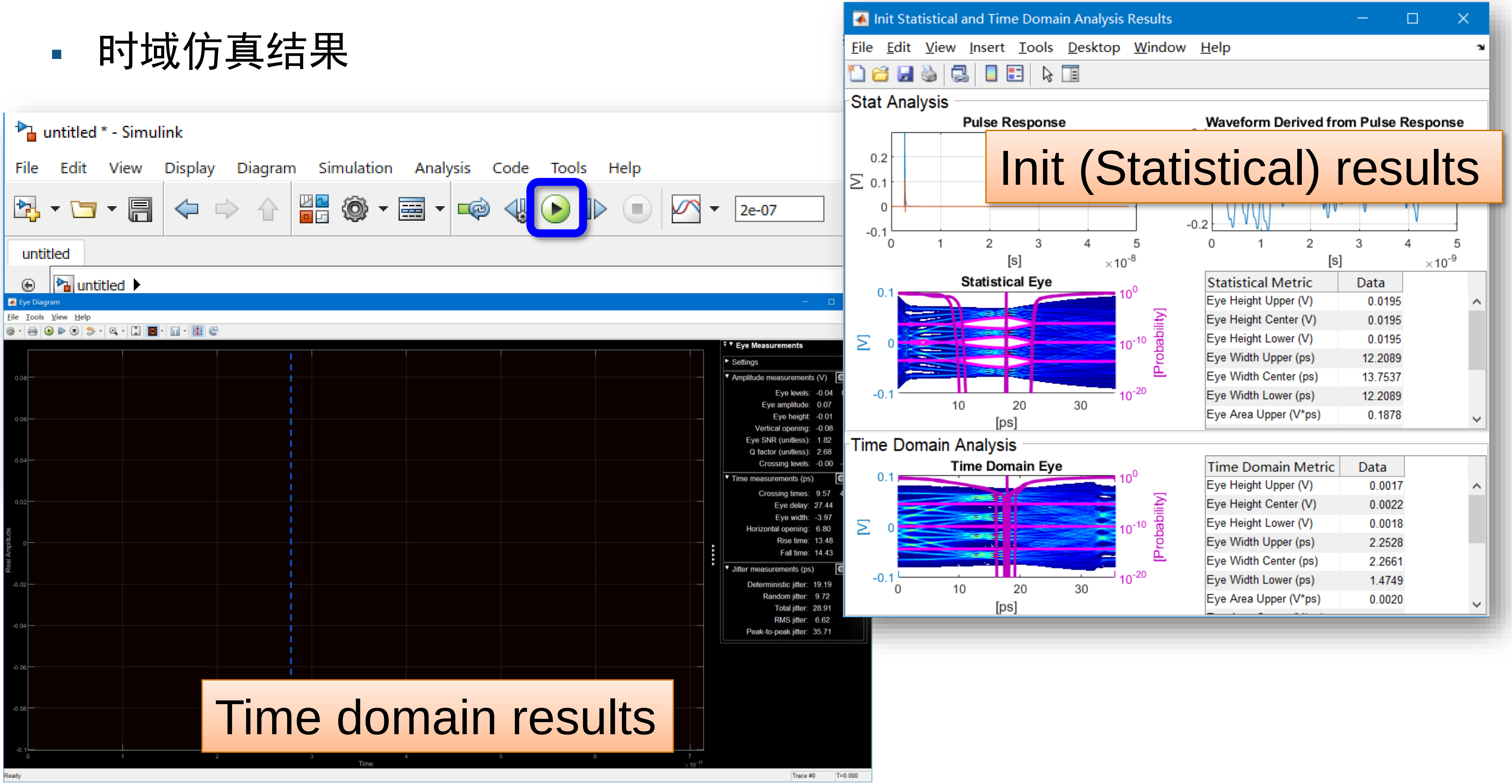
```
    end

    %% Simulink functions
    function icon = getIconImpl(obj)
        % Define icon for System block
        icon = "Pass Through";
    end
```

TF-8 | LF | PassThrough / stepImpl | Ln 101 | Col 30

SerDes 时域仿真

- 时域仿真结果


untitled * - Simulink
File Edit View Display Diagram Simulation Analysis Code Tools Help
2e-07
untitled
Eye Diagram
File Tools View Help
Real Amplitude
Time
Ready
Trace #0
T=0.000
Init Statistical and Time Domain Analysis Results
File Edit View Insert Tools Desktop Window Help
Stat Analysis
Pulse Response
Waveform Derived from Pulse Response
Statistical Eye
[V]
[s]
[ps]
[Probability]
Time Domain Analysis
Time Domain Eye

Eye Measurements

Settings

Amplitude measurements (V)

Eye levels: -0.04
Eye amplitude: 0.07
Eye height: -0.01
Vertical opening: -0.08
Eye SNR (unitless): 1.82
Q factor (unitless): 2.68
Crossing levels: -0.00

Time measurements (ps)

Crossing times: 9.57
Eye delay: 27.44
Eye width: -3.97
Horizontal opening: 6.80
Rise time: 13.48
Fall time: 14.43

Jitter measurements (ps)

Deterministic jitter: 19.19
Random jitter: 9.72
Total jitter: 28.91
RMS jitter: 6.62
Peak-to-peak jitter: 35.71

Statistical Metric	Data
Eye Height Upper (V)	0.0195
Eye Height Center (V)	0.0195
Eye Height Lower (V)	0.0195
Eye Width Upper (ps)	12.2089
Eye Width Center (ps)	13.7537
Eye Width Lower (ps)	12.2089
Eye Area Upper (V*ps)	0.1878

Time Domain Metric	Data
Eye Height Upper (V)	0.0017
Eye Height Center (V)	0.0022
Eye Height Lower (V)	0.0018
Eye Width Upper (ps)	2.2528
Eye Width Center (ps)	2.2661
Eye Width Lower (ps)	1.4749
Eye Area Upper (V*ps)	0.0020

Init (Statistical) results

Time domain results

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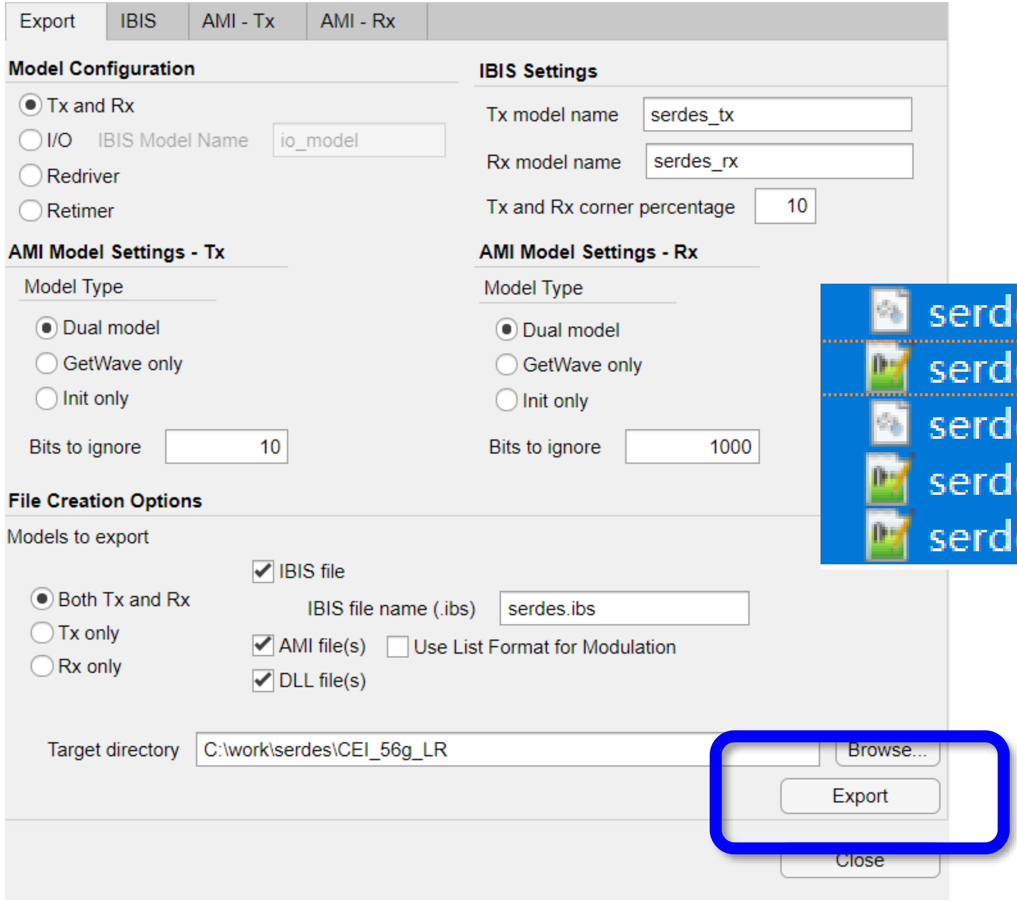
从MATLAB/Simulink自动生成IBIS-AMI 模型



Model Configuration

● Tx and Rx
○ I/O IBIS Model Name io_model
○ Redriver
○ Retimer

IBIS Settings

Tx model name: serdes_tx
Rx model name: serdes_rx
Tx and Rx corner percentage: 10

AMI Model Settings - Tx

Model Type
● Dual model
○ GetWave only
○ Init only
Bits to ignore: 10

AMI Model Settings - Rx

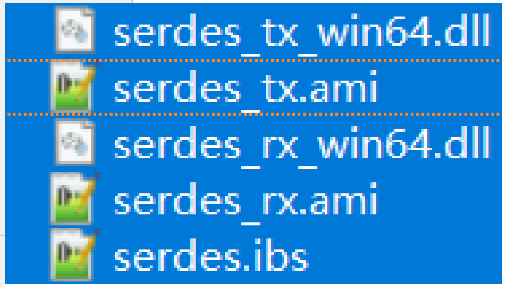
Model Type
● Dual model
○ GetWave only
○ Init only
Bits to ignore: 1000

File Creation Options

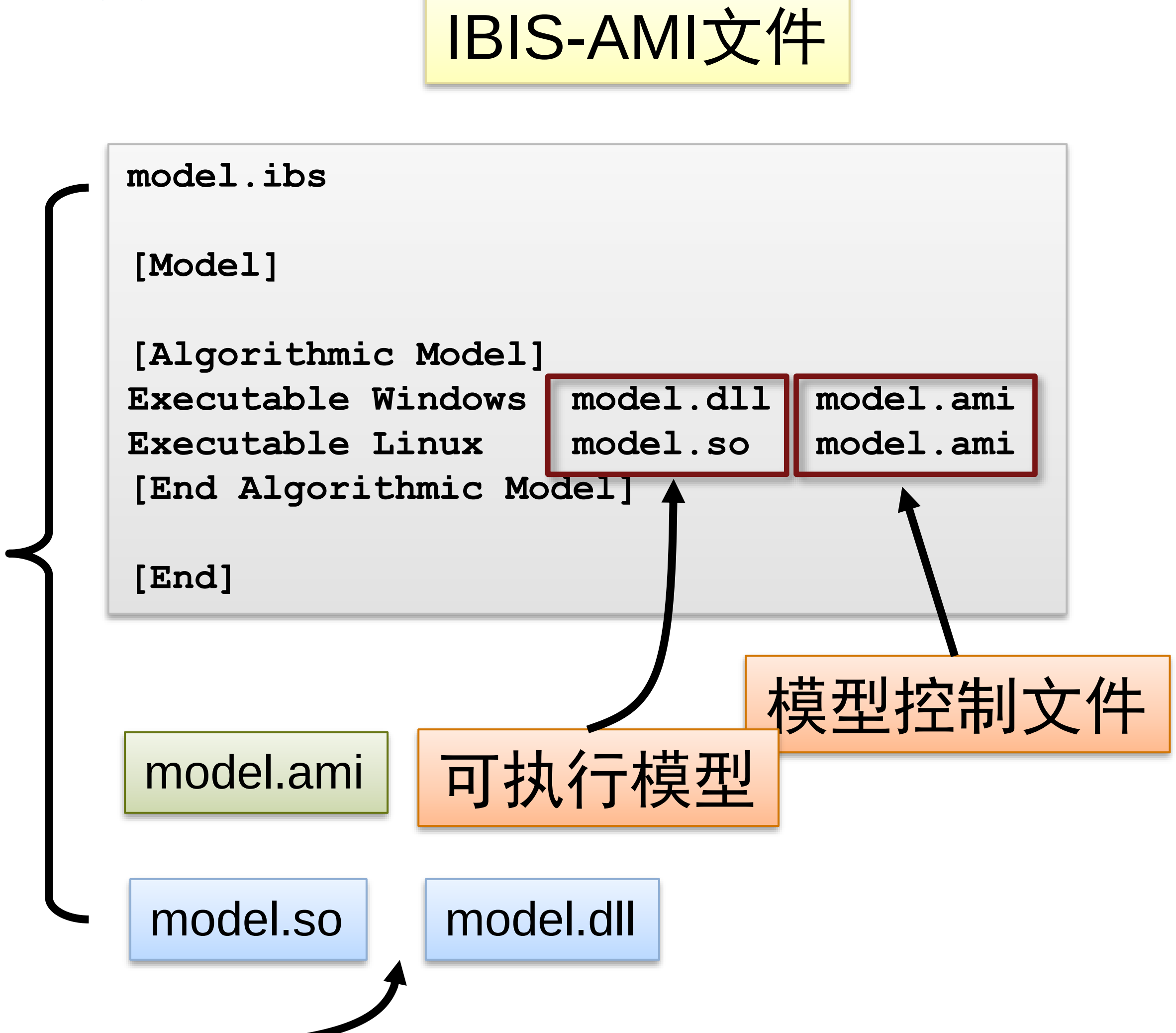
Models to export
● Both Tx and Rx
○ Tx only
○ Rx only

☑ IBIS file
IBIS file name (.ibs): serdes.ibs
☑ AMI file(s) ☐ Use List Format for Modulation
☑ DLL file(s)

Target directory: C:\work\serdes\CEI_56g_LR



serdes_tx_win64.dll
serdes_tx.ami
serdes_rx_win64.dll
serdes_rx.ami
serdes.ibs



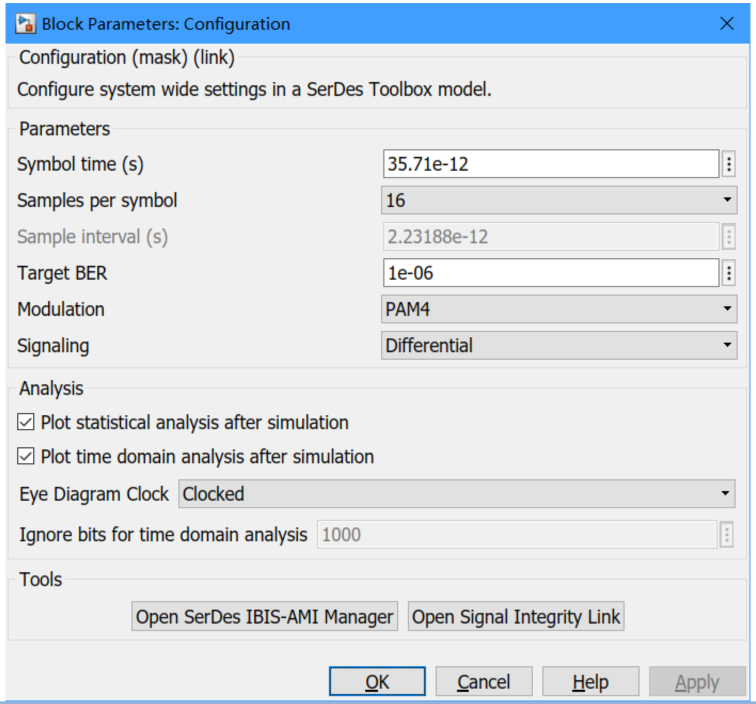
IBIS-AMI文件

```
model.ibs

 [Model]

 [Algorithmic Model]
Executable Windows  model.dll  model.ami
Executable Linux    model.so   model.ami
 [End Algorithmic Model]

 [End]
```

自动编译：
Window系统上生成.dll, Linux系统上生成 .so

从IBIS-AMI模型到系统信号完整性仿真

- 生成IBIS-AMI模型，自动导入到SI Toolbox



Block Parameters: Configuration

Configuration (mask) (link)

Configure system wide settings in a SerDes Toolbox model.

Parameters

Symbol time (s): 35.71e-12
Samples per symbol: 16
Sample interval (s): 2.23188e-12
Target BER: 1e-06
Modulation: PAM4
Signaling: Differential

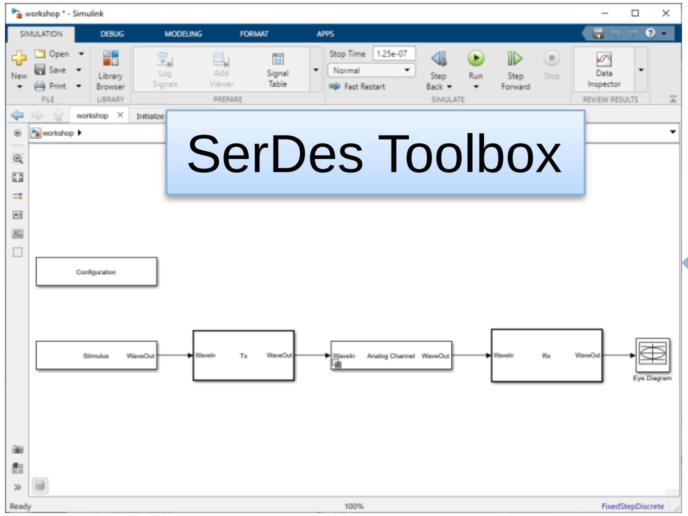
Analysis

☑ Plot statistical analysis after simulation
☑ Plot time domain analysis after simulation

Eye Diagram Clock: Clocked
Ignore bits for time domain analysis: 1000

Tools

Open SerDes IBIS-AMI Manager
Open Signal Integrity Link
OK
Cancel
Help
Apply

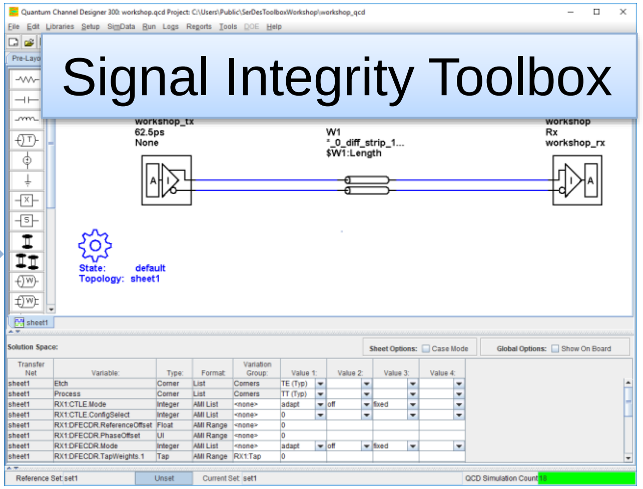


SerDes Toolbox

workshop * - Simulink
Configuration
Stimulus
Tx
Analog Channel
Rx
Eye Diagram

IBIS-AMI model files

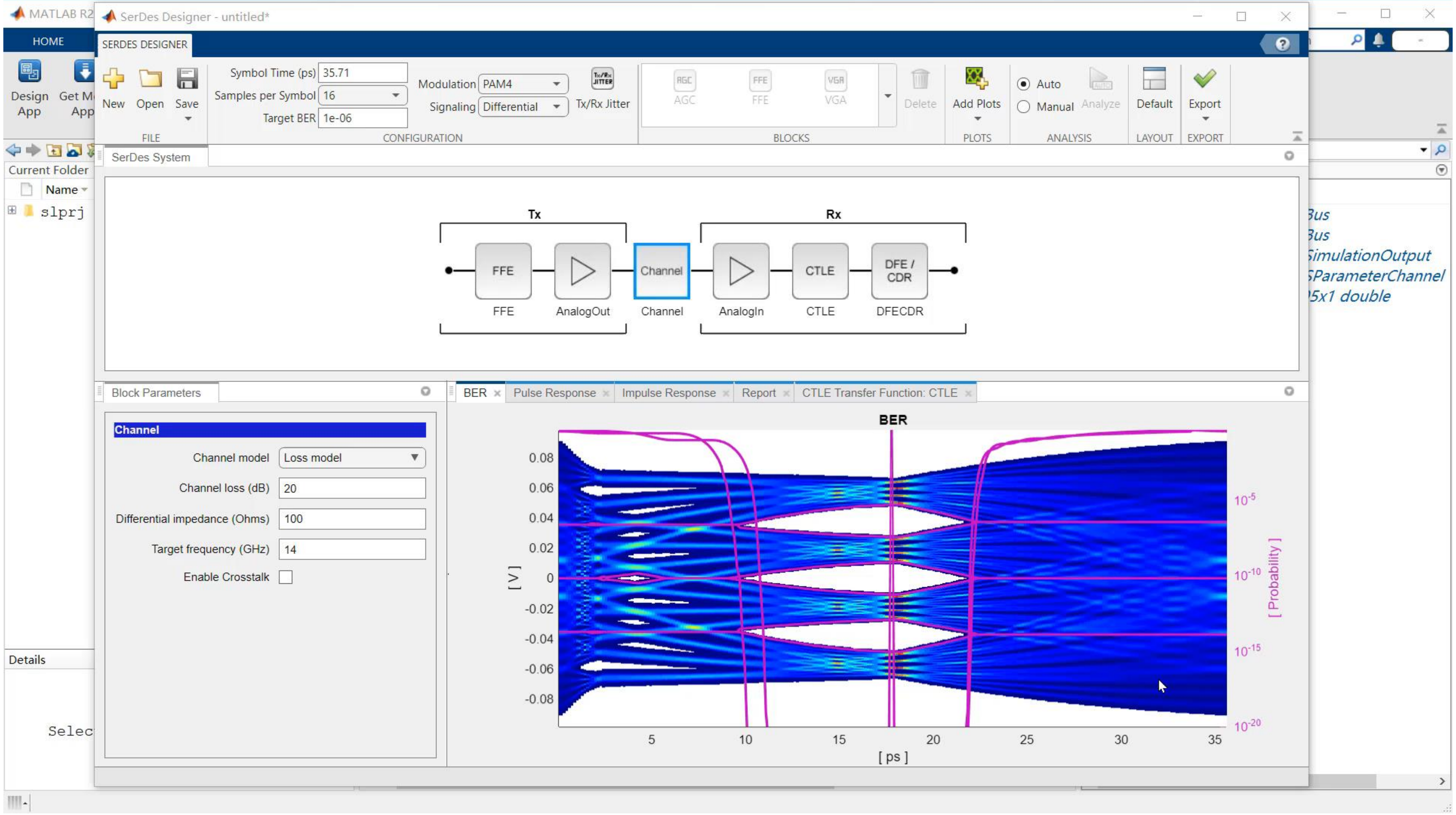
UI, Samples/bit, Target BER



Signal Integrity Toolbox

workshop_tx
workshop_rx
State: default
Topology: sheet1

从SerDes时域仿真到系统信号完整性仿真



SerDes Designer - untitled*

Symbol Time (ps): 35.71
Samples per Symbol: 16
Target BER: 1e-06
Modulation: PAM4
Signaling: Differential
● Auto ○ Manual

Channel
Channel model: Loss model
Channel loss (dB): 20
Differential impedance (Ohms): 100
Target frequency (GHz): 14
Enable Crosstalk: ☐

Bus
Bus
SimulationOutput
SParameterChannel
5x1 double

MATLAB R2
HOME
SERDES DESIGNER
Design App
Get M App
New
Open
Save
FILE
Tx/Rx Jitter
CONFIGURATION
AGC
FFE
VGA
Delete
BLOCKS
Add Plots
PLOTS
Analyze
ANALYSIS
Default
LAYOUT
Export
EXPORT
Current Folder
Name
slprj
Details
Selec
SerDes System
Tx
Rx
FFE
AnalogOut
Channel
AnalogIn
CTLE
DFE / CDR
DFECDR
Block Parameters
BER
Pulse Response
Impulse Response
Report
CTLE Transfer Function: CTLE
BER
0.08
0.06
0.04
0.02
0
-0.02
-0.04
-0.06
-0.08
[V]
5
10
15
20
25
30
35
[ps]
10^{-5}
10^{-10}
10^{-15}
10^{-20}
[Probability]

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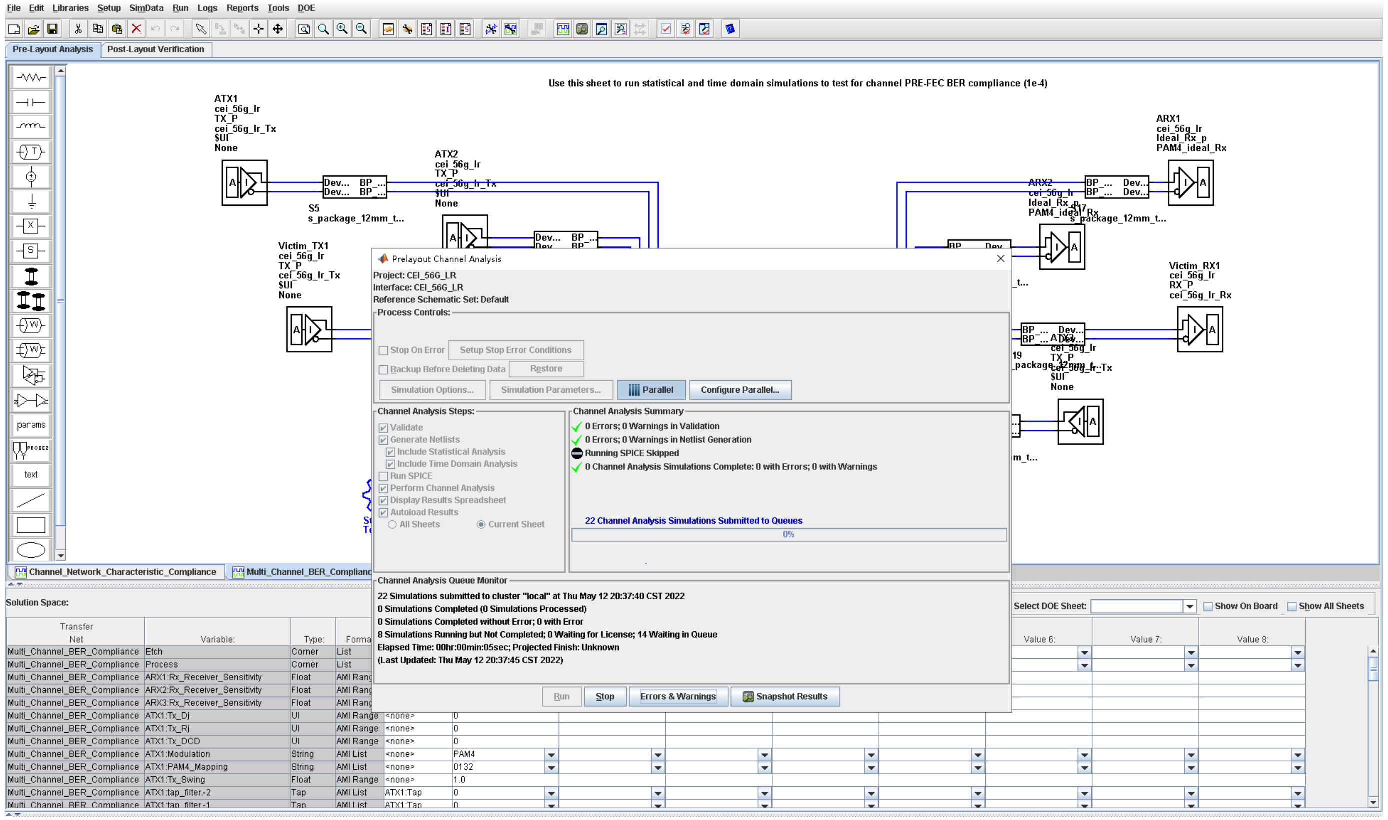
基于Signal Integrity Toolbox的端到端验证

- 功能强大
  - IBIS-AMI
  - 统计和时域仿真
  - 参数化扫描
  - 丰富的合规套件
  - ISI\BER\眼图\抖动\噪声
  - 波形可视化


File Edit Libraries Setup SimData Run Logs Reports Tools DOE
Pre-Layout Analysis
Post-Layout Verification
ATX1
ATX2
ARX1
ARX2
Victim_TX1
Victim_RX1
params
text
Channel_Network_Characteristic_Compliance
Multi_Channel_BER_Complianc

Use this sheet to run statistical and time domain simulations to test for channel PRE-FEC BER compliance (1e-4)

Prelayout Channel Analysis

Project: CEI_56G_LR
Interface: CEI_56G_LR
Reference Schematic Set: Default

Process Controls:

☐ Stop On Error
☐ Backup Before Deleting Data

Channel Analysis Steps:

☑ Validate
☑ Generate Netlists
  ☑ Include Statistical Analysis
  ☑ Include Time Domain Analysis
☐ Run SPICE
☑ Perform Channel Analysis
☑ Display Results Spreadsheet
☑ Autoload Results
○ All Sheets ● Current Sheet

Channel Analysis Summary

✓ 0 Errors; 0 Warnings in Validation
✓ 0 Errors; 0 Warnings in Netlist Generation
⊖ Running SPICE Skipped
✓ 0 Channel Analysis Simulations Complete: 0 with Errors; 0 with Warnings

22 Channel Analysis Simulations Submitted to Queues

0%

Channel Analysis Queue Monitor

22 Simulations submitted to cluster "local" at Thu May 12 20:37:40 CST 2022
0 Simulations Completed (0 Simulations Processed)
0 Simulations Completed without Error; 0 with Error
8 Simulations Running but Not Completed; 0 Waiting for License; 14 Waiting in Queue
Elapsed Time: 00hr:00min:05sec; Projected Finish: Unknown
(Last Updated: Thu May 12 20:37:45 CST 2022)

Setup Stop Error Conditions
Restore
Simulation Options...
Simulation Parameters...
Parallel
Configure Parallel...
Run
Stop
Errors & Warnings
Snapshot Results
Select DOE Sheet:
Show On Board
Show All Sheets

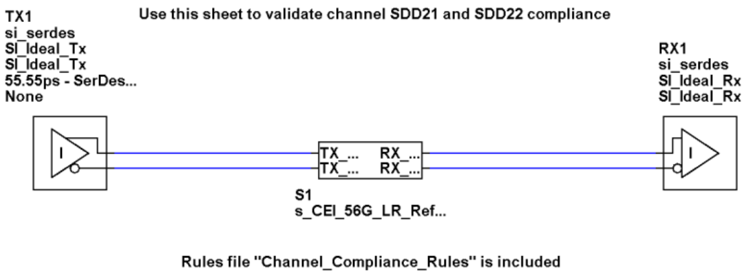
Solution Space:

Transfer Net	Variable:	Type:	Forma		
Multi_Channel_BER_Compliance	Etch	Corner	List		
Multi_Channel_BER_Compliance	Process	Corner	List		
Multi_Channel_BER_Compliance	ARX1:Rx_Receiver_Sensitivity	Float	AMI Rang		
Multi_Channel_BER_Compliance	ARX2:Rx_Receiver_Sensitivity	Float	AMI Rang		
Multi_Channel_BER_Compliance	ARX3:Rx_Receiver_Sensitivity	Float	AMI Rang		
Multi_Channel_BER_Compliance	ATX1:Tx_Dj	UI	AMI Range	<none>	0
Multi_Channel_BER_Compliance	ATX1:Tx_Rj	UI	AMI Range	<none>	0
Multi_Channel_BER_Compliance	ATX1:Tx_DCD	UI	AMI Range	<none>	0
Multi_Channel_BER_Compliance	ATX1:Modulation	String	AMI List	<none>	PAM4
Multi_Channel_BER_Compliance	ATX1:PAM4_Mapping	String	AMI List	<none>	0132
Multi_Channel_BER_Compliance	ATX1:Tx_Swing	Float	AMI Range	<none>	1.0
Multi_Channel_BER_Compliance	ATX1:tap_filter.-2	Tap	AMI List	ATX1:Tap	0
Multi_Channel_BER_Compliance	ATX1:tap_filter.-1	Tap	AMI List	ATX1:Tap	0

56G系统设计和通道仿真

1

Channel Network Characteristic Compliance



TX1
si_serdes
SI_Ideal_Tx
SI_Ideal_Tx
55.55ps - SerDes...
None

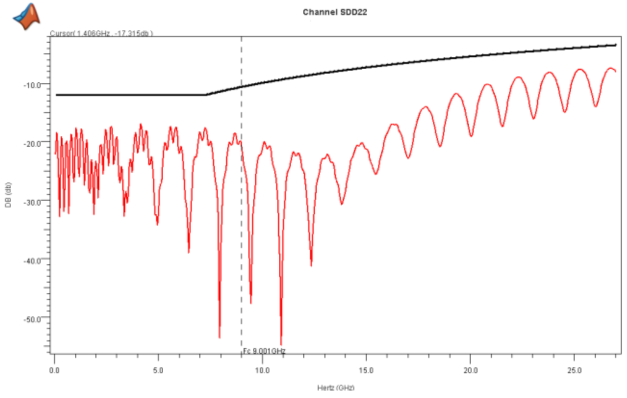
Use this sheet to validate channel SDD21 and SDD22 compliance

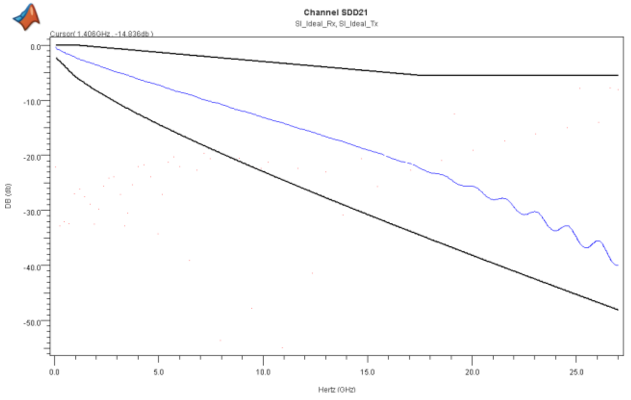
RX1
si_serdes
SI_Ideal_Rx
SI_Ideal_Rx

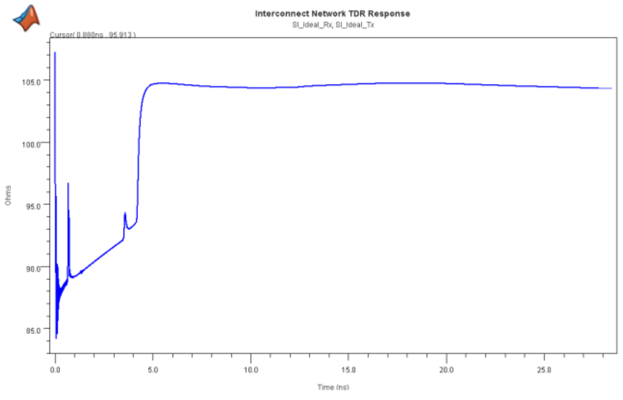
TX_...
TX_...
RX_...
RX_...

S1
s_CEI_56G_LR_Ref...

Rules file "Channel_Compliance_Rules" is included



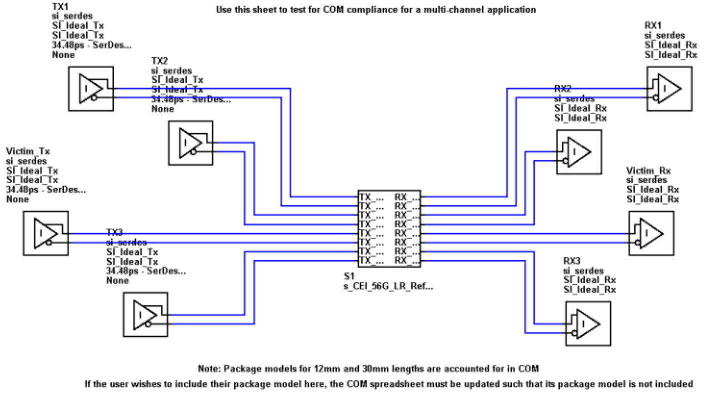




56G系统设计和通道仿真

2

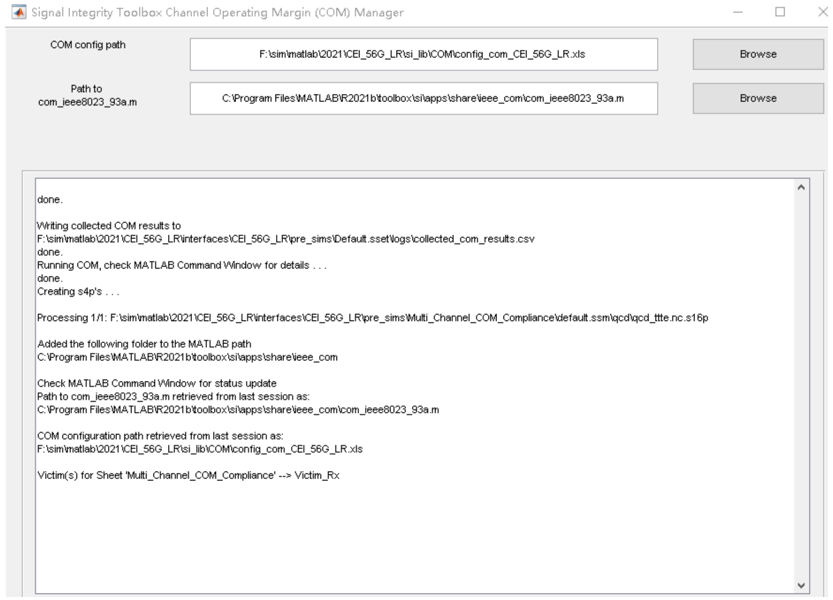
Multi Channel COM Compliance


Use this sheet to test for COM compliance for a multi-channel application

TX1
si_serdes
SI_Ideal_Tx
SI_Ideal_Tx
34.48ps - SerDes...
None
TX2
si_serdes
SI_Ideal_Tx
SI_Ideal_Tx
34.48ps - SerDes...
None
Victim_Tx
si_serdes
SI_Ideal_Tx
SI_Ideal_Tx
34.48ps - SerDes...
None
TX3
si_serdes
SI_Ideal_Tx
SI_Ideal_Tx
34.48ps - SerDes...
None
S1
s_CEI_56G_LR_Ref...
TX_...
RX_...
RX1
si_serdes
SI_Ideal_Rx
SI_Ideal_Rx
RX2
si_serdes
SI_Ideal_Rx
SI_Ideal_Rx
Victim_Rx
si_serdes
SI_Ideal_Rx
SI_Ideal_Rx
RX3
si_serdes
SI_Ideal_Rx
SI_Ideal_Rx

Note: Package models for 12mm and 30mm lengths are accounted for in COM

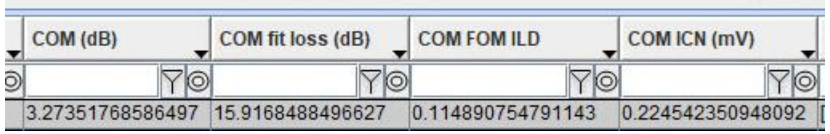
If the user wishes to include their package model here, the COM spreadsheet must be updated such that its package model is not included


Signal Integrity Toolbox Channel Operating Margin (COM) Manager
Browse
Browse

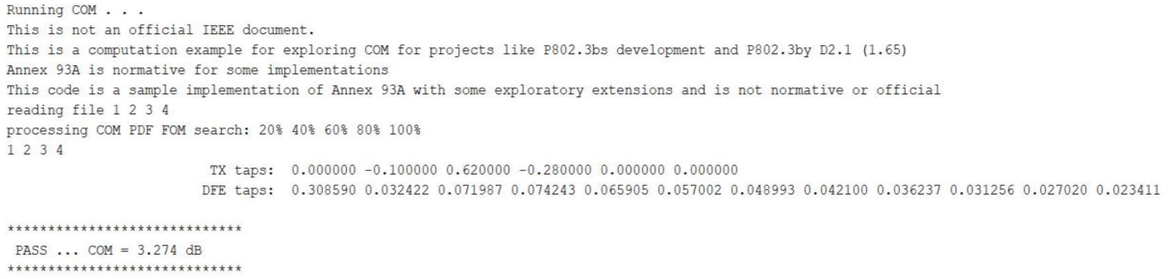
COM config path: F:\sim\matlab\2021\CEI_56G_LR\si_lib\COM\config_com_CEI_56G_LR.xls

Path to com_ieee8023_93a.m: C:\Program Files\MATLAB\R2021b\toolbox\si\apps\share\ieee_com\com_ieee8023_93a.m

```
done.

Writing collected COM results to
F:\sim\matlab\2021\CEI_56G_LR\interfaces\CEI_56G_LR\pre_sims\Default.sset\logs\collected_com_results.csv
done.
Running COM, check MATLAB Command Window for details . . .
done.
Creating s4p's . . .

Processing 1/1: F:\sim\matlab\2021\CEI_56G_LR\interfaces\CEI_56G_LR\pre_sims\Multi_Channel_COM_Compliance\default.ssm\qcd\qcd_ttte.nc.s16p

Added the following folder to the MATLAB path
C:\Program Files\MATLAB\R2021b\toolbox\si\apps\share\ieee_com

Check MATLAB Command Window for status update
Path to com_ieee8023_93a.m retrieved from last session as:
C:\Program Files\MATLAB\R2021b\toolbox\si\apps\share\ieee_com\com_ieee8023_93a.m

COM configuration path retrieved from last session as:
F:\sim\matlab\2021\CEI_56G_LR\si_lib\COM\config_com_CEI_56G_LR.xls

Victim(s) for Sheet 'Multi_Channel_COM_Compliance' --> Victim_Rx
```



COM (dB)	COM fit loss (dB)	COM FOM ILD	COM ICN (mV)
3.27351768586497	15.9168488496627	0.114890754791143	0.224542350948092

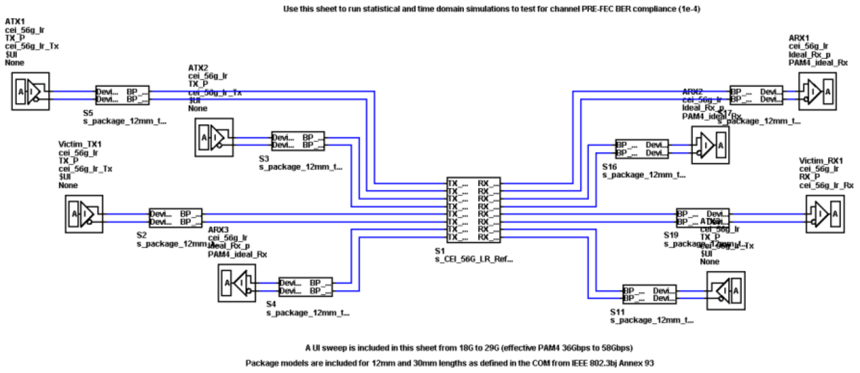


```
Running COM . . .
This is not an official IEEE document.
This is a computation example for exploring COM for projects like P802.3bs development and P802.3by D2.1 (1.65)
Annex 93A is normative for some implementations
This code is a sample implementation of Annex 93A with some exploratory extensions and is not normative or official
reading file 1 2 3 4
processing COM PDF FOM search: 20% 40% 60% 80% 100%
1 2 3 4
                         TX taps:  0.000000 -0.100000 0.620000 -0.280000 0.000000 0.000000
                        DFE taps:  0.308590 0.032422 0.071987 0.074243 0.065905 0.057002 0.048993 0.042100 0.036237 0.031256 0.027020 0.023411

*****************************
 PASS ... COM = 3.274 dB
*****************************
```

56G系统设计和通道仿真

3

Multi Channel BER Simulation

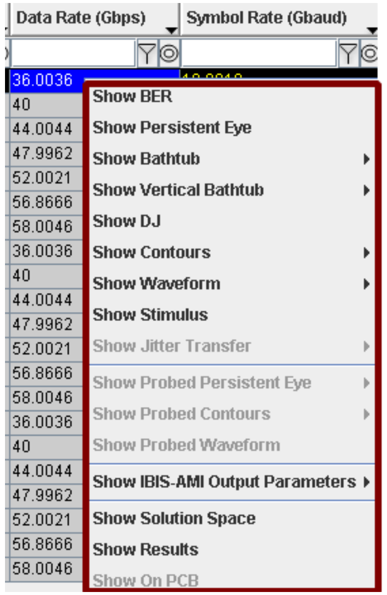


Use this sheet to run statistical and time domain simulations to test for channel PRE-FEC BER compliance (1e-4)

ATX1
cei_56g_lr
TX_P
cei_56g_lr_Tx
ATX2
Victim_TX1
S5
s_package_12mm_t...
S3
S2
S4
ARX3
cei_56g_lr
Ideal_Rx_p
PAM4_ideal_Rx
S1
s_CEI_56G_LR_Ref...
ARX1
cei_56g_lr
Ideal_Rx_p
PAM4_ideal_Rx
ARX2
S16
Victim_RX1
cei_56g_lr
RX_P
cei_56g_lr_Rx
S19
S11
s_package_12mm_t...

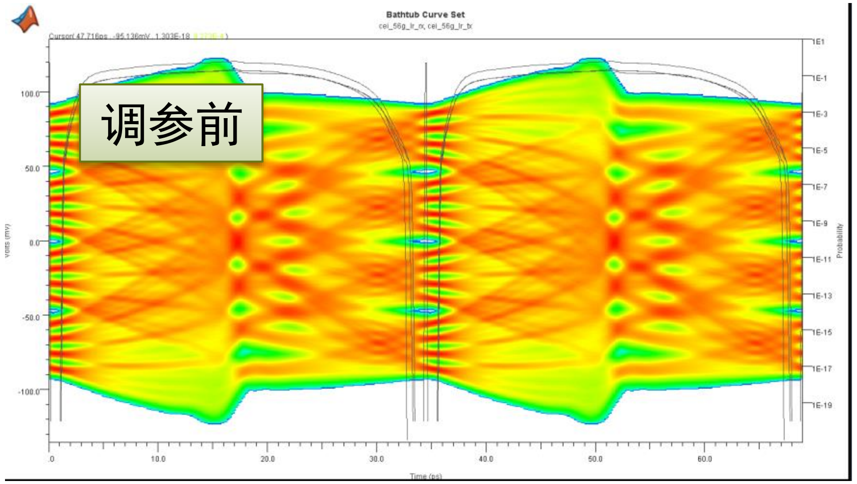
A UI sweep is included in this sheet from 18G to 29G (effective PAM4 36Gbps to 58Gbps)

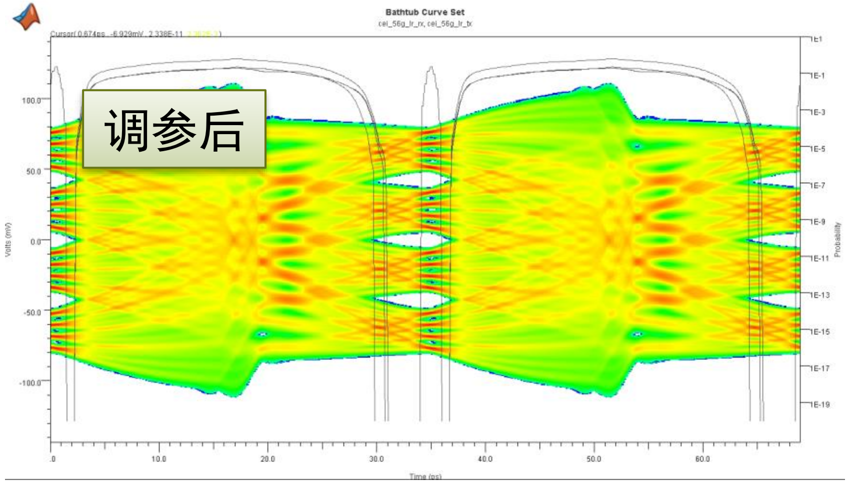
Package models are included for 12mm and 30mm lengths as defined in the COM from IEEE 802.3bj Annex 93



Data Rate (Gbps)	Symbol Rate (Gbaud)
36.0036	
40	
44.0044	
47.9962	
52.0021	
56.8666	
58.0046	
36.0036	
40	
44.0044	
47.9962	
52.0021	
56.8666	
58.0046	
36.0036	
40	
44.0044	
47.9962	
52.0021	
56.8666	
58.0046	

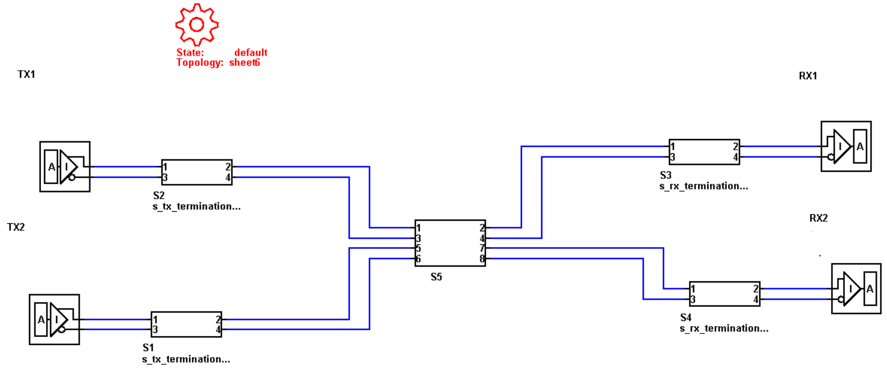
Show BER
Show Persistent Eye
Show Bathtub
Show Vertical Bathtub
Show DJ
Show Contours
Show Waveform
Show Stimulus
Show Jitter Transfer
Show Probed Persistent Eye
Show Probed Contours
Show Probed Waveform
Show IBIS-AMI Output Parameters
Show Solution Space
Show Results
Show On PCB



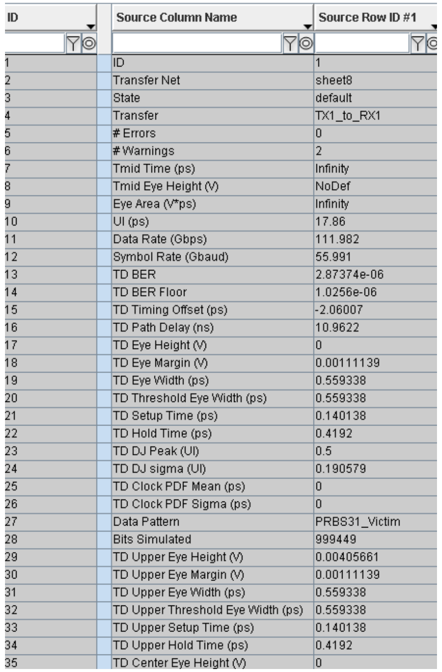


112G系统设计和通道仿真

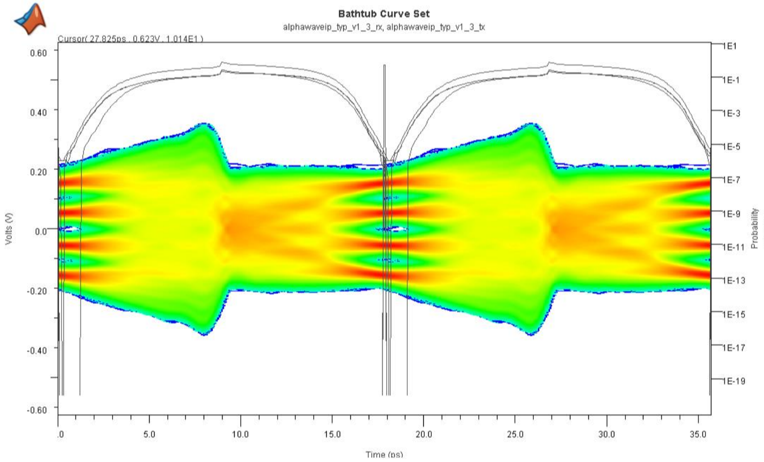
有源仿真


State: default
Topology: sheet6
TX1
TX2
RX1
RX2
S2
s_tx_termination...
S1
s_tx_termination...
S5
S3
s_rx_termination...
S4
s_rx_termination...

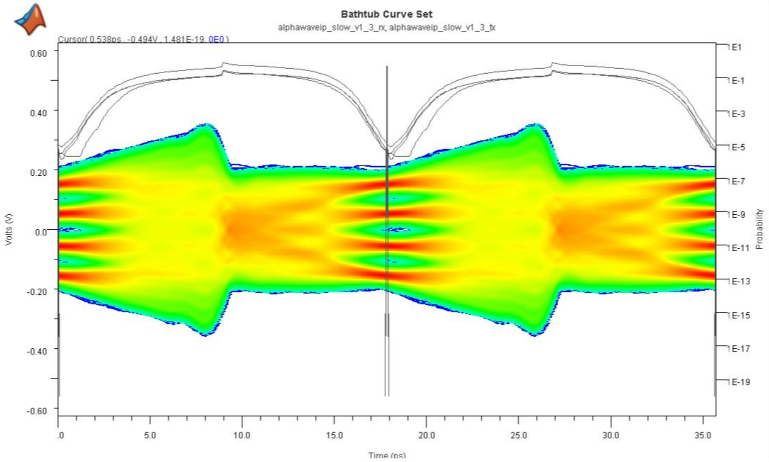
Corner	UI (ps)	Data Rate (Gbps)	Symbol Rate (Gbaud)	TD BER	Pattern
Typ	17.86	111.982	55.991	2.8737E-06	PRBS31Q
Slow	17.86	111.982	55.991	1.2187E-05	PRBS31Q
Fast	17.86	111.982	55.991	1.0256E-06	PRBS31Q



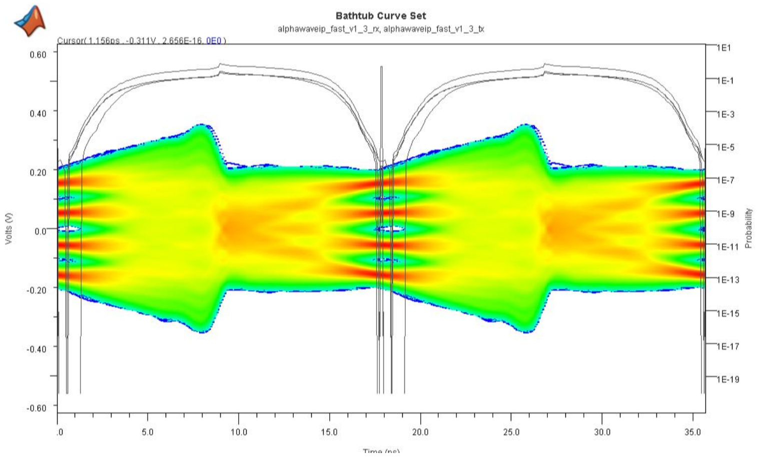
ID	Source Column Name	Source Row ID #1
1	ID	1
2	Transfer Net	sheet8
3	State	default
4	Transfer	TX1_to_RX1
5	# Errors	0
6	# Warnings	2
7	Tmid Time (ps)	Infinity
8	Tmid Eye Height (V)	NoDef
9	Eye Area (V*ps)	Infinity
10	UI (ps)	17.86
11	Data Rate (Gbps)	111.982
12	Symbol Rate (Gbaud)	55.991
13	TD BER	2.87374e-06
14	TD BER Floor	1.0256e-06
15	TD Timing Offset (ps)	-2.06007
16	TD Path Delay (ns)	10.9622
17	TD Eye Height (V)	0
18	TD Eye Margin (V)	0.00111139
19	TD Eye Width (ps)	0.559338
20	TD Threshold Eye Width (ps)	0.559338
21	TD Setup Time (ps)	0.140138
22	TD Hold Time (ps)	0.4192
23	TD DJ Peak (UI)	0.5
24	TD DJ sigma (UI)	0.190579
25	TD Clock PDF Mean (ps)	0
26	TD Clock PDF Sigma (ps)	0
27	Data Pattern	PRBS31_Victim
28	Bits Simulated	999449
29	TD Upper Eye Height (V)	0.00405661
30	TD Upper Eye Margin (V)	0.00111139
31	TD Upper Eye Width (ps)	0.559338
32	TD Upper Threshold Eye Width (ps)	0.559338
33	TD Upper Setup Time (ps)	0.140138
34	TD Upper Hold Time (ps)	0.4192
35	TD Center Eye Height (V)	0



typ



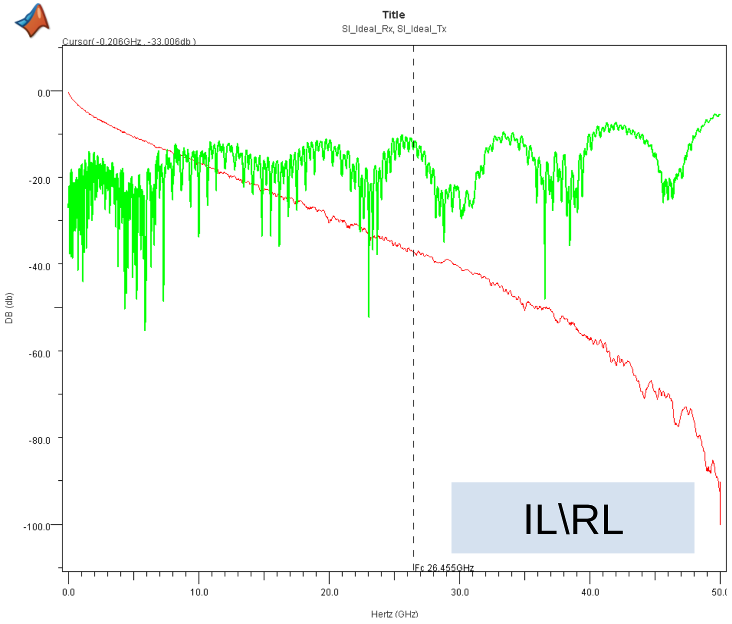
slow

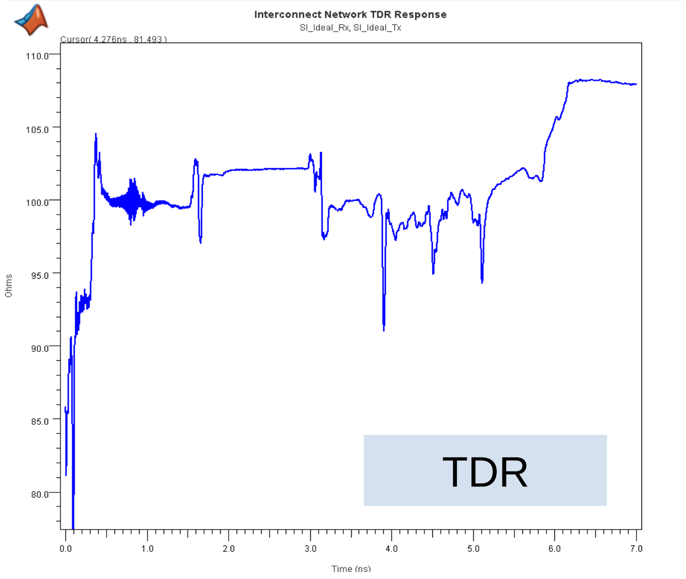


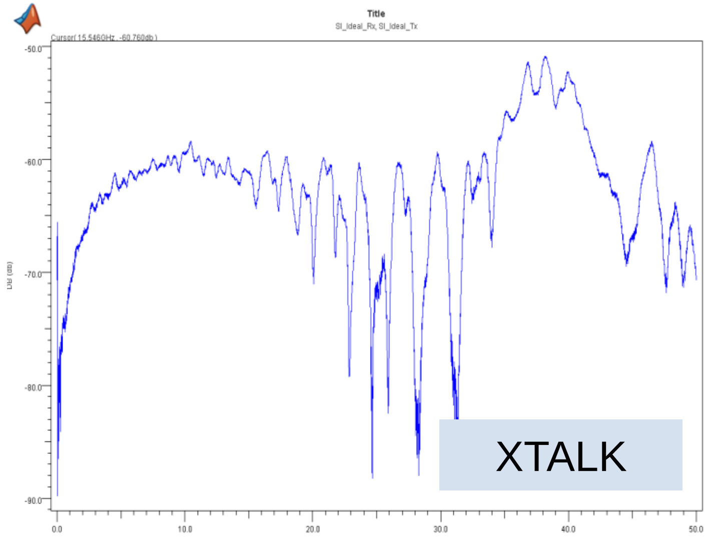
fast

112G系统设计和通道仿真

无源仿真







目录

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2 SerDes架构设计和系统开发

3 SerDes仿真验证

4 IBIS-AMI模型建立

5 系统链路SI仿真

➡ 6 总结

总结

- ZTE有SerDes系统开发标准化流程
- 仿真工具可以支撑ZTE的SerDes系统开发需求
- 实现了56G\112G SerDes系统设计和通道仿真验证，可以评估BER\眼图等关键性能指标
- 助力产品化落地

MATLAB EXPO

谢谢

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