



MATLAB EXPO 2017

通往5G之路：
无线系统的仿真和原型实现

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通信, 电子, 半导体行业经理, MathWorks

目录

- 5G系统的挑战
- 从算法到天线的的设计
- 空口的测试 (Over the Air Testing and Software Defined Radio)
- 原型实现

5G 展望和应用场景

5G的技术需求

- 新的物理层技术
- 新的RF架构
- 新的网络配置
- 新的设计方法和外场测试

5G 技术挑战

- 毫米波 (mmWave)
- 天线和中射频设计
- 信道模型(>6GHz)
- 新的信道编码 Polar Code
- 新的波形 (f-OFDM)
- 多天线 Massive MIMO
- 快速原型
- 外场测试

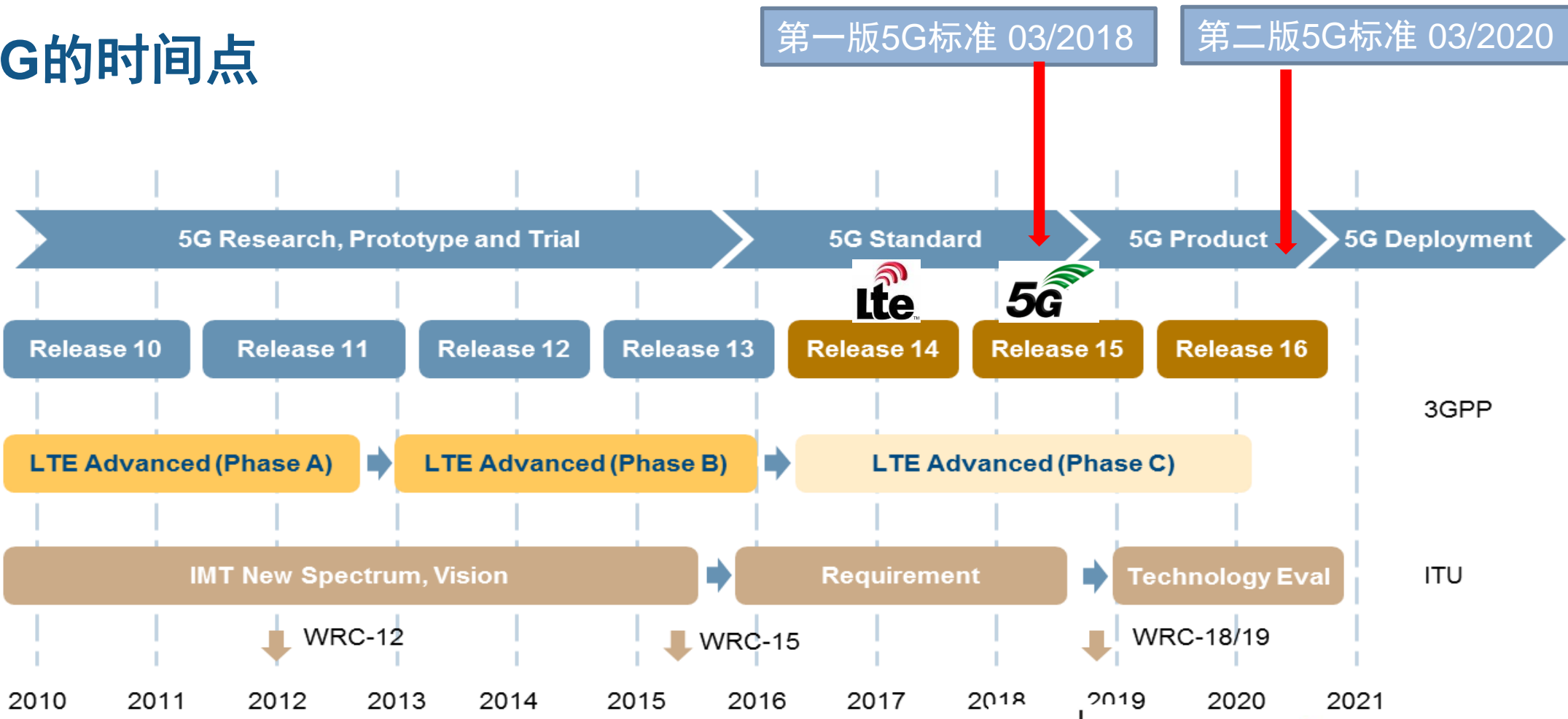


IoT 物联网

V2X 车联网

Ultra-Fast Mobile 超高速宽带

5G的时间点



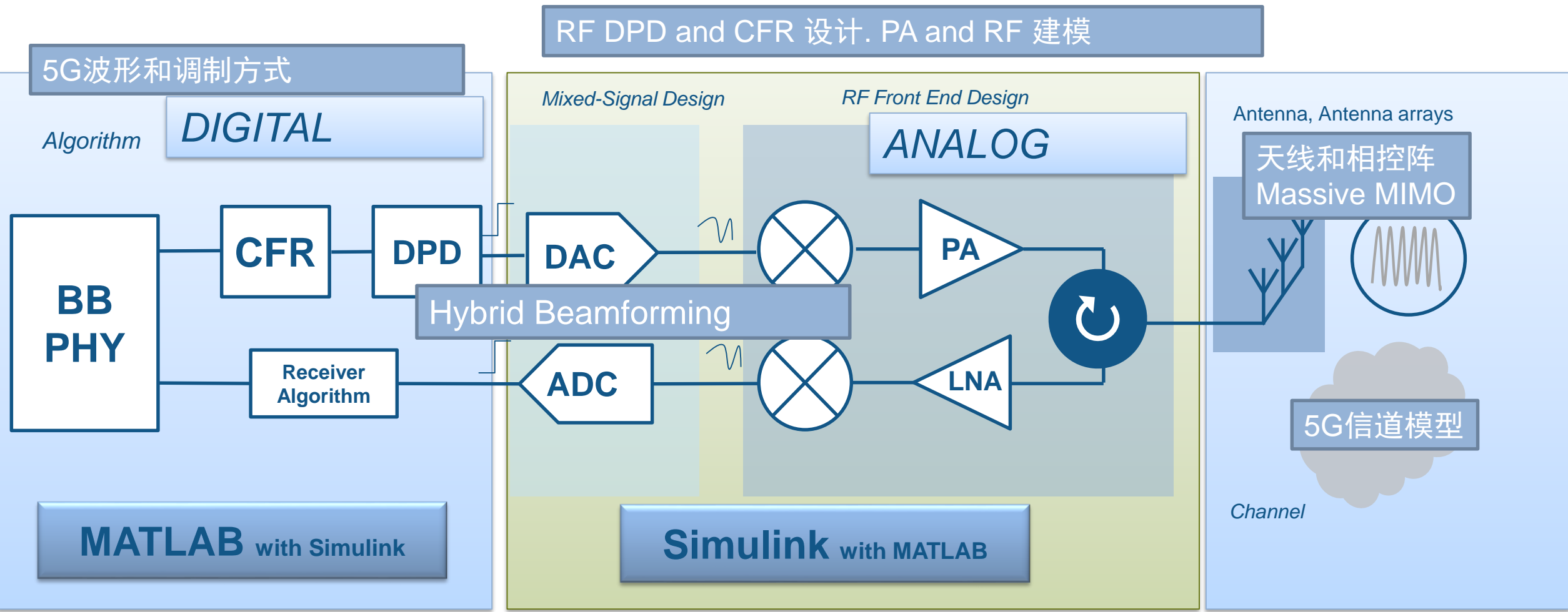
- **LTE: Long Term Evolution**
 - Long Term Employment
- **5G: NR: New Radio**
 - Never Retirement

5G Library Support Package

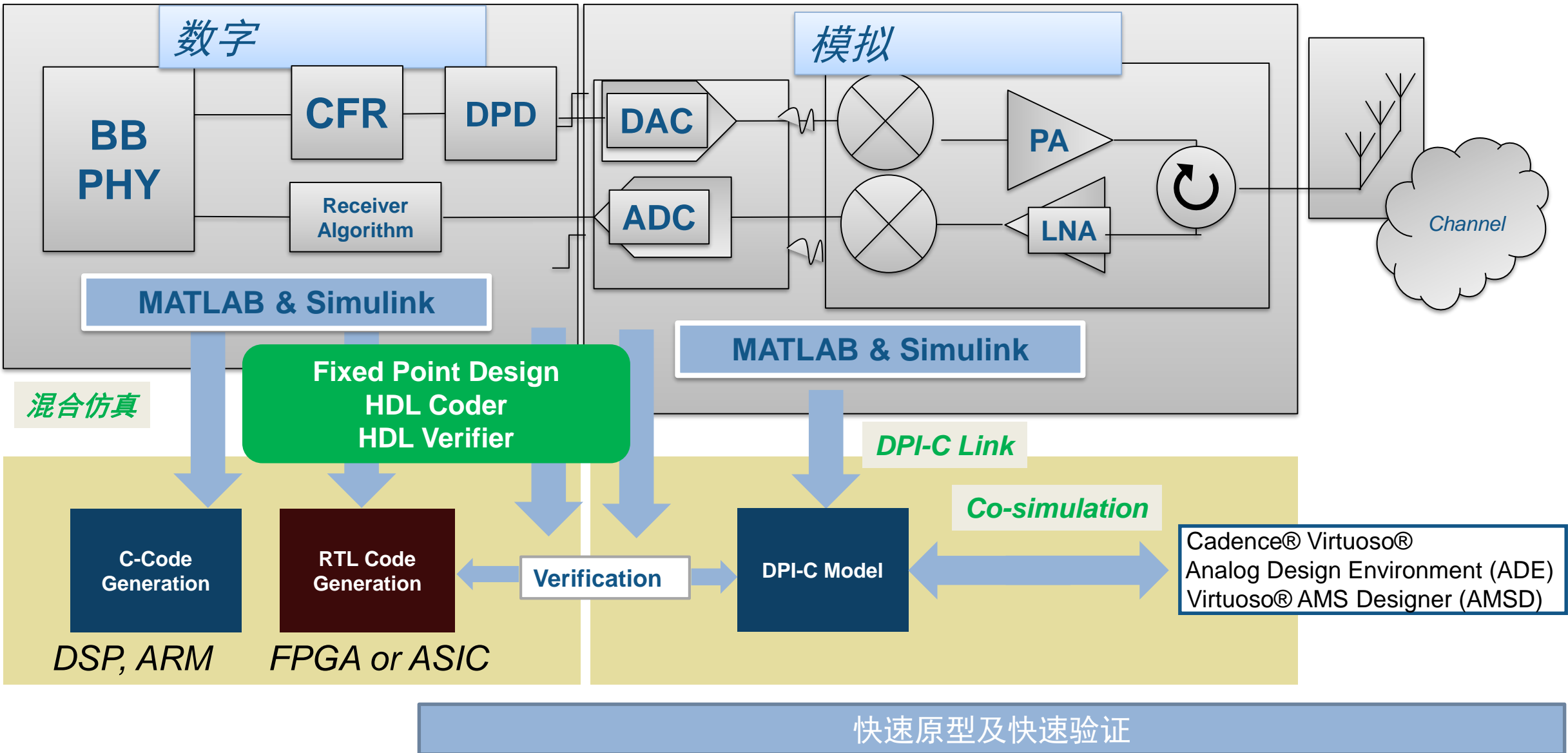
Source: 3GPP

LTE System Toolbox

5G: 从算法到天线

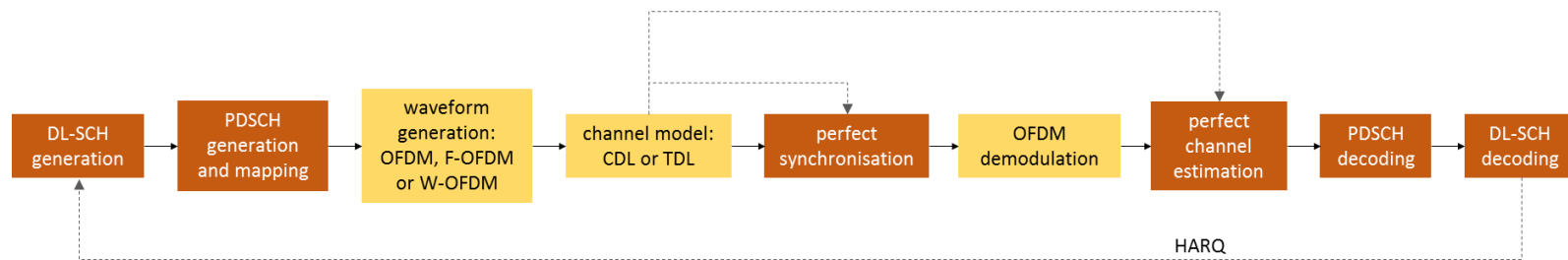
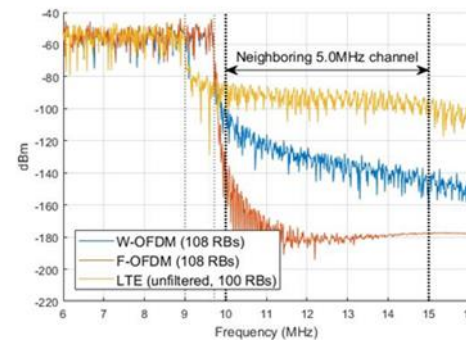
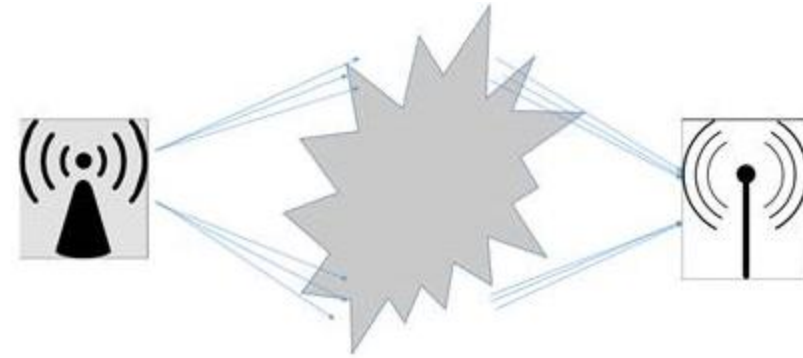


5G: 从算法到实现



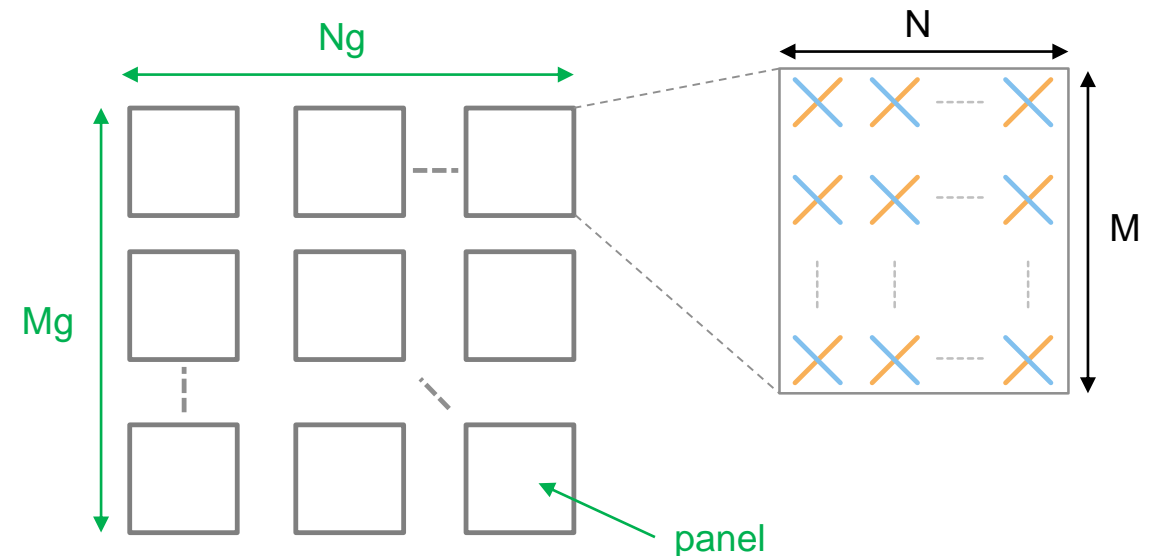
5G Support Package

- 5G 信道模型(3GPP TR 38.900)
- 新的波形(F-OFDM, W-OFDM)
- 链路仿真参考平台

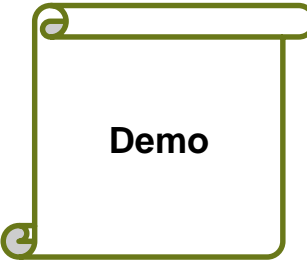


5G 信道模型

- 5G 信道模型 TR 38.900的数学实现
- 包括以下可调参数
 - Delay profile: TDL and CDL profiles: A, B, C, D, E or custom
 - Channel delay spread
 - 多普勒
 - MIMO 相关性
 - CDL: spatial channel model, includes also:
 - Antenna array geometry [M, N, P, Mg, Ng]

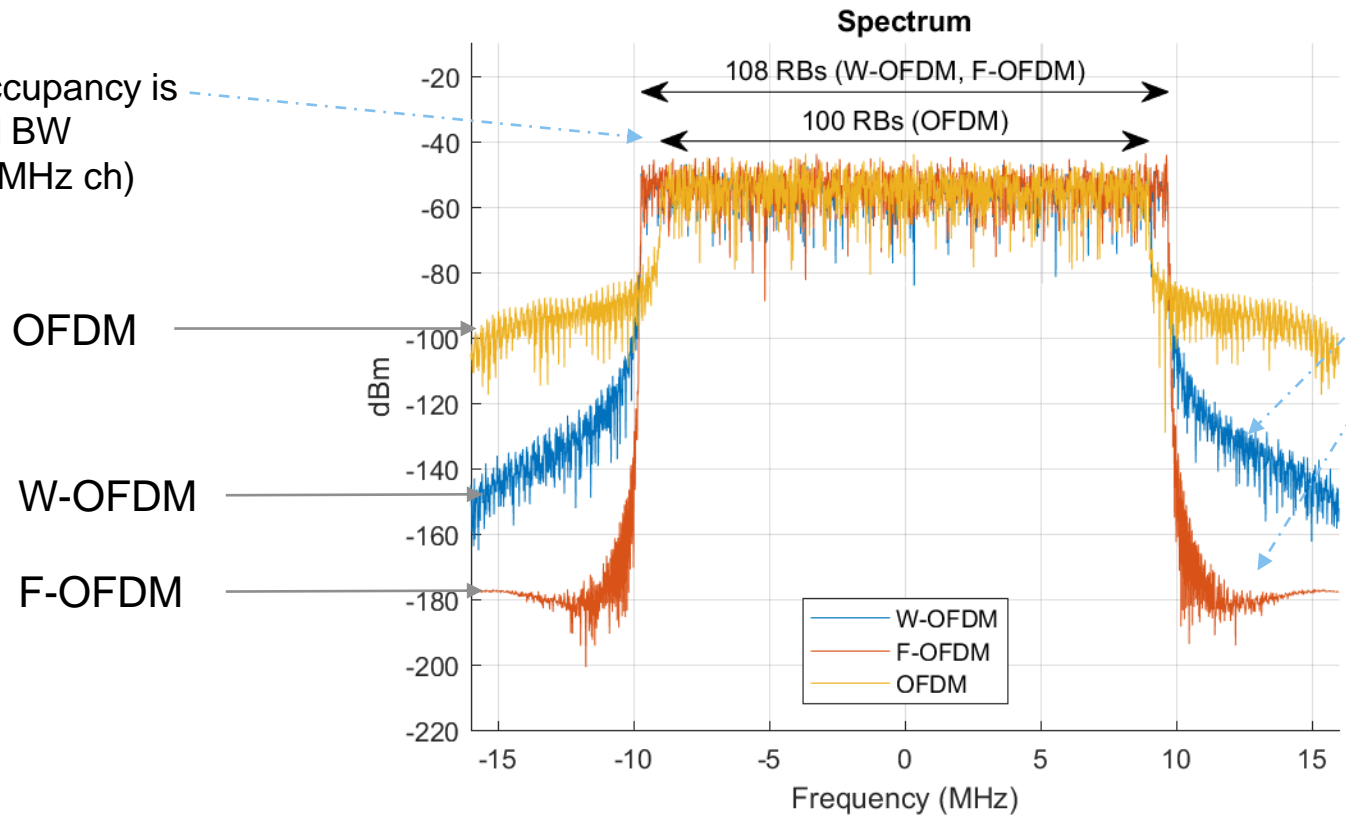


新的波形的分析



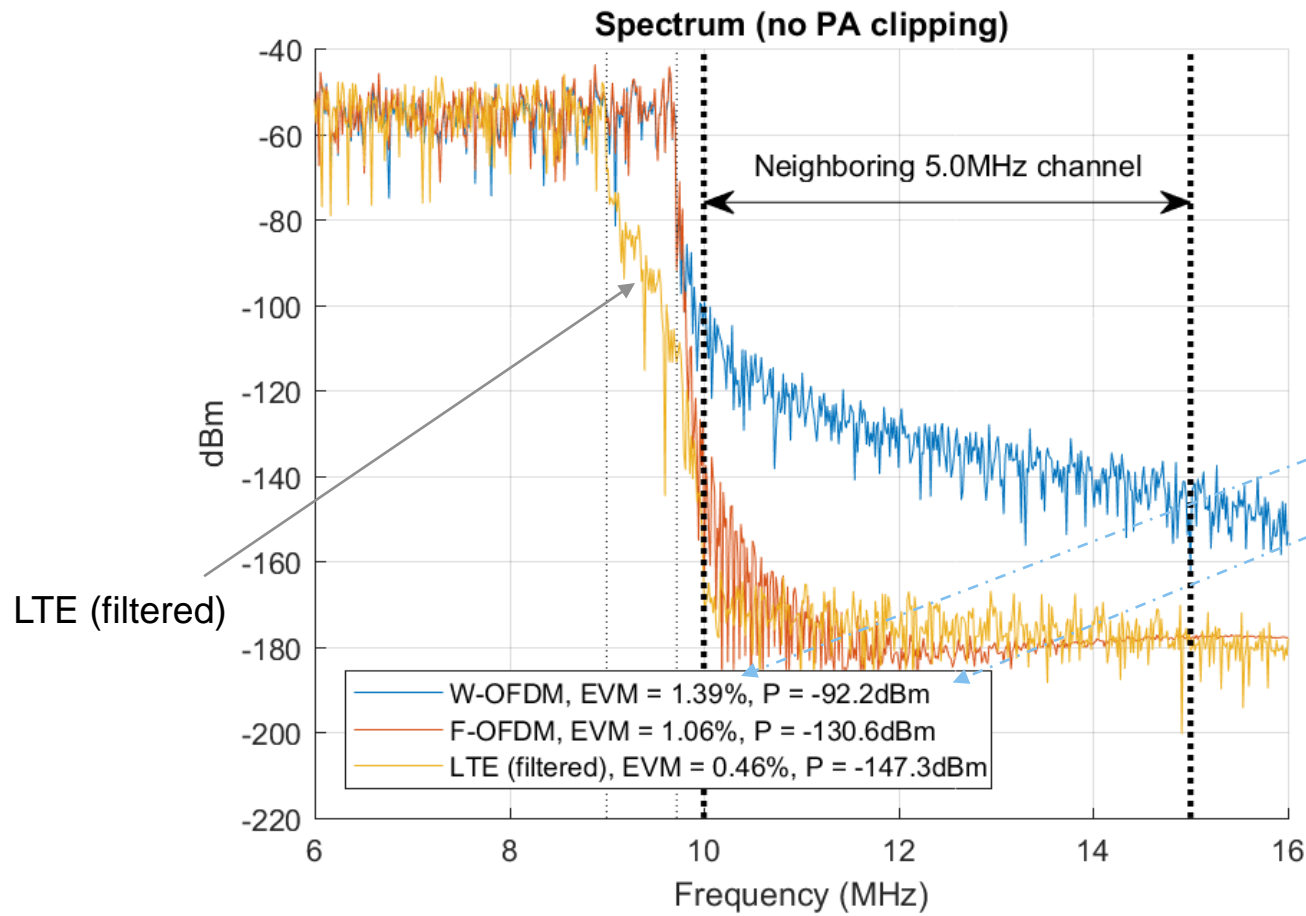
- 5G 增加带宽效率（超过LTE的90%的限制）

LTE: Max BW occupancy is 90% of allocated BW (100 RBs for 20 MHz ch)



In 5G the 90% limit does not apply, we need to design a filter (F-OFDM) or windowing parameters (W-OFDM) to limit out of band emissions

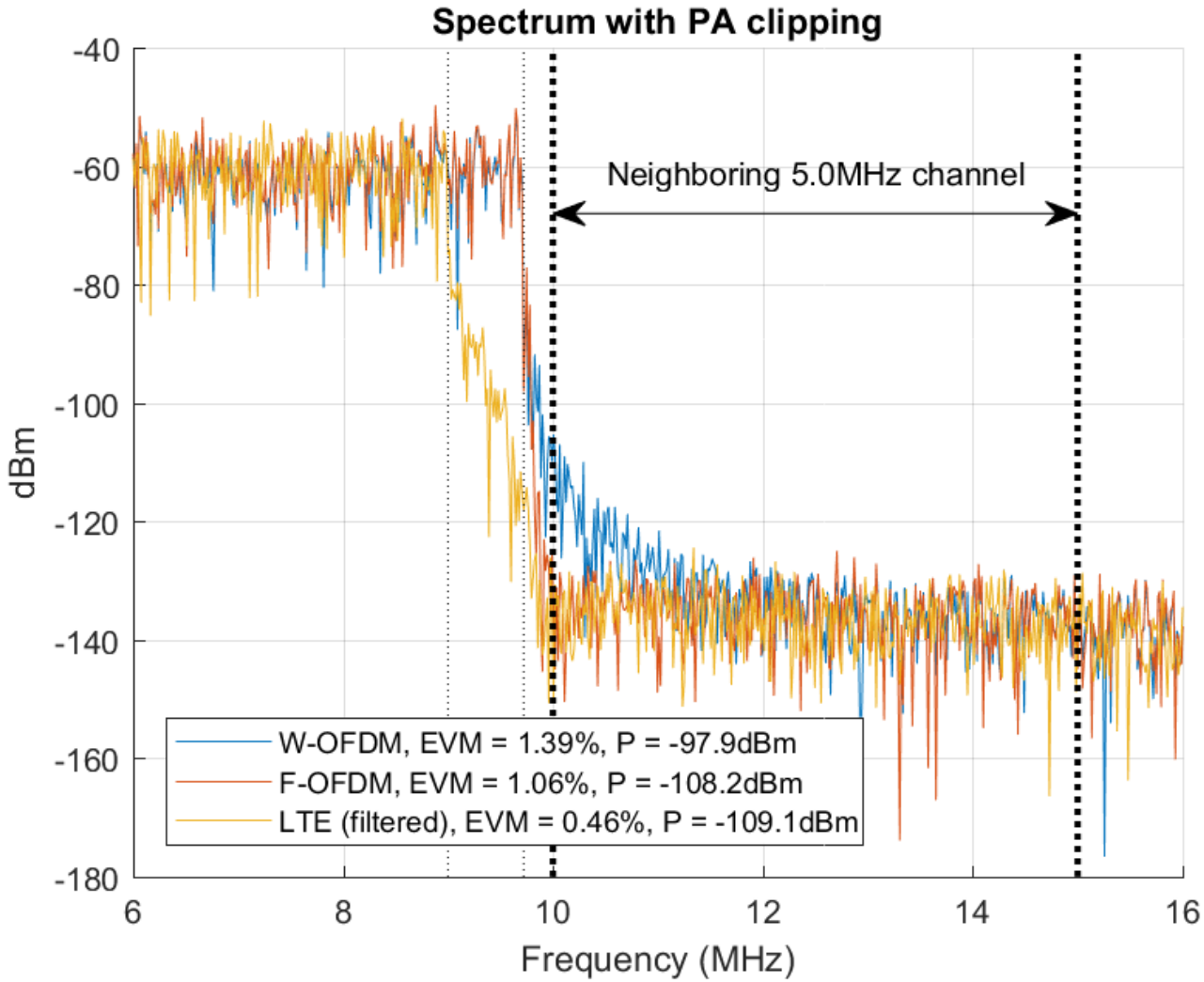
仿真带外特性



Filter和Window如何应先带外特性

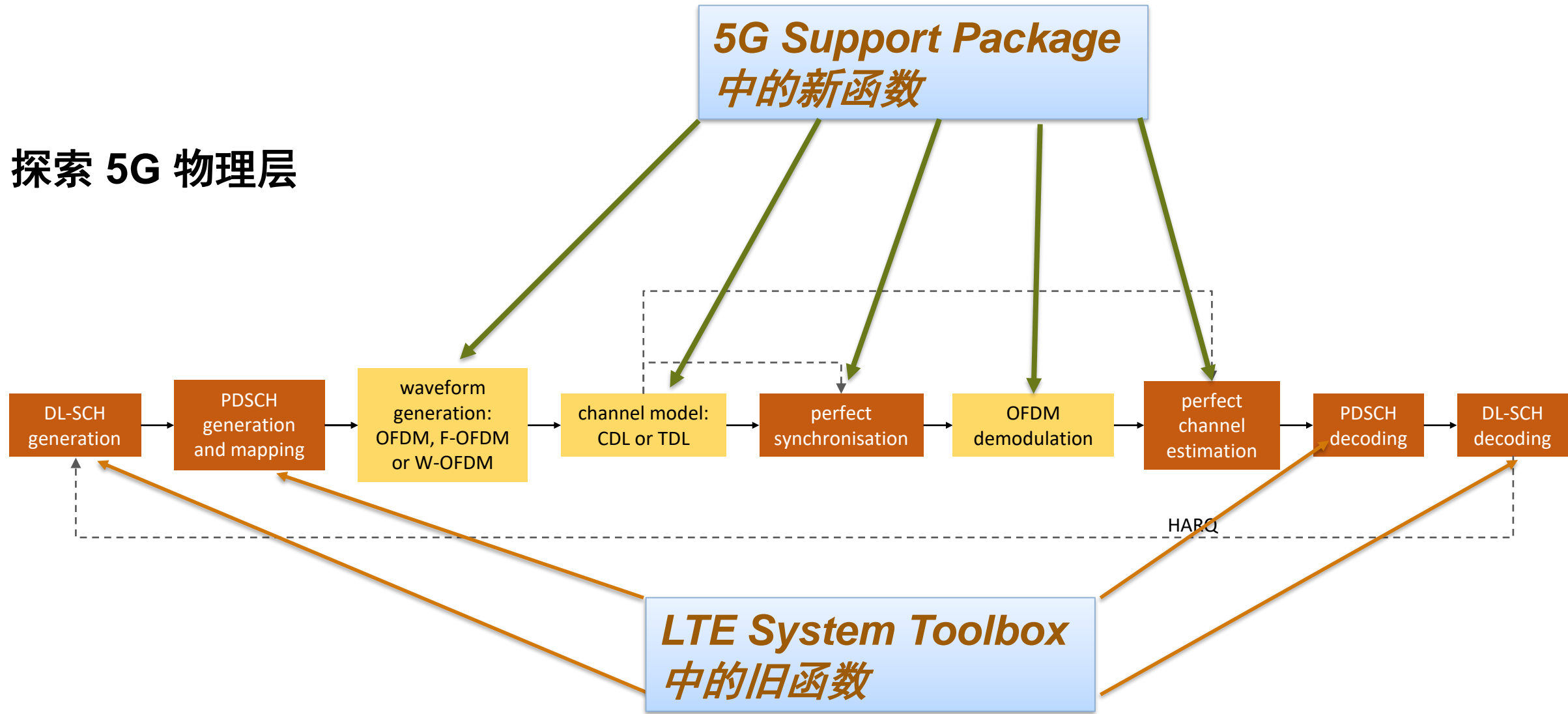
- Distortion: EVM
- Energy leakage to neighbouring bands

功率放大器的非线性特性的影响



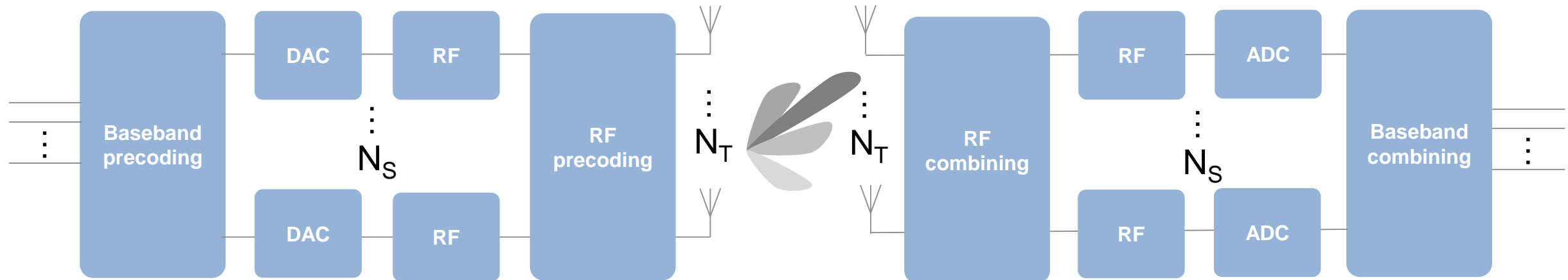
5G 链路仿真平台

探索 5G 物理层



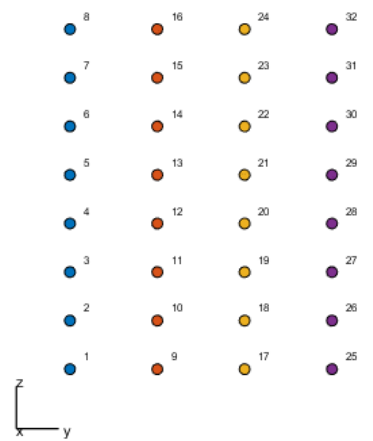
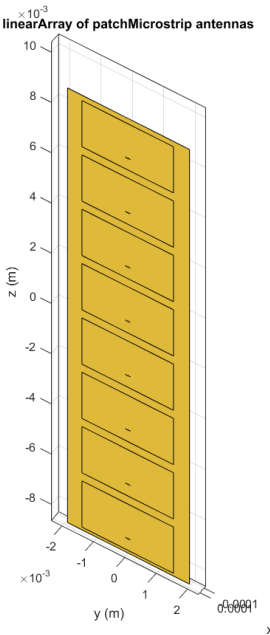
Hybrid Beamforming

- Beamforming 在基带和RF中的混合设计
 - 性能的Trade-off, power dissipation, 实现复杂度的考量
- 不同的模拟器件的实现方式
 - Phase shifters vs. Switching networks
- 不同模拟器件的结构
 - RF chains 和每条天线相连还是和每个子天线阵相连

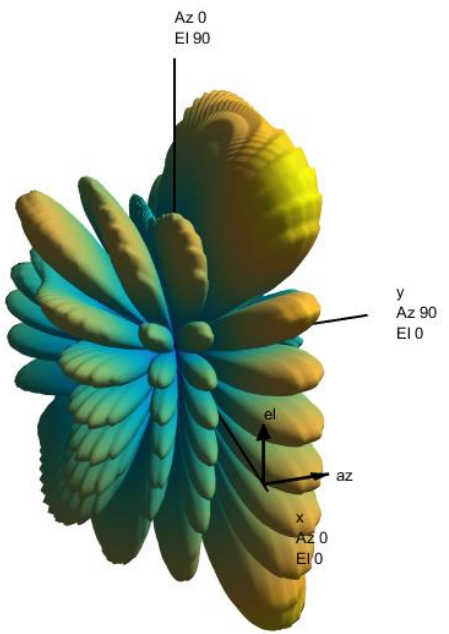
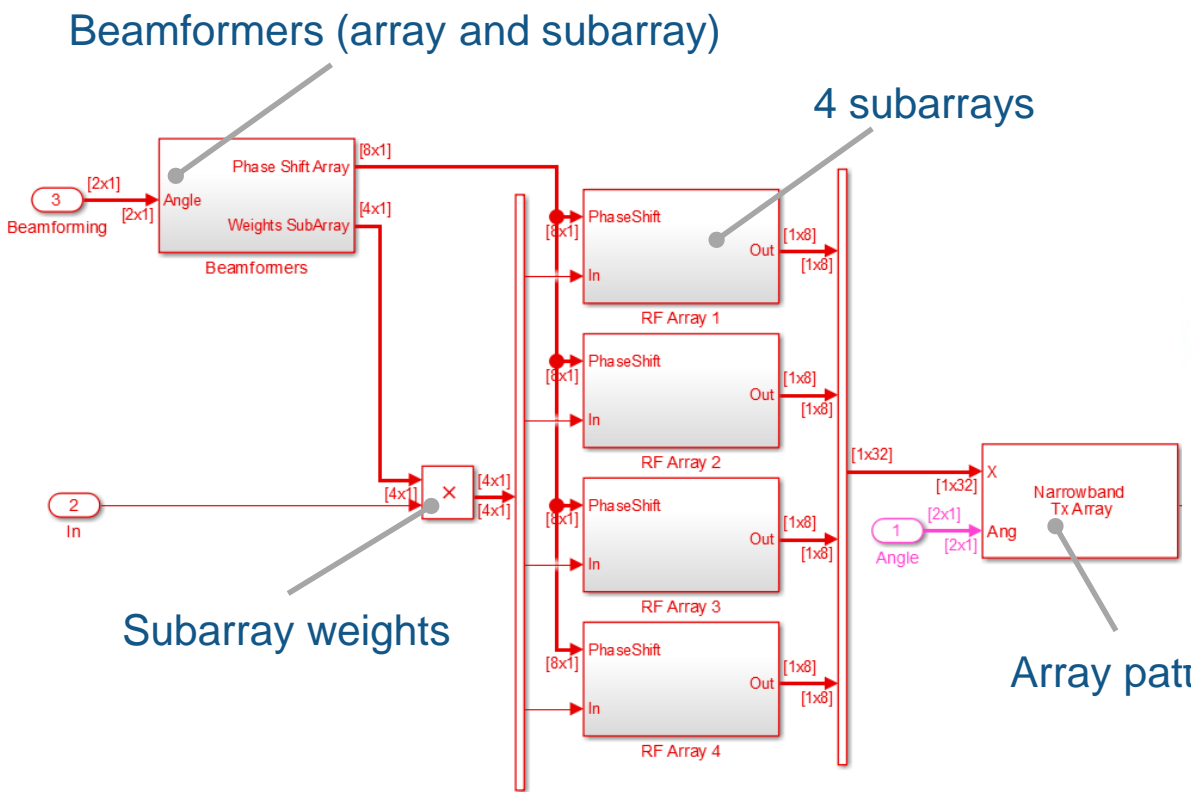


举例: Hybrid Beamforming 发送端相控阵

- 4 subarrays of 8 patch antennas operating at 66GHz → 8x4 = 32 antennas
- 数字beamforming 到 4 个子天线阵 (azimuth steering)
- RF beamforming (phase shifters) 到 8 个天线阵 (elevation steering)



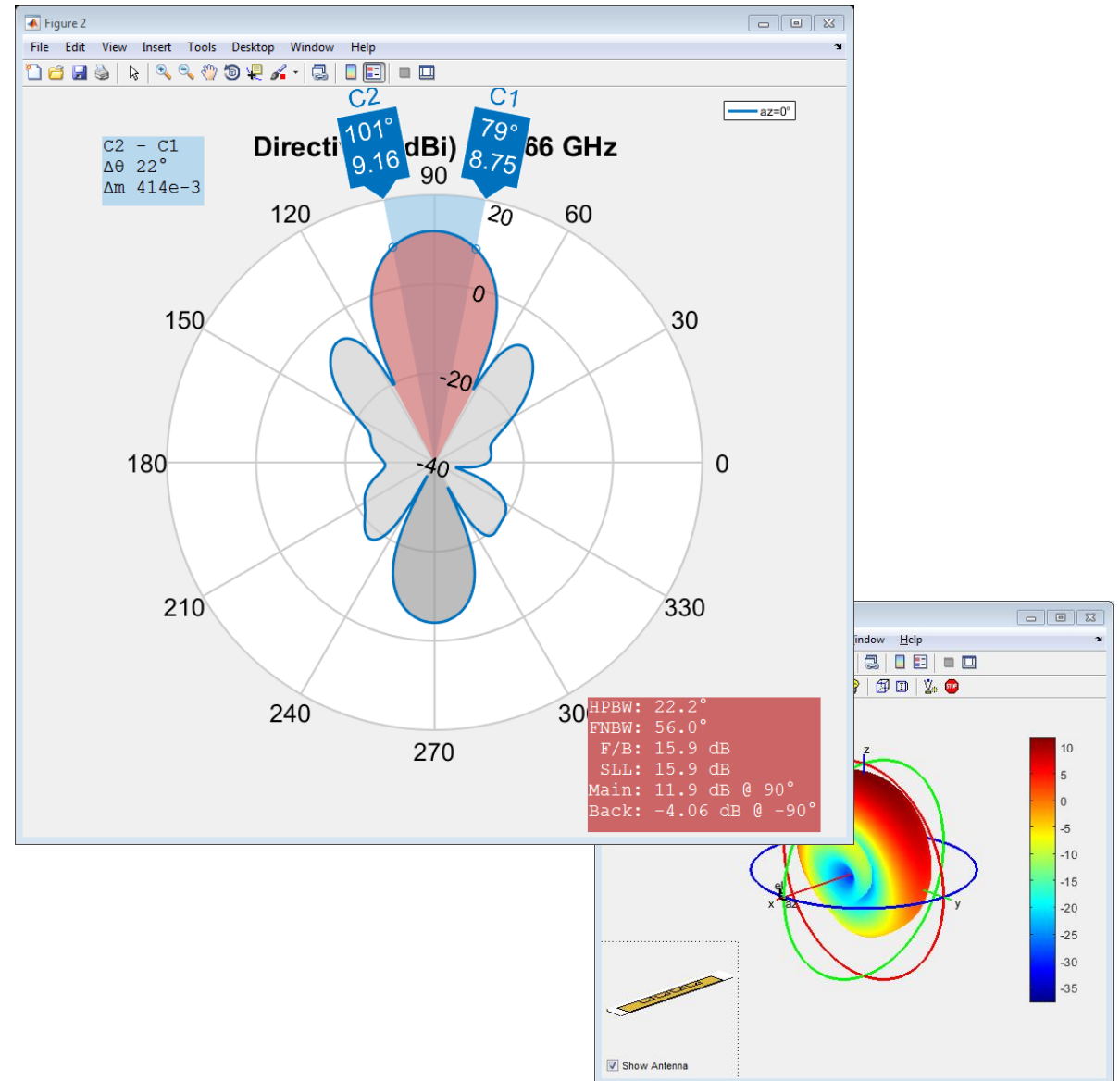
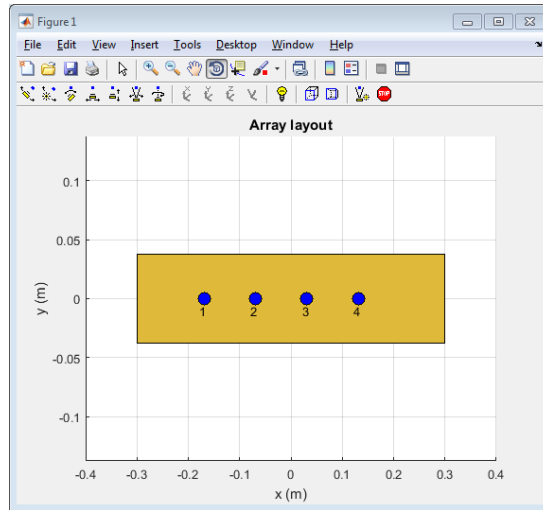
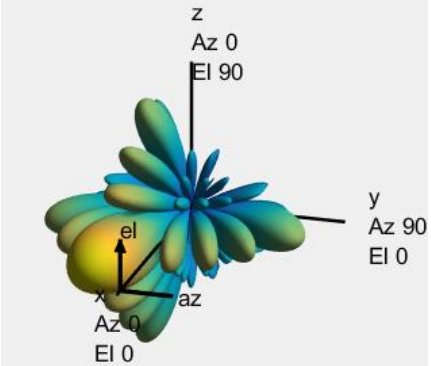
Array Span:
 X axis = 0.000 mm
 Y axis = 11.680 mm
 Z axis = 15.141 mm



例子：你的第一个自行设计的天线

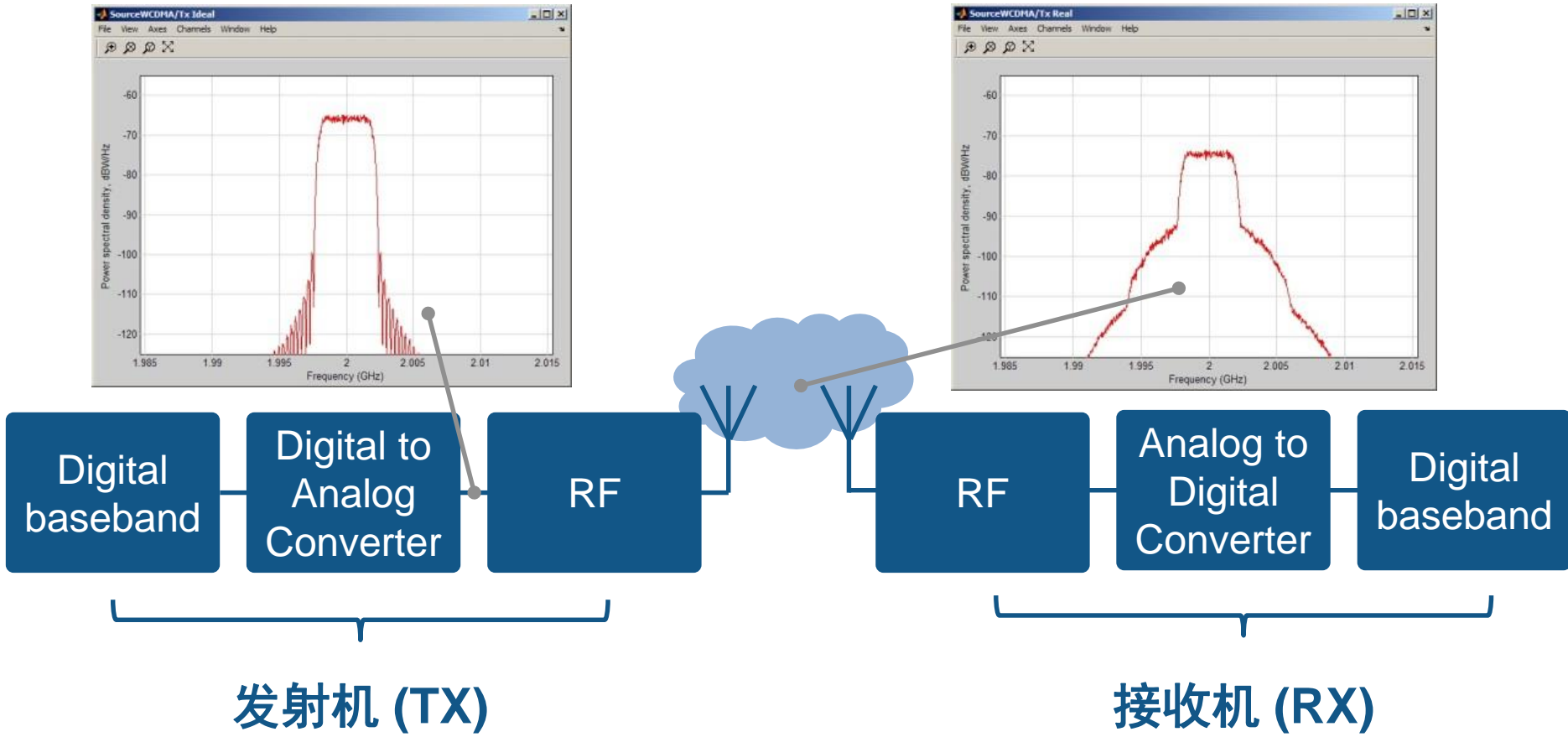
```
>> a = linearArray
>> a.Element = p;
>> a.ElementSpacing = 0.1;
>> a.NumElements = 4;
>> layout(a);
>> pattern(a, 1.66e9);
```

3D Radiation Pattern for UE #1

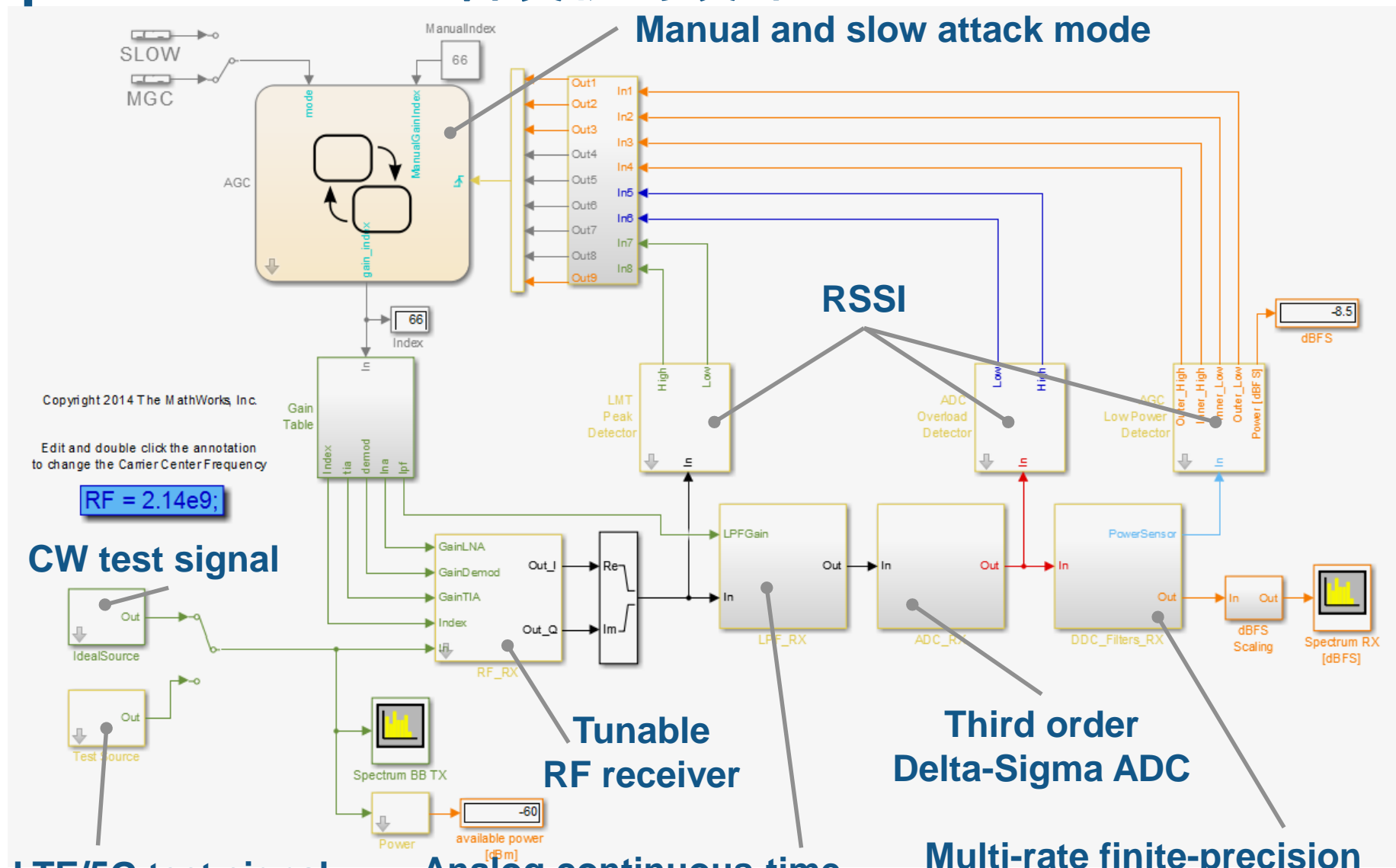


为什么要在5G链路级仿真中考虑RF

- 5G的mmWave高频设计需要考虑RF
- RF和基带在5G设计中需要统一考虑



Example: AD9361 RF 首发机的设计 AGC



Custom LTE/5G test signal

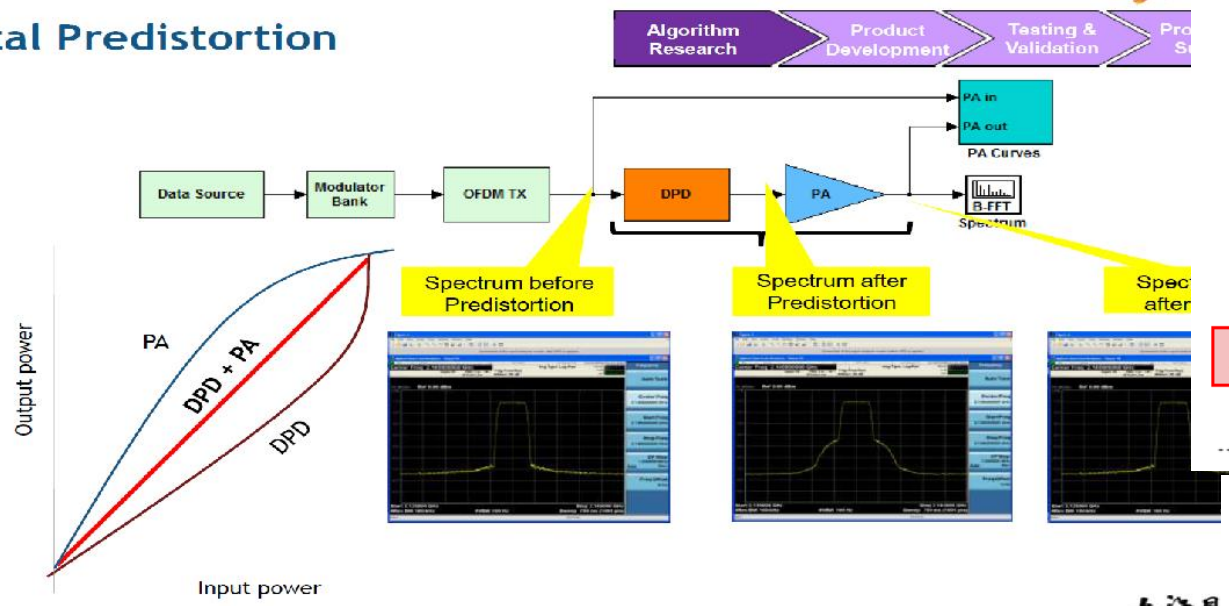
Analog continuous-time programmable filters

Third order Delta-Sigma ADC

Multi-rate finite-precision programmable decimation filters

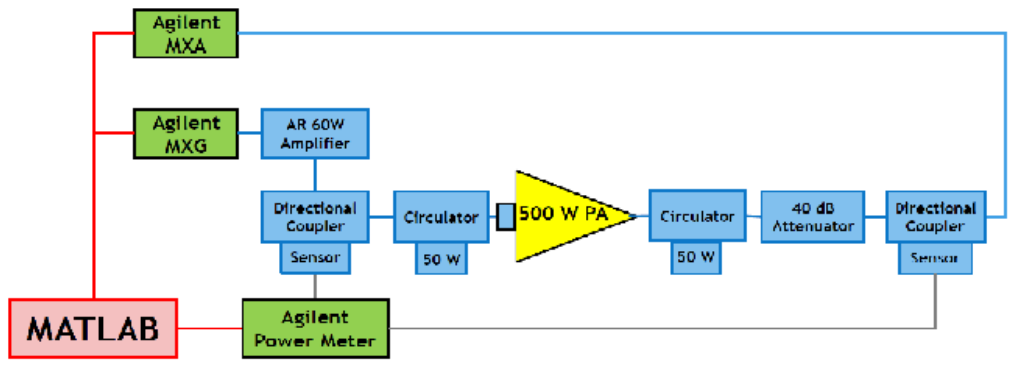
DPD: 基站中的RF with MATLAB

Digital Predistortion



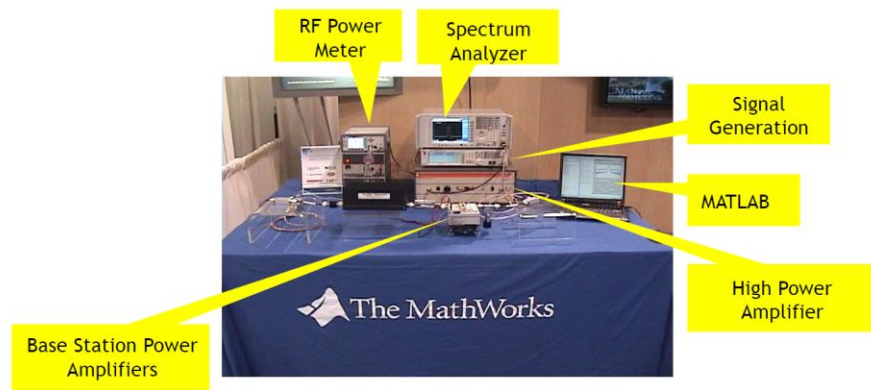
上海贝尔 Alcatel-Lu

Algorithm Development Platform



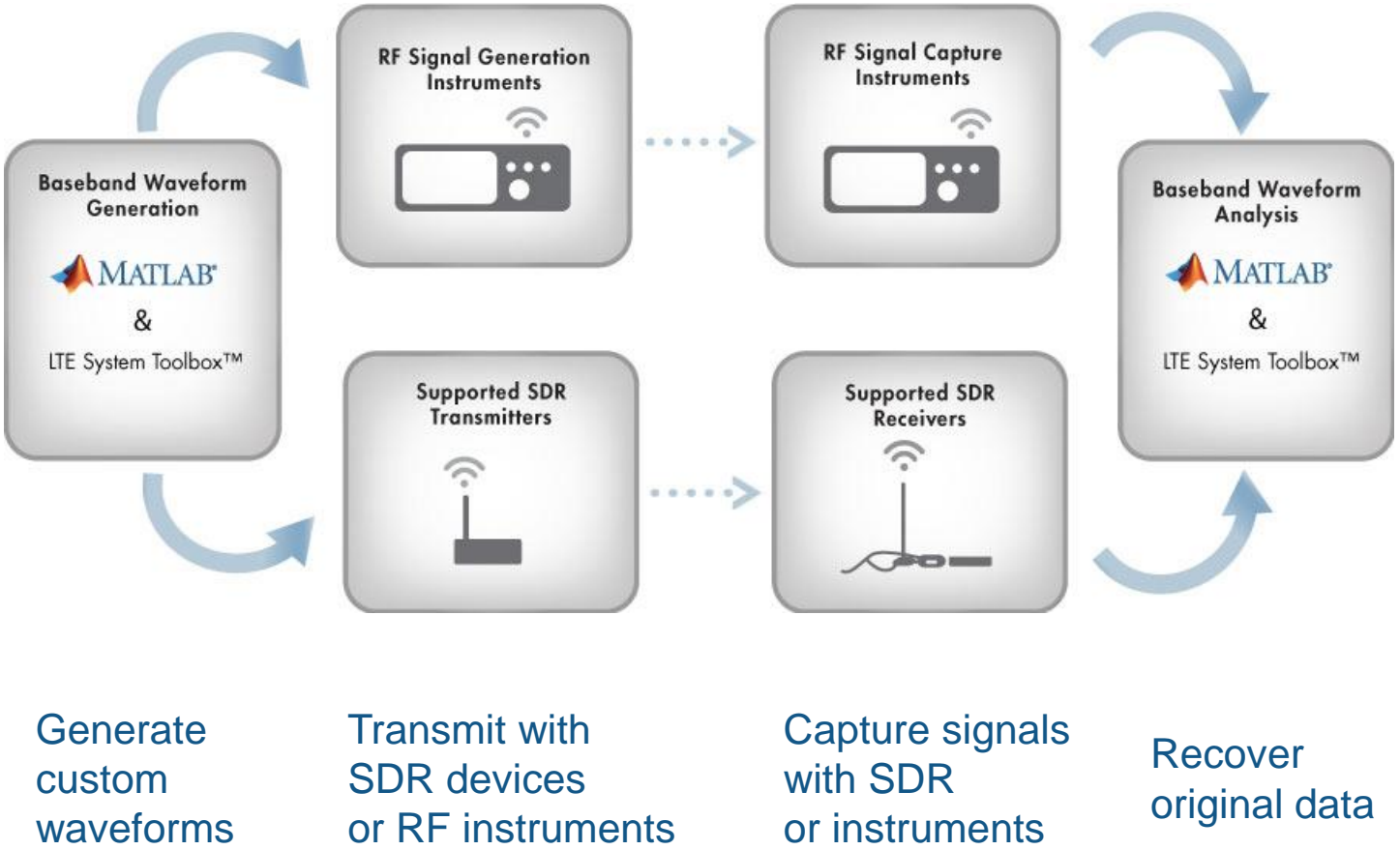
上海贝尔 Alcatel-Lucent

上海贝尔的实例 [The Base Station RF Development with MATLAB](#)



上海贝尔 Alcatel-Lucent

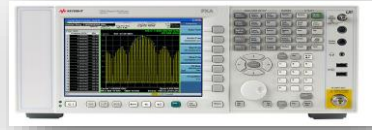
5G - Over-the-air testing with SDRs & RF instruments



Range of supported hardware



RF Signal Generator



Spectrum Analyzer



Zynq Radio SDR



USRP SDR

Example: MATLAB 连接 SDR and AD9361/9371 进行验证

AD9361 RF Transceiver

Baseband Waveform Generation

MATLAB
&
LTE System Toolbox™



RF Signal Generation

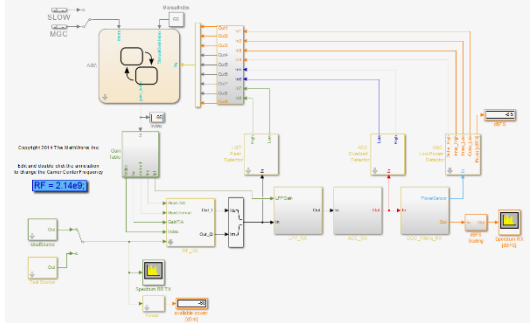
HW Support package

SDR platform



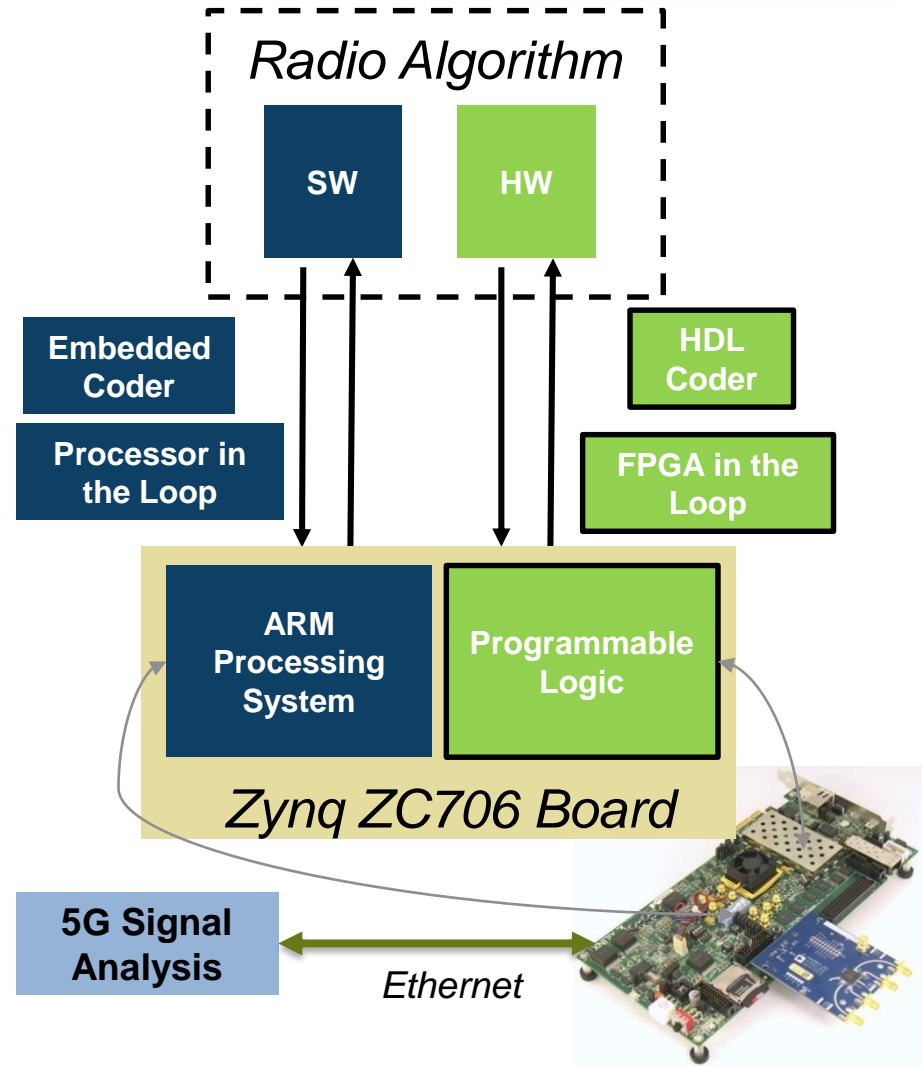
Over-the-Air

Zynq ZC706 Board

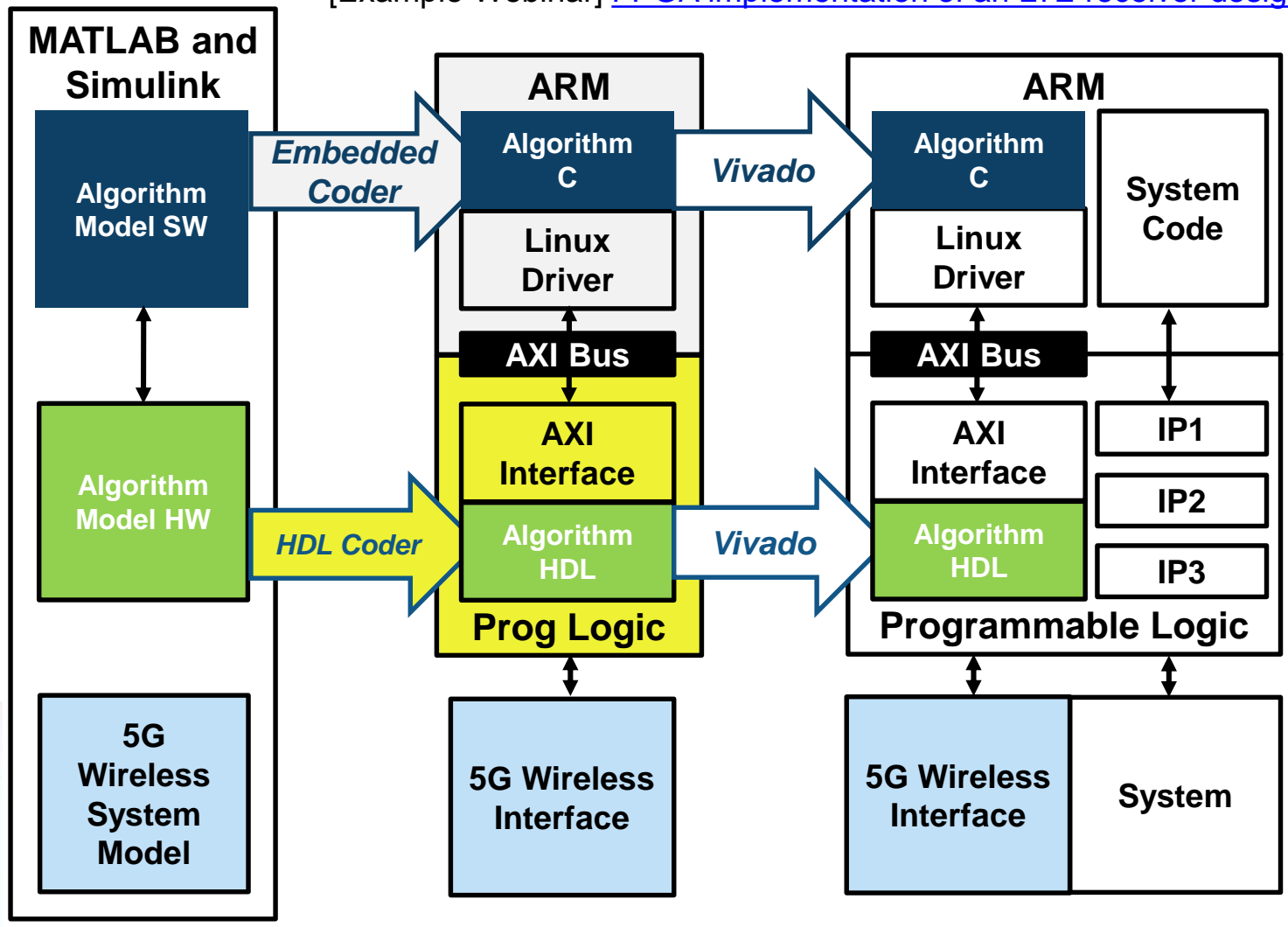


从仿真到实现: Xilinx Zynq + AD9361 SDR

MATLAB code (.m) Simulink Model



[Example Webinar] [FPGA implementation of an LTE receiver design](#)



Ericsson – 射频验证板的设计 Using HDL Coder

Radio Testbed Design Using HDL Coder



Systems & Technology (S&T) is the department at Ericsson responsible for securing technology leadership for Development Unit Radio. S&T is involved in standardization, concept development, and pre-pre-studies of new features, standards, and concepts, and acts as a driver for radio technology strategic work. An important part of this work is the development of test beds to validate and demonstrate new technology. In this session, Tomas shares his experiences incorporating HDL Coder™ into the design workflow of a new test bed radio. He highlights how it has been a key factor in managing the rapid development of a complex FPGA application and how it has enabled the design to quickly adapt to changes in specifications.

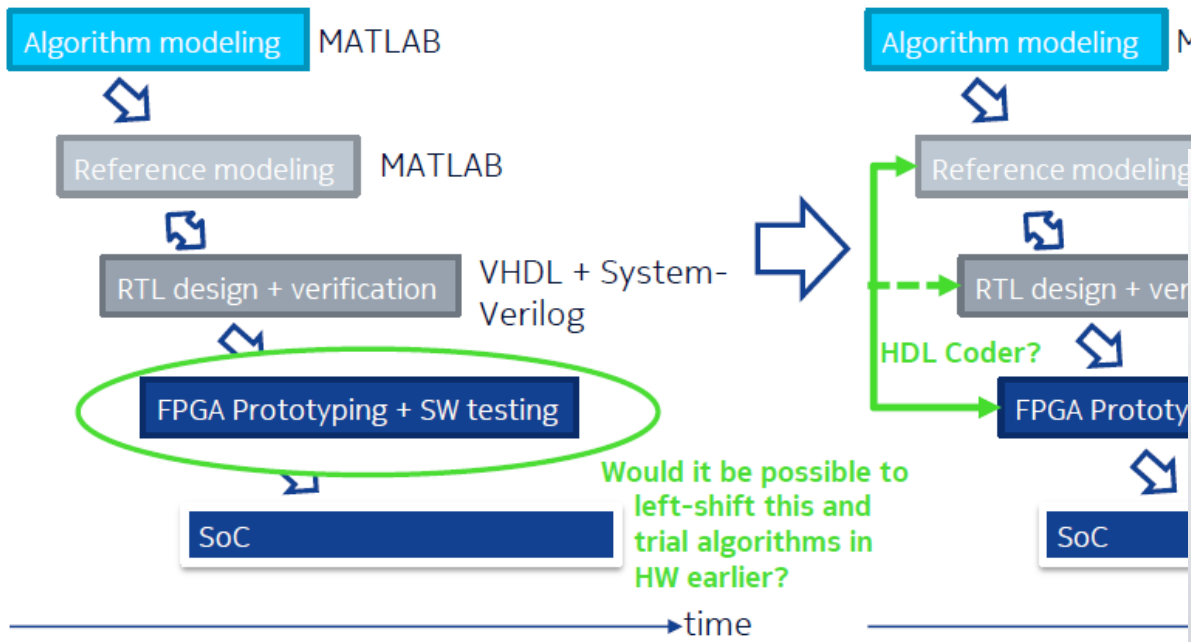


View video online at:

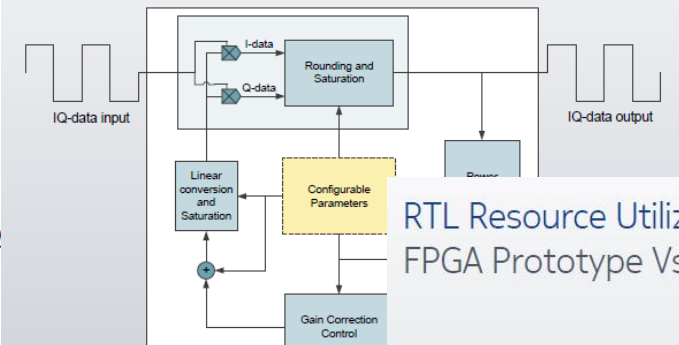
<http://www.mathworks.co.uk/videos/radio-testbed-design-using-hdl-coder-92636.html>

Nokia: 快速原型实现 Using HDL Coder

Challenge



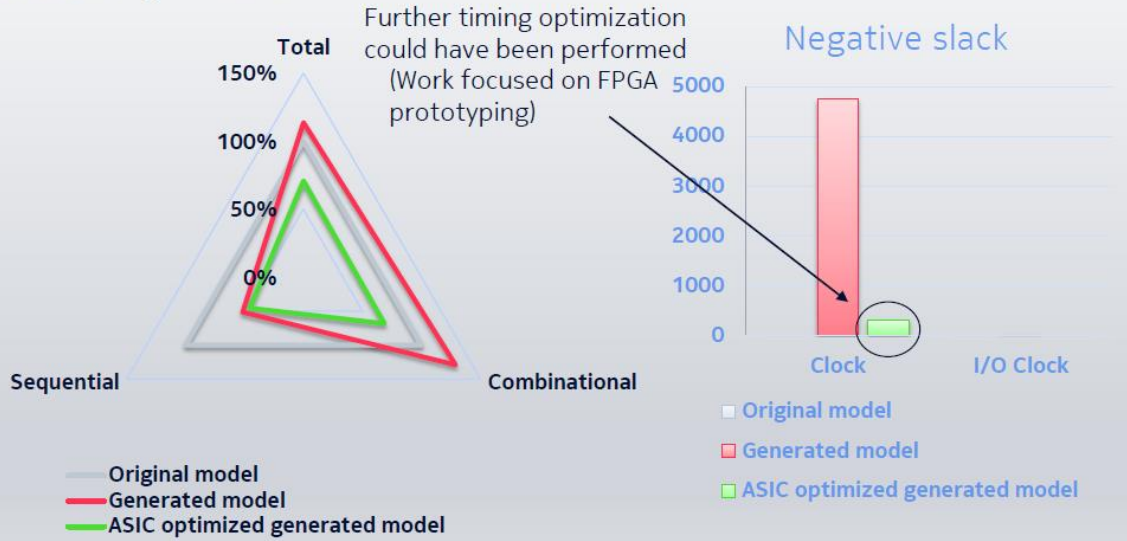
Example Design for HDL Coder Flow Scaling and Power Limitation Block



RTL Resource Utilization Comparison
FPGA Prototype Vs. Original ASIC Targeted Model

Flip-Flops
100%

ASIC Optimization
Area and Timing Results



系统级 ASIC 算法平台 using MATLAB and Simulink

Security Level:

System-Level ASIC Algorithm Simulation Platform using Simulink

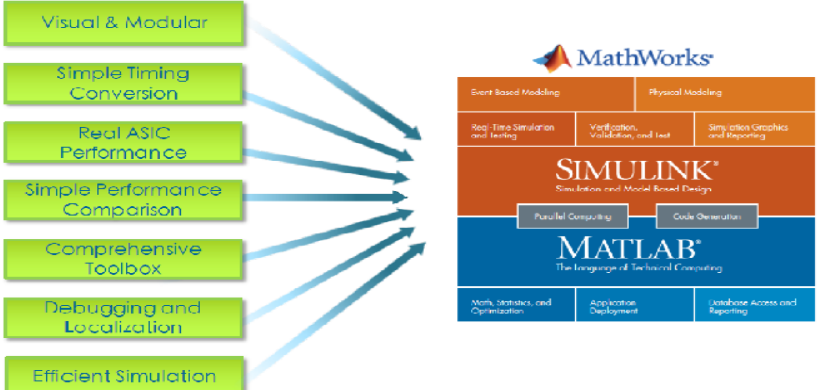
Dr. Sun, Defu
Huawei Technologies Co., LTD.
2015/11/03

www.huawei.com

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ASIC Algorithm Simulation Platform Requirements



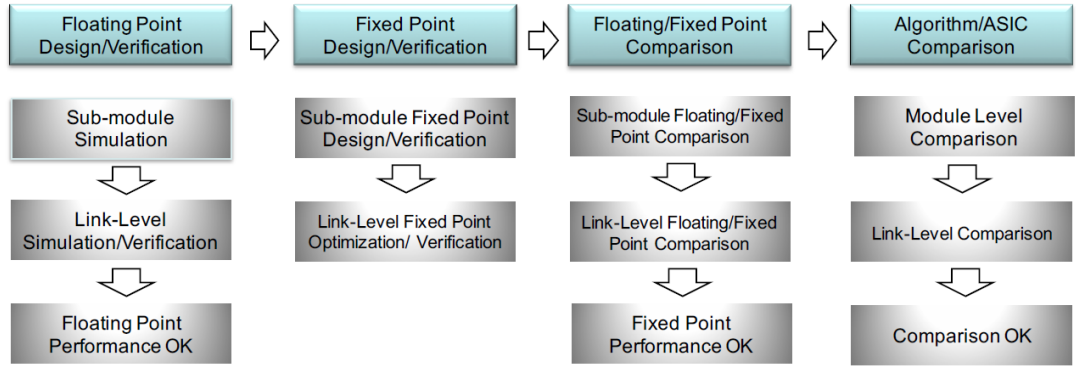
MathWorks MATLAB & Simulink is great for algorithm simulation in ASIC
 Huawei consider it as important ASIC algorithm verification tool

HUAWEI TECHNOLOGIES CO., LTD.

PAGE 11



Algorithm Simulation/Verification Workflow in ASIC



Characteristics of ASIC Algorithm Simulation/Verification

1. System Level Design and Verification of Floating Point Arithmetic
2. Accurate Fixed Point design and Performance Comparison with Floating Point
3. Performance Comparison between Fixed Point Algorithm and RTL in ASIC

Compared to conventional floating point algorithm simulation, for ASIC algorithm verification is more extensive to verify accuracy with high degree of confidence

HUAWEI TECHNOLOGIES CO., LTD.



- Huawei: [System Level ASIC Algorithm Simulation Platform using Simulink](#)

小结与展望

- 5G系统的挑战
 - 多天线, mmWave, 信道模型, 快速原型
- 从算法到天线的的设计
 - MATLAB 统一算法开发平台, 天线, RF, 基带
- 空口的测试
 - 符合5G/LTE行业标准的信号, SDR
- 原型实现
 - 自动C和HDL代码生成, 缩短开发时间

更多信息

- Website
 - <https://www.mathworks.com/discovery/5g-wireless-technology.html>