MATLAB EXPO

Intel® Agilex™ 7 FPGA-in-the-Loop Simulation
Enabling DSP Emulation for Space-BACN

Ziyi Zhu, Platform Hardware Engineer, Intel® PSG CTO Office
Allen Chan, Managing Principal Engineer, Intel® PSG CTO Office
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• DSP Emulation Challenges and Solutions
  ▪ MathWorks FPGA-in-the-Loop (FIL) Simulation
  ▪ Intel® Agilex™ 7 FPGA I-Series
• FIL Architectures for Intel® Agilex™ 7 FPGA I-Series
  ▪ Ethernet (via HPS) - Intel® Agilex™ 7 FPGA I-Series Transceiver-SoC Development Kit
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• FIL Simulation Demo
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DARPA Space-BACN Program

Space-Based Adaptive Communications Node (Space-BACN) program aims to create a reconfigurable intersatellite optical communications terminal that is low size, weight, power, and cost (SWaP-C), and easy to integrate.

It allows seamless communication between heterogeneous constellations that operate on different optical intersatellite link (OISL) specifications, and which otherwise would not be able to communicate.

The program objectives are summarized as “100 Cubed”:
- 100 Gbps to support most optical standards.
- 100W or less to minimize power consumption.
- Under $100K to make it affordable.

Space-BACN will focus on three key technical areas:
- A low-cost, optical aperture capable of coupling into single mode fiber Lower-risk design integration (TA1).
- A reconfigurable modem that can support multiple optical waveforms up to 100 Gbps (TA2).
- A novel cross-constellation command and control approach to automate interactions between government and commercial satellites (TA3).

# TA2 Requirements & DSP Implementation Considerations

**Digital Signal Processing (DSP) Emulation Considerations:**

- **Modulation/Demodulation Formats**
  - OOK, PPM, DPSK, BPSK, QPSK, and DP-QPSK

- **Datarates**
  - Up to 10Gbps OOK & Up to 100Gbps PSK

- **Timing Recovery Loops**
  - Clock Data Recovery (CDR)
  - Doppler + CDR

- **FEC coding**
  - DVB-S2 (LDPC+BCH), SDA (LDPC), OFEC (Turbo), CCSDS (RS, LDPC), G709 (RS)

- **Post-FEC BER**
  - ≤1E-15

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<table>
<thead>
<tr>
<th>TA2 Metric</th>
<th>Phase 1</th>
<th>Phase 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supported modulation formats</td>
<td>Reconfigurable design for OOK, PPM, DPSK, BPSK, QPSK, and DP-QPSK</td>
<td>EDU reconfigurable for OOK, PPM, DPSK, BPSK, QPSK, and DP-QPSK</td>
</tr>
<tr>
<td>Baud rate</td>
<td>Programmable 1-33 G baud</td>
<td>Programmable 1-33 G baud</td>
</tr>
<tr>
<td>Supported datarates</td>
<td>Up to 10 Gbps OOK, up to 100 Gbps PSK</td>
<td>Up to 10 Gbps OOK, up to 100 Gbps PSK</td>
</tr>
<tr>
<td><strong>Transmitter</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Tunable/selectable wavelength range</td>
<td>1.530 nm – 1.565 nm</td>
<td>1.530 nm – 1.565 nm</td>
</tr>
<tr>
<td>Laser RIN</td>
<td>-140 dB/Hz peak, -145 dB/Hz average</td>
<td>-140 dB/Hz peak, -145 dB/Hz average</td>
</tr>
<tr>
<td>Laser spectral linewidth</td>
<td>500 kHz</td>
<td>500 kHz</td>
</tr>
<tr>
<td>Optical output measured in SMF</td>
<td>0 dBm per polarization</td>
<td>0 dBm per polarization</td>
</tr>
<tr>
<td>TX OSNR</td>
<td>&gt;30 dB/0.1 nm</td>
<td>&gt;30 dB/0.1 nm</td>
</tr>
<tr>
<td>TX output polarization</td>
<td>PM-SMF</td>
<td>PM-SMF</td>
</tr>
<tr>
<td><strong>Receiver</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sensitivity at 100G</td>
<td>-18 dBm</td>
<td>-18 dBm</td>
</tr>
<tr>
<td>Post-FEC BER</td>
<td>≤1E-15</td>
<td>≤1E-15</td>
</tr>
<tr>
<td>Optical input</td>
<td>SMF</td>
<td>SMF</td>
</tr>
<tr>
<td>FEC coding supported (code rates ≥1/2)</td>
<td>DVB-S2 (LDPC+BCH), SDA (LDPC), OFEC (Turbo), CCSDS (RS, LDPC), G709 (RS)</td>
<td>Phase 1 + programmable to other variants</td>
</tr>
<tr>
<td>Doppler</td>
<td>Up to ±50 ppm</td>
<td>Up to ±50 ppm</td>
</tr>
</tbody>
</table>

Space-BACN program TA2 metrics:

[https://sam.gov/opp/e704657b448649a4a5ff7debeb39540a/view Space_BACN_Appendix_amended_20210927.pdf](https://sam.gov/opp/e704657b448649a4a5ff7debeb39540a/view Space_BACN_Appendix_amended_20210927.pdf)
DSP Simulation Challenges and Solutions

Does the design implemented in HDL match the specification?

Algorithm Design as Specification

Implemented Hardware Design

Software simulation is SLOW!

Processing 16B+ samples of LTE Turbo Decoder test stimulus can take 21.5 days

MATLAB/Simulink as Test Bench for Hardware IP FPGA-in-the-Loop (FIL)

Relevant Key Features:
- PCI Express (PCIe) 5.0 Support
- Hard Processor System (HPS)
  - Quad-core Arm Cortex-A53
- AGI 027
  - 2700 KLE
  - DDR4

Ethernet FIL Architecture for Agilex

Host PC

MATLAB / Simulink
WRITE READ

TCP/IP

Agilex™ 7 SoC

HPS (Linux)

LibIIO

User Space

mw_stream_iio_channel
Kernel Space

FPGA

MM2S DMA
S2MM DMA

FIL I/F wrapper

DUT

Intel® Agilex™ 7 FPGA I-Series Transceiver-SoC Development Kit (4x F-Tile) DK-SI-AGI027FB

https://www.rocketboards.org/foswiki/Documentation/AgilexSoCGSRDSIAGI027

https://github.com/mathworks/altera-linux/tree/mw-agilex-soc-5.15/drivers/misc/mathworks
PCI-Express FIL Architecture for Agilex (On-going)

- Host PC
  - MATLAB / Simulink
  - WRITE
  - READ

- User Space
  - mcdma-custom-driver

- Kernel Space
  - PCIe

- Agilex™ 7 FPGA
  - R-Tile
  - FPGA fabric
  - Multi Channel DMA for PCI Express
  - Memory
  - MM2S DMA
  - S2MM DMA
  - FIL I/F wrapper
  - DUT

Intel® Agilex™ 7 FPGA I-Series Development Kit (2x R-Tile and 1x F-Tile) DK-DEV-AGI027R1BES


FIL Simulation Demo - LTE Turbo Decoder

Simulink / MATLAB

1. LTE Turbo Data Generation
   - Iteturbo Encode
   - Itesymbol Modulate (QPSK)
   - Transmitte d Frames
   - AWGN (SNR)

2. LTE Turbo Decoder FIL
   - LTE Turbo Decoder Algorithm
   - To Samples
   - To Frames

3. Verify

HPS

FIL I/F wrapper

LTE Turbo Decoder


https://www.mathworks.com/help/lte/ref/lte turbocode.html
FIL Simulation Demo - Results

Decoded bits - Sim vs. FIL (1e6 bits, Eb/No = 0.5)

- Bit and cycle accuracy between the hardware module and the source Simulink model used to generate the RTL code
- Simulation: 518 hours (21.5 days)
- FIL cycle accurate: 48 hours (2 days)
- FIL free running: 23 minutes

1e9 bits per Eb/No value

[Graph showing Bit Error Rate vs. Eb/No]
Notices & Disclaimers

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