External Cleanup PLL
Closed Loop Stability Analysis
and Phase Noise consideration

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This analysis is based on external (board) clean up PLL used with HSS Cores.

Use of clean up PLL allows for utilizing less expensive oscillator and lower Reference frequencies. It also greatly helps to clean recovered clock phase noise from receiver (Rx).

The overall closed loop system peaking (Generally three PLLs chained) may require less than 0.1 dB peaking.

Closed loop analysis of system need to show good stability. 65 degree or better Phase Margin and acceptable Gain Margin.

PLL in HSS core can contribute peaking to overall closed loop system. Generally clean up PLL shows good capability of jitter clean up due to its close loop low bandwidth (i.e. Khz range).
Pole/Zero approximation of three PLLs chained using Matlab RF tool box shows very good correlation to hardware measurements. “rationalfit” function of RF tool box, allows for representation of low entropy transfer function.

Possible large signal (Time domain) simulation of closed loop system can be designed in combination of using Simulink and its communication tool box.

Location and values of Poles and Zeros of the closed loop plotted and calculated. Location of Poles & Zeros in left half side of imaginary axis can further enhance understanding of dominant Poles & Zeros.

Phase noise analysis of recovered clock from HSS receiver, also discussed using utilizing Matlab programming.

Matlab/Simulink interface with software products from independent, third-party services used in this analysis.
High-level System Design Example for External Clean up PLL

PCB

Various clock frequencies

On-board Clocks & Logic
- SETS CLOCK
- Xtal Osc

Customer determines when to switch the mux

Clean-up PLL

HSS PLL

ASIC

TX A

RX A

HSS

TX_CLK

RX_CLK

data

Other Logic?

RXDCLK
This is a loop back at PCB for this analysis.
- Clean up PLL transfer function $TF_1$ synthesized in S-domain.
- Tx PLL transfer function $TF_2$ synthesized in S-domain.
- RX/CDR transfer function $TF_3$ synthesized in S-domain.

$$\frac{\text{Output}}{\text{Input}} = TF = T F_1 \times TF_2 \times TF_3$$

$$TF_{ol} = \frac{(TF_1 \times TF_2 \times TF_3)}{1 - (TF_1 \times TF_2 \times TF_3)}$$

$TF_{ol}$ is used to calculate PM & GM.
Synthesizing clean up PLL closed loop bandwidth

\[ TF_{\text{cleanup_pll}} = \frac{(5.39e16)s + 4.933e20}{s^4 + (5.262e6)s^3 + (1.325e12)s^2 + (6.367e16)s + 4.933e20} \]
Synthesizing Tx JTF

\[ TF_{Tx} = \frac{(4.615e15)s + 6.461e23}{s^3 + (4.42e8)s^2 + (5.157e16)s + 6.461e23} \]

Poles:
-2.2997e8
-1.9783e8
-14.202e6

Zero:
-140e6

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Synthesizing CDR JTF

Measured data

\[
TF_{CDR} = \frac{(1.333e18)s + 2e26}{s^3 + (6.6e8)s^2 + (1.092e18)s + 2e26}
\]
$$TF_{\text{cleanup_pll}} = \frac{5.39e16s + 4.933e20}{s^4 + (5.262e6)s^3 + (1.325e12)s^2 + (6.367e16)s + 4.933e20}$$

$$TF_{\text{Tx}} = \frac{4.615e15s + 6.461e23}{s^3 + (4.42e8)s^2 + (5.157e16)s + 6.461e23}$$

$$TF_{\text{CDR}} = \frac{1.333e18s + 2e26}{s^3 + (6.6e8)s^2 + (1.092e18)s + 2e26}$$
Close Loop system overall Bandwidth

0.0588 dB at 1210 Hz

-3 dB at 8310 Hz
Close Loop system Poles & Zeros

Poles:
-2.3000e+08 + 9.7319e+08i
-2.3000e+08 - 9.7319e+08i
-2.2997e+08
-2.0000e+08
-1.9783e+08
-1.4202e+07
-4.9995e+06
-2.0193e+05
-5.0961e+04
-9.5882e+03

Zeros:
-1.5004e+08
-1.4000e+08
-1.1521e+03
Bode Diagram

$G_m = 39.2 \, \text{dB (at } 1.54e+05 \, \text{Hz)}}$, $P_m = 78.2 \, \text{deg (at } 6.62e+03 \, \text{Hz)}}$
Phase noise analysis of recovered Clock
Calculating input phase noise for TX RefClk (adjusted for Noise floor -145dBC/Hz)

Effect of external clean up PLL and GPLL

RXDCLK phase noise entering external clean up PLL

HSS input RefClk phase noise Mask

Phase noise of TX Input RefClk

Rj = 0.702ps for Noise floor of -140 dBC/Hz and carrier frequency of 311.0 Mhz.
Backup Slides
Possible Methodology for time Domain analysis of closed loop (Under development)

Configure for clean up PLL

Configure for Tx PLL

Configure for RX/CDR

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Example of Buck converter
Ferrite Bead filter

Example of full wave Rectifier providing line Voltage to SMPS

mV range transient noise

Signal & Power Integrity modeling and simulation combining Cadence & Matlab/Simulink